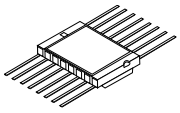
# RHFL4913A

Datasheet

## Rad-hard adjustable positive voltage regulator



**FLAT-16**

**SMD5C:**
5-connection SMD

| Maturity status link |
| --- |
| RHFL4913A |

## Features

- Operating input voltage from 3 V to 12 V
- Adjustable output voltage
- 3 A maximum guaranteed output current in SMD5C package, 2 A in FLAT-16
- Very low dropout voltage: 350 mV typ. @ 400 mA
- Embedded overtemperature and overcurrent protection
- Adjustable overcurrent limitation
- Very low noise: 40 $\mu V_{RMS}$ (10 Hz-100 kHz)
- Output overload monitoring/signalling
- Inhibit (ON/OFF) TTL-compatible control
- Programmable output short-circuit current
- Remote sensing operation
- Low quiescent current: 1.5 mA typ. @ no load, 150 µA in shutdown
- Rad-hard: guaranteed up to 300 krad Mil Std 883E Method 1019.6 high dose rate and 0.01 rad/s in ELDRS conditions
- Heavy ion, SEL immune.

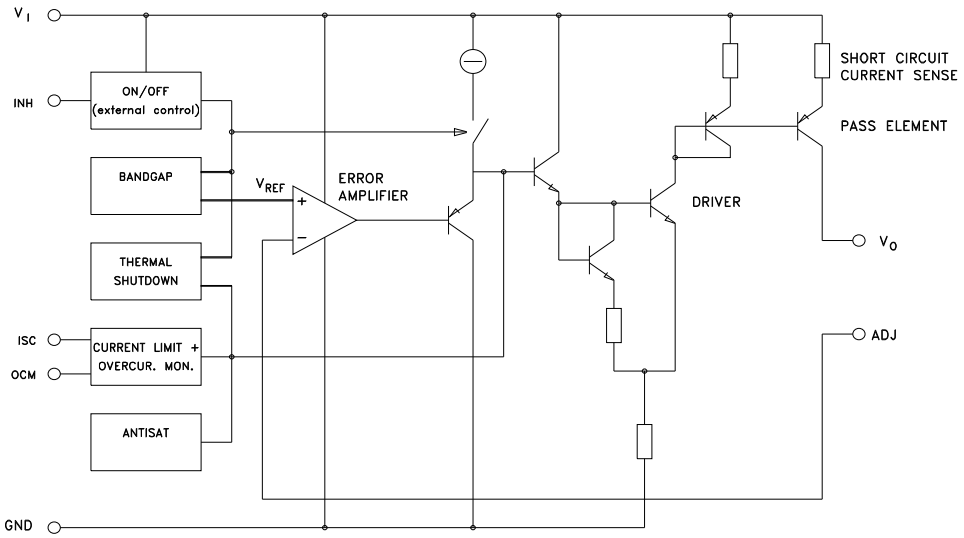
## Description

The RHFL4913A is a high-performance adjustable positive voltage regulator, able to provide 2 A of maximum current in FLAT-16 package (3 A in the SMD5C package) from an input voltage ranging from 3 V to 12 V, with a typical dropout voltage of 350 mV.

The RHFL4913A features exceptional radiation performances. It is tested in accordance with Mil Std 883E Method 1019.6, in ELDRS conditions. The device is available in the FLAT-16 and the SMD5C hermetic ceramic package, and the QML-V die is suitable for harsh environments. It operates with an input supply of up to 12 V. The RHFL4913A is QML-V qualified, DSCC SMD #5962F02524.

# 1 Diagram

**Figure 1. Block diagram**

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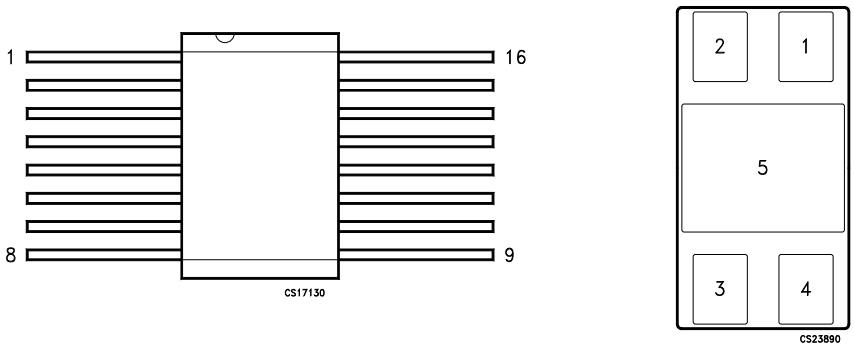
# 2 Pin configuration

**Figure 2. Pin configuration (top view for FLAT-16, bottom view for SMD5C)**




FLAT-16 SMD5C

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**Table 1. Pin description**

| Pin name | FLAT-16 (1) | SMD5C (2) |
|---|---|---|
| $V_O$ | 1, 2, 6, 7 | 1 |
| $V_I$ | 3, 4, 5 | 4 |
| GND | 13 | 5 |
| $I_{SC}$ | 8 | |
| OCM | 10 | |
| INHIBIT | 14 | 3 |
| ADJ | 15 | 2 |
| NC | 9, 11, 12, 16 | |

1. *The upper metallic package lid and the bottom metallization are neither connected to regulator die nor to package terminals, hence electrically floating.*
2. *The upper metallic package lid is neither connected to regulator die nor to package terminals, hence electrically floating.*

# 3 Maximum ratings

**Table 2. Recommended maximum operating ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_I$ | DC input voltage, $V_I$ - $V_{GROUND}$ | 12 | V |
| $V_O$ | DC output voltage range | 1.23 to 9 | V |
| $V_{ADJ}$ | ADJ pin voltage | -0.3 to ($V_O$ + 0.3) | V |
| $V_{OCM}$ | Over current monitor pin voltage vs. GND | -0.3 to ($V_I$ + 0.3) | V |
| $V_{ISC}$ | Current limit pin voltage vs. GND | -0.3 to ($V_I$ + 0.3) | V |
| $V_{INHIBIT}$ | Inhibit pin voltage vs. GND | -0.3 to ($V_I$ + 0.3) | V |
| $I_O$ | Output current, RHFL4913KPA | 2 | A |
| $I_O$ | Output current, RHFL4913SCA | 3 | |
| $P_D$ | $T_C$ = 25 °C power dissipation | 15 | W |
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |
| $T_{OP}$ | Operating junction temperature range | -55 to +150 | °C |
| $E_{SD}$ | Electrostatic discharge capability | Class 3 | |

*Note: Exceeding maximum ratings may damage the device.*

**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Thermal resistance junction-case, FLAT-16 and SMD5C | 8.3 | °C/W |
| $T_{SOLD}$ | Maximum soldering temperature, 10 sec. | 300 | °C |

# 4 Electrical characteristics

$T_J$ = 25 °C, $V_I$ = $V_O$ + 2.5 V, $C_I$ = $C_O$ = 1 µF, unless otherwise specified.

**Table 4. Electrical characteristics**

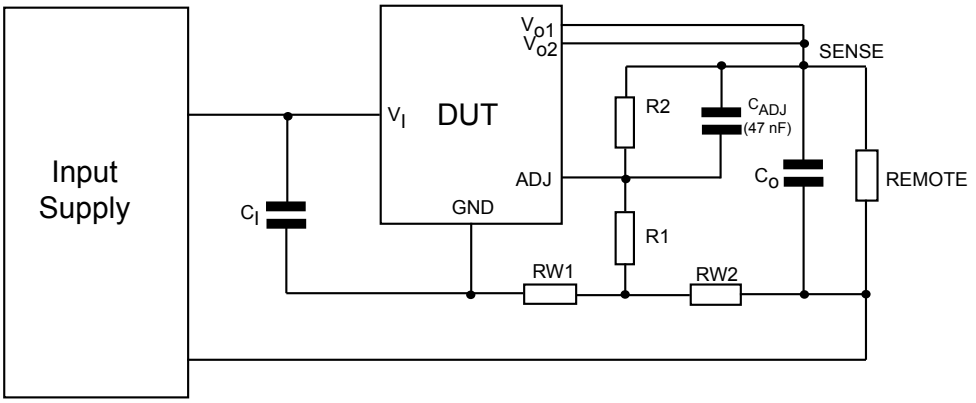
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_I$ | Operating input voltage | $I_O$ = 1 A, $T_J$ = -55 to 125 °C | 3 | | 12 | V |
| $V_O$ | Output voltage | $I_O$ = 1 A for FLAT-16, 2 A for SMD5C, $V_O$ = $V_{ADJ}$ | 1.19 | 1.23 | 1.27 | V |
| | | $I_O$ = 1 A for FLAT-16, 2 A for SMD5C, $V_O$ = 9 V | 8.7 | | 9.3 | |
| $I_{SHORT}$ | Output current limit (1) | Adjustable by mask/external resistor | 1 | 4.5 | | A |
| $\Delta V_O/\Delta V_I$ | Line regulation | $V_I$ = $V_O$ +2.5 V to 12 V, $I_O$ = 5 mA, $T_J$ = +25 °C | | 0.07 | 0.35 | % |
| | | $V_I$ = $V_O$ +2.5 V to 12 V, $I_O$ = 5 mA, $T_J$ = -55 °C | | 0.05 | 0.4 | |
| | | $V_I$ = $V_O$ +2.5 V to 12 V, $I_O$ = 5 mA, $T_J$ = +125 °C | | 0.1 | 0.4 | |
| | | $V_I$ = 3 V to 12 V, $I_O$ = 5 mA, $T_J$ = -55 °C to +125 °C | | 0.1 | 0.5 | |
| $\Delta V_O/\Delta I_O$ | Load regulation | $V_I$ = $V_O$ + 2.5 V, $I_O$ = 5 to 400 mA, $T_J$ = +25 °C | | 0.04 | 0.3 | % |
| | | $V_I$ = $V_O$ + 2.5 V, $I_O$ = 5 to 400 mA, $T_J$ = -55 °C | | 0.02 | 0.5 | |
| | | $V_I$ = $V_O$ + 2.5 V, $I_O$ = 5 to 400 mA, $T_J$ = +125 °C | | 0.02 | 0.5 | |
| | | $V_I$ = $V_O$ + 2.5 V, $I_O$ = 5 mA to 1 A, $T_J$ = +25 °C | | 0.08 | 0.5 | |
| | | $V_I$ = $V_O$ + 2.5 V, $I_O$ = 5 mA to 1 A, $T_J$ = -55 °C | | 0.05 | 0.6 | |
| | | $V_I$ = $V_O$ + 2.5 V, $I_O$ = 5 mA to 1 A, $T_J$ = +125 °C | | 0.04 | 0.6 | |
| | | $V_I$ = 3 V, $I_O$ = 5 mA to 1 A, $T_J$ = -55 °C to +125 °C | | 0.1 | 0.7 | |
| $Z_{OUT}$ | Output impedance | $I_O$ = 100 mA DC and 20 mA rms | | 100 | | mΩ |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_q$ | Quiescent current | $V_I = V_O + 2.5$ V,<br>$I_O = 5$ mA,<br>ON mode (+25 °C) | | 1.5 | 6 | mA |
| | | $V_I = V_O + 2.5$ V,<br>$I_O = 30$ mA,<br>ON mode (+25 °C) | | 2.7 | 8 | |
| | | $V_I = V_O + 2.5$ V,<br>$I_O = 300$ mA,<br>ON mode (+25 °C) | | 11 | 25 | |
| | | $V_I = V_O + 2.5$ V,<br>$I_O = 1$ A,<br>ON mode (+25 °C) | | 32 | 60 | |
| $I_{q(on)}$ | Quiescent current<br>ON mode | $V_I = V_O + 2.5$ V,<br>$I_O = 30$ mA, (-55 °C) | | 3 | 14 | mA |
| | | $V_I = V_O + 2.5$ V,<br>$I_O = 300$ mA, (-55 °C) | | 15 | 40 | |
| | | $V_I = V_O + 2.5$ V,<br>$I_O = 1$ A, (-55 °C) | | 52 | 100 | |
| | | $V_I = V_O + 2.5$ V,<br>$I_O = 30$ mA, (+125 °C) | | 3 | 8 | |
| | | $V_I = V_O + 2.5$ V,<br>$I_O = 300$ mA, (+125 °C) | | 8 | 20 | |
| | | $V_I = V_O + 2.5$ V,<br>$I_O = 1$ A, (+125 °C) | | 20 | 40 | |
| $I_{q(off)}$ | Quiescent current<br>Shutdown mode | $V_I = V_O + 2$ V,<br>$V_{INH} = 2.4$ V,<br>OFF mode | | 0.15 | 1 | mA |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_d$ | Dropout voltage | $I_O$ = 0 mA, $V_O$ = 2.5 V to 9 V | | 130 | | mV |
| | | $I_O$ = 400 mA, $V_O$ = 2.5 to 9 V, (+25 °C) | | 350 | 450 | |
| | | $I_O$ = 400 mA, $V_O$ = 2.5 to 9 V, (-55 °C) | | 300 | 400 | |
| | | $I_O$ = 400 mA, $V_O$ = 2.5 to 9 V, (+125 °C) | | 450 | 550 | |
| | | $I_O$ = 1 A, $V_O$ = 2.5 to 9 V, (+25 °C) | | 500 | 650 | |
| | | $I_O$ = 1 A, $V_O$ = 2.5 to 9 V, (-55 °C) | | 400 | 550 | |
| | | $I_O$ = 1 A, $V_O$ = 2.5 to 9 V, (+125 °C) | | 640 | 800 | |
| | | $I_O$ = 2 A, $V_O$ = 2.5 to 9 V, (+25 °C) | | 750 | | |
| | | $I_O$ = 2 A, $V_O$ = 2.5 to 9 V, (+125 °C) | | 950 | | |
| $V_{INH(ON)}$ | Inhibit voltage | $I_O$ = 5 mA, $T_J$ = -55 to +125 °C | | | 0.8 | V |
| $V_{INH(OFF)}$ | Inhibit voltage | $I_O$ = 5 mA, $T_J$ = -55 to +125 °C | 2.4 | | | |
| SVR | Supply voltage rejection (1) | $V_I$ = $V_O$ + 2.5 V ± 0.5 V, $V_O$ = 3 V, $I_O$ = 5 mA f = 120 Hz | 60 | 70 | | dB |
| | | $V_I$ = $V_O$ + 2.5 V ± 0.5 V, $V_O$ = 3 V, $I_O$ = 5 mA f = 33 kHz | 30 | 40 | | |
| $I_{SH}$ | Shutdown input current | $V_{INH}$ = 5 V | | 15 | | µA |
| $V_{OCM}$ | OCM pin voltage | Sinked $I_{OCM}$ = 24 mA active low | | 0.38 | | V |
| $t_{PLH}$ $t_{PHL}$ | Inhibit propagation delay (1) | $V_I$ = $V_O$ + 2.5 V, $V_{INH}$ = 2.4 V, $I_O$ = 400 mA, $V_O$ = 3 V | ON-OFF | | 20 | µs |
| | | | OFF-ON | | 100 | µs |
| eN | Output noise voltage (1) | B = 10 Hz to 100 kHz, $I_O$ = 5 mA to 2 A | | 40 | | µVrms |

1. *These values are guaranteed by design. For each application it is strongly recommended to comply with the maximum current limit of the package used.*

**Figure 3. Application diagram for remote sensing operation**

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# 5 Device description

The RHFL4913A adjustable voltage regulator contains a PNP type power element controlled by a signal resulting from an amplified comparison between the internal temperature-compensated band-gap and the fraction of the desired output voltage value obtained from an external resistor divider bridge. The device is protected by several functional blocks.

## 5.1 ADJ pin

The load output voltage feedback comes from an external resistor divider bridge mid-point connected to the ADJ pin (allowing all possible output voltage settings as per user requirements) established between load terminals.

## 5.2 Inhibit ON-OFF control

By setting the INHIBIT pin TTL high, the device switches off the output current and voltage. The device is ON when the INHIBIT pin is set low. Since the INHIBIT pin is pulled down internally, it can be left floating in cases where the inhibit function is not used.

## 5.3 Overtemperature protection

A temperature detector internally monitors the power element junction temperature. The device turns off when a temperature of approximately 175 °C is reached, returning to ON mode when back to approximately 135 °C. Combined with the other protection blocks, the device is protected from destructive junction temperature excursions in all load conditions. It should be noted that when the internal temperature detector reaches 175 °C, the active power element can be as high as 225 °C. Prolonged operation under these conditions far exceeds the maximum operating ratings and device reliability cannot be guaranteed.

## 5.4 Programmable overcurrent protection

An internal non fold-back short circuit limitation is set with $I_{SHORT}$ > 3.8 A ($V_O$ is 0 V). This value can be decreased via an external $R_{SH}$ resistor connected between the $I_{SC}$ and $V_I$ pins, with a typical value range of 10 kΩ to 200 kΩ (refer to Figure 44. Short circuit current vs. $R_{SH}$ and Figure 45. Short circuit current vs. $R_{SH}$ (zoom)).To maintain optimal $V_O$ regulation, it is necessary to set $I_{SHORT}$ 1.6 times greater than the maximum desired application $I_O$. When $I_O$ reaches $I_{SHORT}$ – 300 mA, the current limiter overrules the regulation, $V_O$ starts to drop and the OCM flag is raised. When no current limitation adjustment is required, the $I_{SC}$ pin must be left unbiased (as it is in 3 pin packages).

## 5.5 OCM pin

The OCM pin goes low when the current limit becomes active, otherwise $V_{OCM} = V_I$. It is buffered and can sink 10 mA. The OCM pin is internally pulled up by a 5 kΩ resistor.

# 6 Application information

To adjust the output voltage, the R2 resistor must be connected between the $V_O$ and ADJ pins. The R1 resistor must be connected between ADJ and ground. Resistor values can be derived from the following formula:

$V_O = V_{ADJ}$ (R1+ R2) / R1

The $V_{ADJ}$ is typically 1.23 V, controlled by the internal temperature-compensated band gap block.

The minimum input voltage is 3 V. The RHFL4913A adjustable is functional as soon as the $V_I$ - $V_O$ voltage difference is slightly above the power element saturation voltage. The adjust pin to ground resistor (R1) value must not be greater than 10 kΩ, in order to keep the output feedback error below 0.2 %. A minimum of 0.5 mA $I_O$ must be set to ensure perfect no-load regulation. It is advisable to dissipate this current into the divider bridge resistor.

All available $V_I$ pins, as well as all available $V_O$ pins, should always be externally interconnected, otherwise the stability and reliability of the device cannot be guaranteed.

The inhibit function switches off the output current electronically, and therefore very quickly. According to Lenz's law, external circuitry reacts with LdI/dt terms which can be of high amplitude in case somewhere a serial coil inductance exists. Large transient voltage would develop on both device terminals. It is advisable to protect the device with Schottky diodes to prevent negative voltage excursions. In the worst case, a 14 V Zener diode could protect the device input.

Since the RHFL4913A adjustable voltage regulator is manufactured with very high speed bipolar technology (6 GHz $f_T$ transistors), the PCB layout must be designed with exceptional care, with very low inductance and low mutually coupling lines. Otherwise, high frequency parasitic signals may be picked up by the device resulting in system self-oscillation. The benefit is an SVR performance extended to far higher frequencies.

## 6.1 Output capacitor selection and stability.

The device has been designed for high stability and low dropout operation.

To ensure regulator stability, input and output capacitors with a minimum 1 µF are mandatory. When large transient currents are expected, larger value capacitors are necessary. The detailed stability plane versus output capacitance and ESR is shown in Figure 54. Stability plan ($V_{out} = V_{adj}$).

In the case of high current operation with short circuit events expected, caution must be exercised with regard to capacitors. They must be connected as close as possible to the device terminals. As some tantalum capacitors may permanently fail when subjected to high charge-up surge currents, it is recommended to decouple them with 470 nF polyester capacitors.

## 6.2 Remote sensing operation

A separate kelvin voltage sensing line provides the ADJ pin with exact load "high potential" information (see Figure 3. Application diagram for remote sensing operation). But variable remote load current consumption induces variable Iq current (Iq is roughly the $I_O$ current divided by the $h_{FE}$ of the internal PNP series power element) routed through the parasitic series line resistor RW2. To compensate for this parasitic voltage, resistor RW1can be introduced to provide the necessary compensating voltage signal to the ADJ pin.

A ceramic or poliester 47nF $C_{ADJ}$ capacitor between ADJ and $V_{OUT}$ pins is recommended when the remote sensing technique is implemented.

## 6.3 FPGA power supply lines

Because FPGA devices are very sensitive to $V_{DD}$ transients beyond a few % of their nominal supply voltage (usually 1.5 V), special attention must be given by supply lines designers to mitigate possible heavy ion disturbances. The worst case heavy ion effect can be summarized as: the RHFL4913 internal control loop being cut (made open) or short-circuited for a sub-microsecond duration. During such an event, the RHFL4913 power element can either provide excessive current or current supply stoppage to the output ($V_{OUT}$) for a duration of about one microsecond, after which time the RHFL4913 smoothly recovers to nominal operation.

According to the simulations, some very short SET (i.e. those having duration < 100 nsec) are dependent also on the stray inductances related to the PCB topology, especially those on the ground.

To mitigate these "transients", it is recommended to implement the RHFL4913 PCB layout as follows:

- Minimizing series/parallel parasitic inductances of the PCB path
- Using an effective grounding scheme with short connections to GND, such as a star-bus topology, whose board GND is at the GND force. The best solution is a ground plane.
- Using a low ESR 47 µF $C_{OUT}$ filtering capacitor, with ESR lower than 30 mΩ, together with a 470 nF ceramic capacitor in parallel (to reduce dynamic ESR)
- Implementing the SET mitigation circuit, by adding additional filtering components as described in Figure 4. Baseline bias configuration with remote feedback and Figure 5. Local feedback configuration.

With this implementation, the ELDO simulated worst transient case shows no more than 90 mV deviation from the nominal line voltage value.

Additional details and suggestions regarding the application techniques aimed to mitigate the SET effects on a linear voltage regulator can be found in the AN2984 (“Minimizing the SET-related effects on the output of a voltage linear regulator, available on www.st.com).

**Figure 4. Baseline bias configuration with remote feedback**

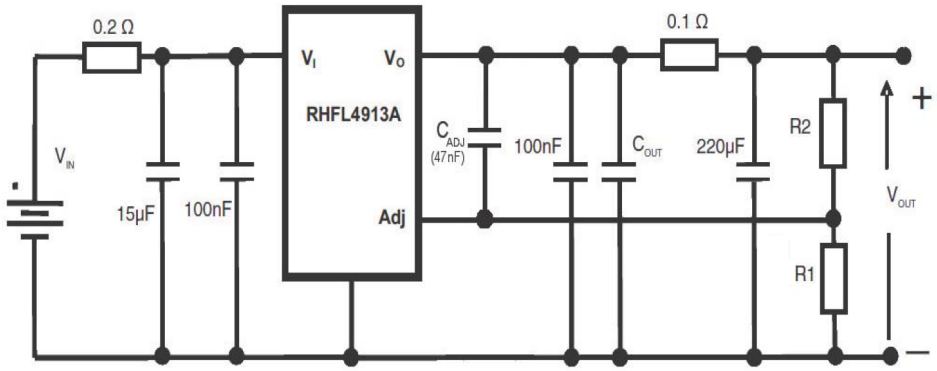
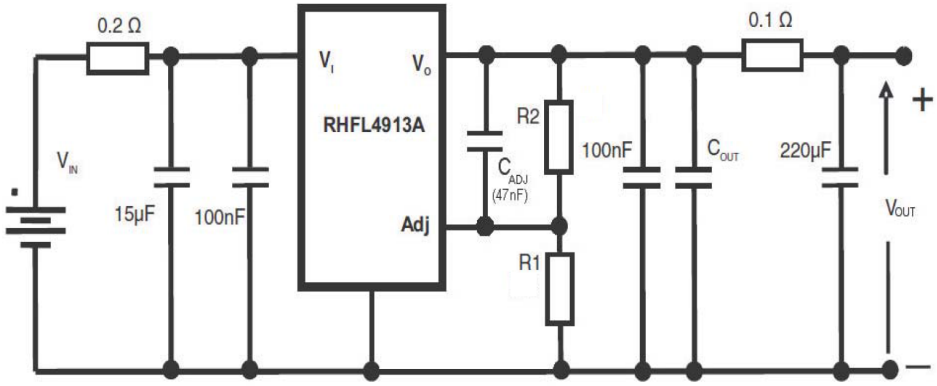



**Figure 5. Local feedback configuration**



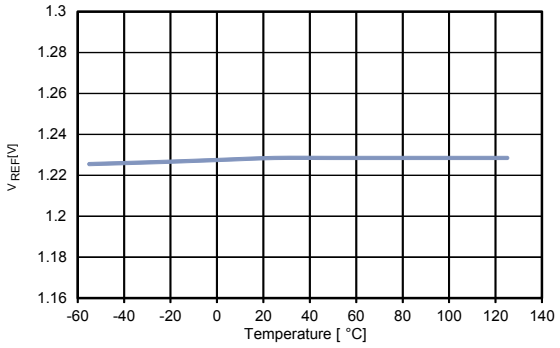
## 6.4 Notes on the 16-pin hermetic package

The bottom section of the 16-pin package is metallized in order to allow the user to directly solder the RHFL4913A onto PCB, no heat sink needed for enhanced heat removal.

This AlN ceramic package features a low thermal coefficient of expansion (TCE) significantly lower than the TCE of some PCBs. It is therefore recommended, especially when its bottom metallic dissipation plate is brazed (as opposed to glued), to carefully design the PCB (material, thickness, layout…) and the mounting process to secure that the package and the solder joint can sustain the worst case temperature cycling its must be qualified for (highest constraints are at lowest temperature). It is strongly recommended to make sure that the actual mounting is well covered by the qualified mounting process for each parameters (PCB material, thickness, layout, temperature profile...).

# 7 Typical characteristics

**Figure 6. Reference voltage vs. temp. ($V_{in}$ = $V_{out}$ + 2.5 V)**




Vin=Vout+2.5V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =5mA

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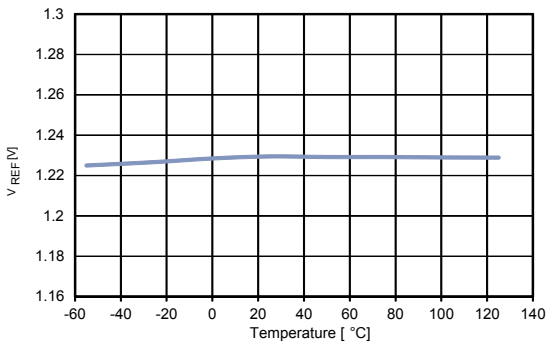
**Figure 7. Reference voltage vs. temp. ($V_{in}$ = 12 V)**




Vin=12V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =5mA

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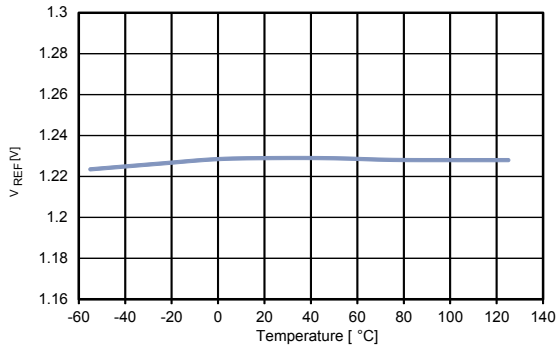
**Figure 8. Reference voltage vs. temp. ($V_{in}$ = $V_{out}$ + 2.5 V, $I_{out}$ = 1 A)**




Vin=Vout+2.5V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =1A

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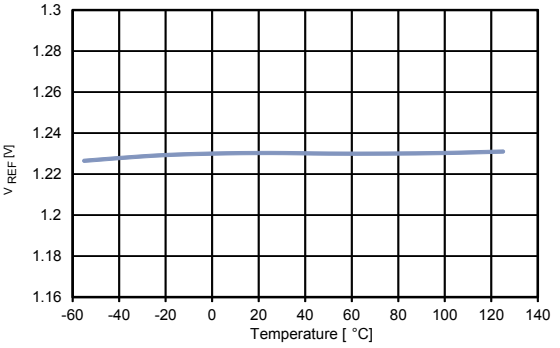
**Figure 9. Reference voltage vs. temp. ($V_{in}$ = 12 V, $I_{out}$= 1 A)**




Vin=12V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =1A

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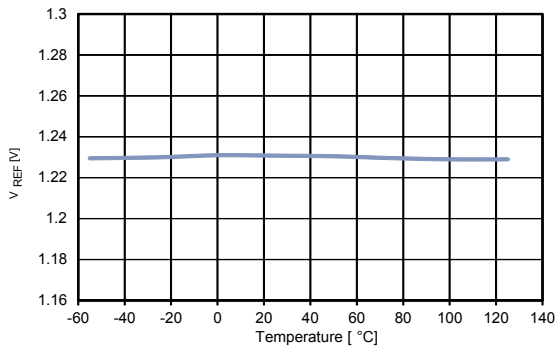
**Figure 10. Reference voltage vs. temp. ($V_{in}$ = $V_{out}$ + 2.5 V, $I_{out}$ = 2 A)**




Vin=Vout+2.5V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =2A

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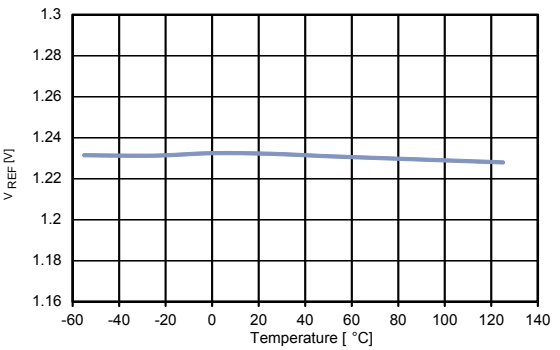
**Figure 11. Reference voltage vs. temp. ($V_{in}$ = 12 V, $I_{out}$= 2 A)**




Vin=12V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =2A

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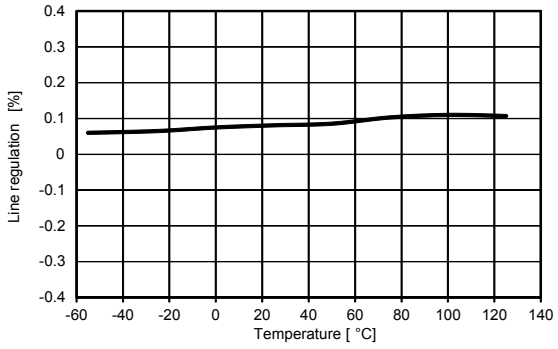
**Figure 12. Line regulation vs. temperature**




Vout+2.5V <Vin < 12V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =5mA

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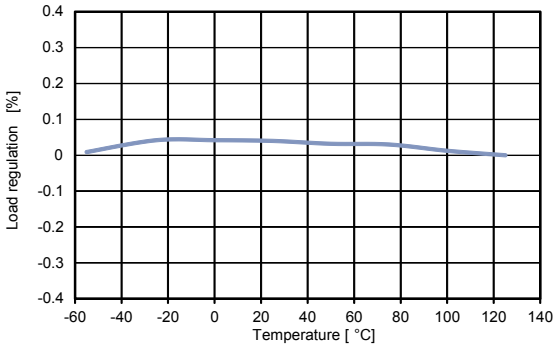
**Figure 13. Load regulation vs. temp. ($I_{out}$ = 5 mA to 400 mA)**




Vin =Vout+2.5V , Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), 5mA< Iout <0.4A

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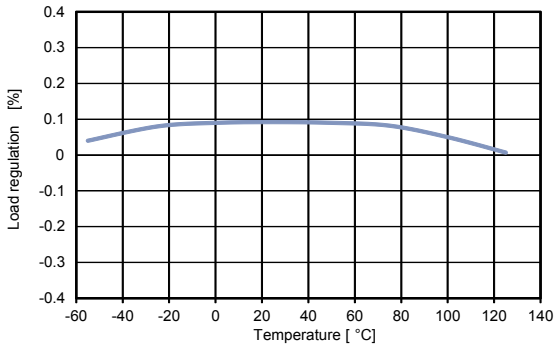
**Figure 14. Load regulation vs. temp. ($I_{out}$ = 5 mA to 1 A)**




Vin =Vout+2.5V , Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), 5mA< Iout <1A

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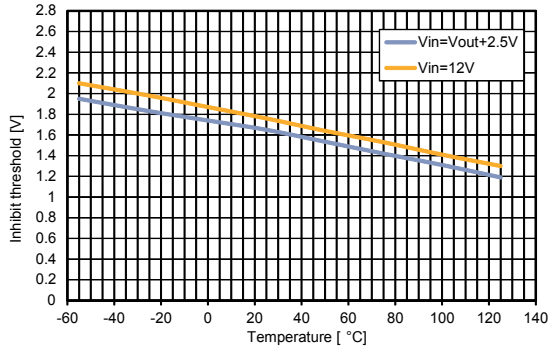
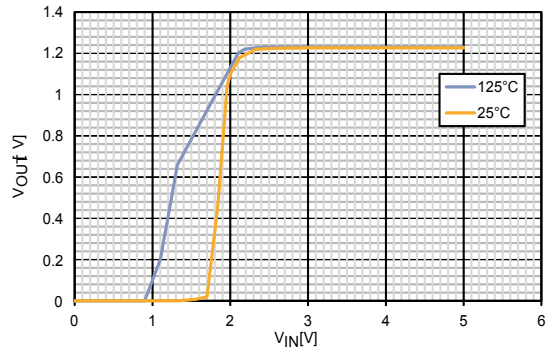
**Figure 15. Inhibit threshold vs. temperature**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), no load

AMG081120161314MT

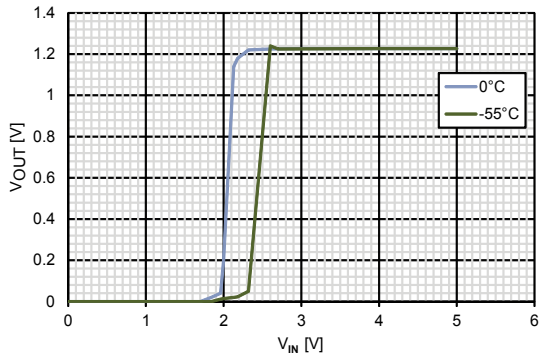
**Figure 16. Output voltage vs. input voltage ($I_{out}$ = 0 mA, T = 25 °C and T = 125 °C)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), No load, T=25°C, T=125°C

AMG081120161315MT

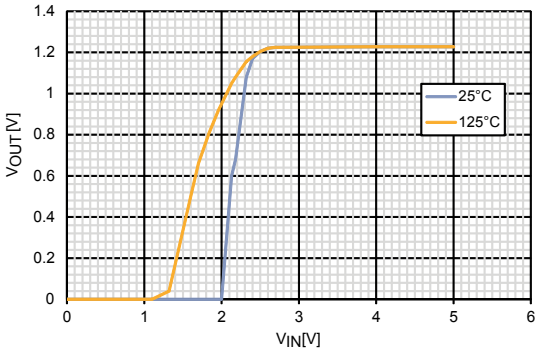
**Figure 17. Output voltage vs. input voltage ($I_{out}$ = 0 mA, T = 0 °C and T = -55 °C)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), No load, T=0°C, T= -55°C

AMG081120161316MT

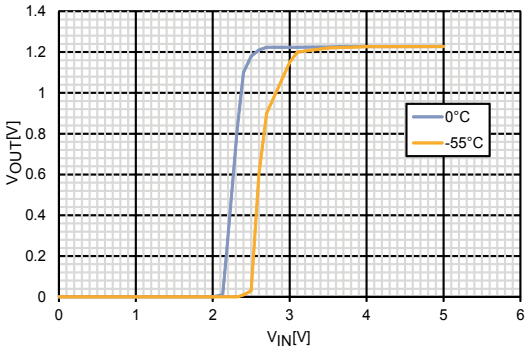
**Figure 18. Output voltage vs. input voltage ($I_{out}$ = 3 A, T = 25 °C and T = 125 °C)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =3A, T=25°C, T=125°C

AMG081120161317MT

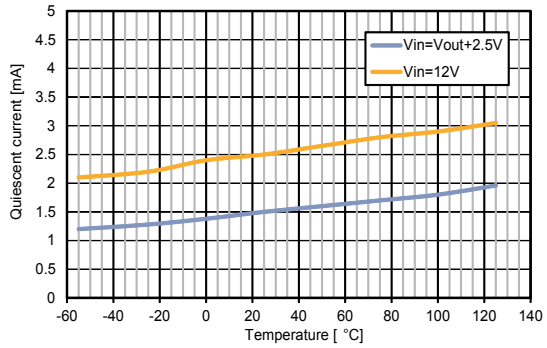
**Figure 19. Output voltage vs. input voltage ($I_{out}$ = 3 A, T = 0 °C and T = -55 °C)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout =3A, T=0°C, T= -55°C

AMG081120161318MT

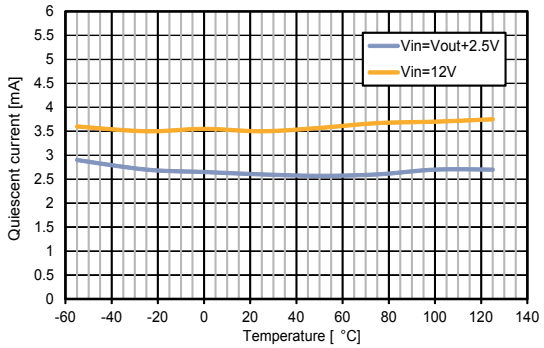
**Figure 20. Quiescent current vs. temp. (no load)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), No load

AMG081120161319MT

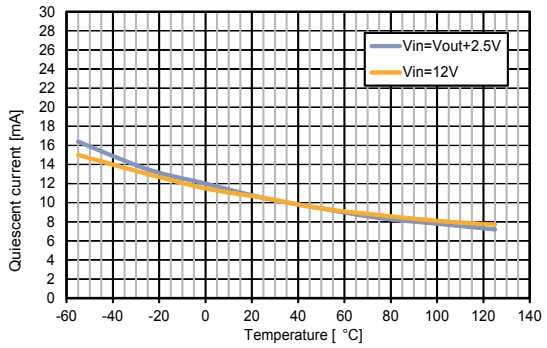
**Figure 21. Quiescent current vs. temp. ($I_{out}$ = 30 mA)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout = 30mA

AMG081120161320MT

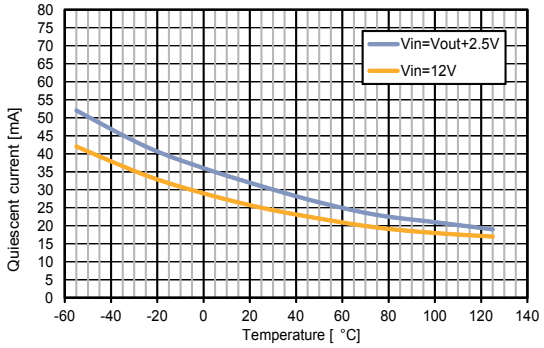
**Figure 22. Quiescent current vs. temp. ($I_{out}$ = 300 mA)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout = 300mA

AMG081120161321MT

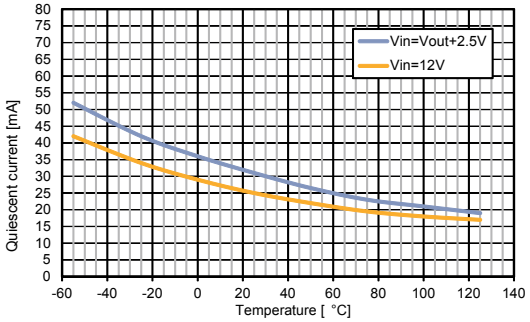
**Figure 23. Quiescent current vs. temp. ($I_{out}$ = 1 A)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout = 1A

AMG081120161322MT

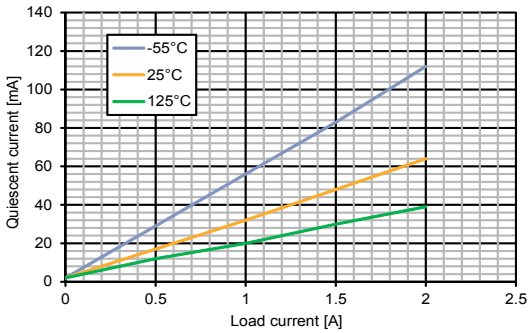
**Figure 24. Quiescent current vs. temp. ($I_{out}$ = 2 A)**




Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant ), Iout = 1A

AMG081120161323MT

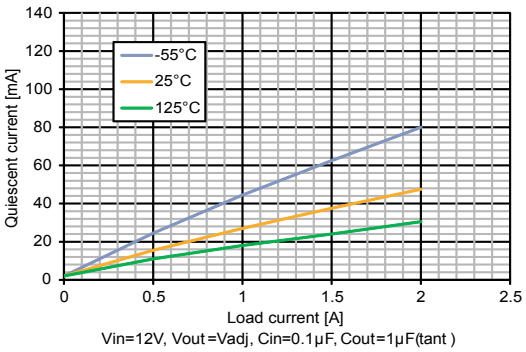
**Figure 25. Quiescent current vs. load current, ($V_{in}$ = $V_{out}$ + 2.5 V)**




Vin=Vout+2.5V, Vout =Vadj , Cin=0.1 µF, Cout =1 µF(tant )

AMG081120161324MT

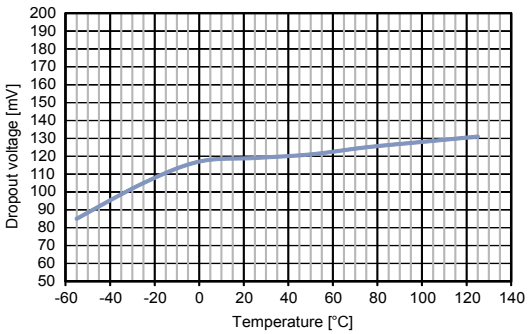
**Figure 26. Quiescent current vs. load current, ($V_{in}$ = 12 V)**




Vin=12V, Vout =Vadj, Cin=0.1 µF, Cout=1 µF(tant )

AMG081120161325MT

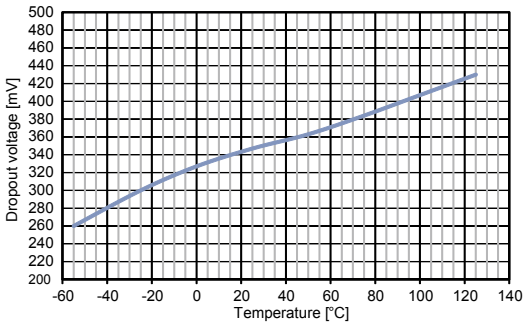
**Figure 27. Dropout voltage vs. temp. ($V_{out}$ = 3 V, no load)**




Vout = 3V, Cin=0.1µF, Cout=1µF(tant), No Load

AMG081120161326MT

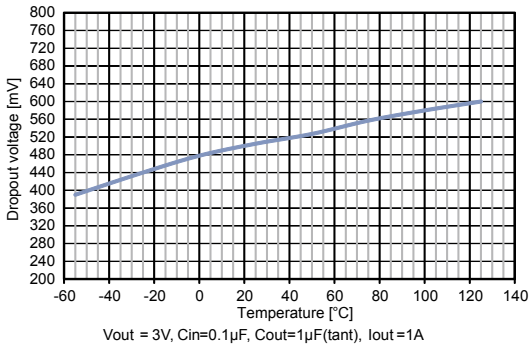
**Figure 28. Dropout voltage vs. temp. ($V_{out}$ = 3 V, $I_{out}$ = 400 mA)**




Vout = 3V, Cin=0.1µF, Cout=1µF(tant), Iout =400mA

AMG081120161327MT

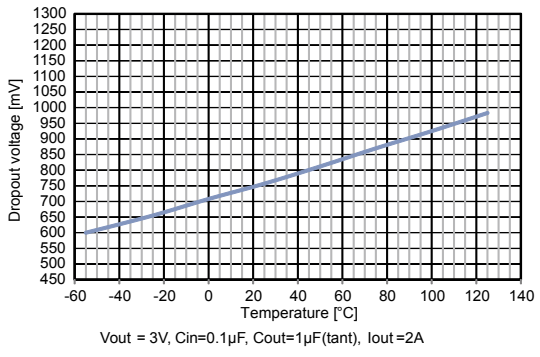
**Figure 29. Dropout voltage vs. temp. ($V_{out}$ = 3 V, $I_{out}$ = 1 A)**




Vout = 3V, Cin=0.1µF, Cout=1µF(tant), Iout =1A

AMG081120161328MT

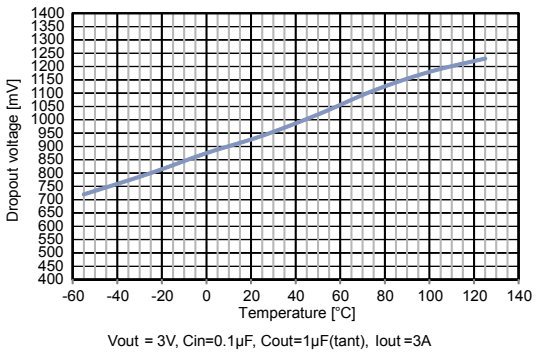
**Figure 30. Dropout voltage vs. temp. ($V_{out}$ = 3 V, $I_{out}$= 2 A)**




Vout = 3V, Cin=0.1µF, Cout=1µF(tant), Iout =2A

AMG081120161329MT

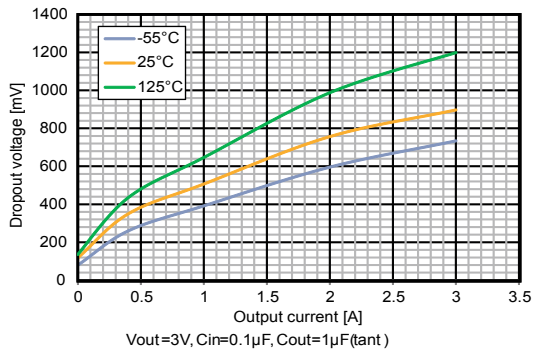
**Figure 31. Dropout voltage vs. temp. ($V_{out}$ = 3 V, $I_{out}$= 3 A)**




Vout = 3V, Cin=0.1µF, Cout=1µF(tant), Iout =3A

AMG081120161330MT

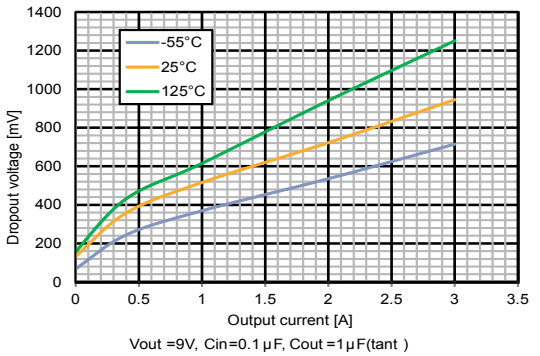
**Figure 32. Dropout voltage vs. load current ($V_{out}$ = 3 V)**




Vout=3V, Cin=0.1µF, Cout=1µF(tant )

AMG081120161331MT

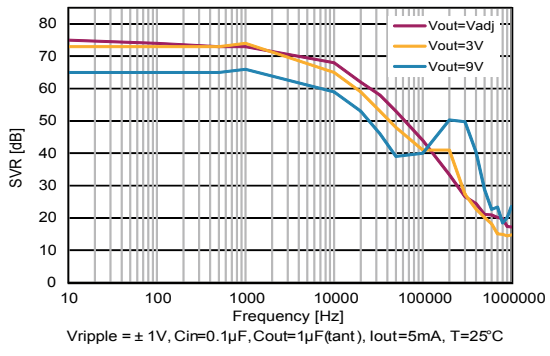
**Figure 33. Dropout voltage vs. load current ($V_{out}$ = 9 V)**




Vout =9V, Cin=0.1 µF, Cout =1 µF(tant )

AMG081120161332MT

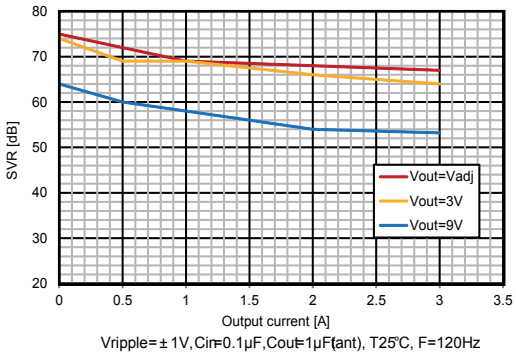
**Figure 34. SVR vs. frequency**




Vripple = ± 1V, Cin=0.1µF, Cout=1µF(tant), Iout=5mA, T=25°C

AMG081120161333MT

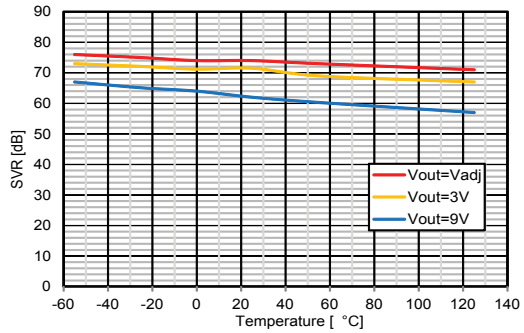
**Figure 35. SVR vs. load current**




Vripple= ± 1V, Cin=0.1µF, Cout=1µF(tant), T25°C, F=120Hz

AMG081120161334MT

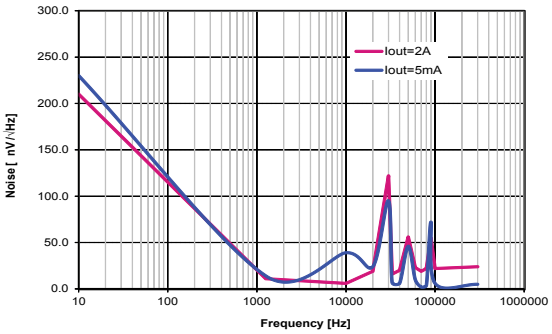
### Figure 36. SVR vs. temperature




Vripple = ±1V, Iout =5mA, Cin=0.1µF, Cout=1µF(tant ), T25°C, F=120Hz

AMG081120161335MT

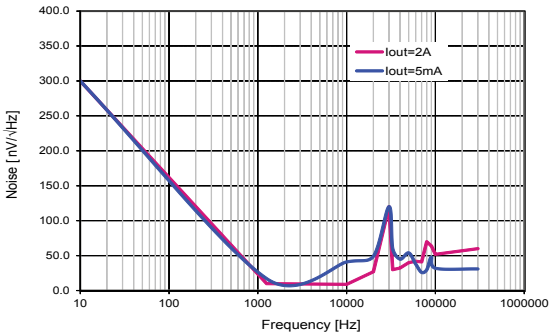
### Figure 37. Output noise spectum ($V_{out}$ = $V_{adj}$)




$V_{IN}$=3.5V, $V_{OUT}$ =$V_{ADJ}$, $C_{IN}$=220µF, $C_{OUT}$=220µF tantalum+0.47µF ceramic

AMG081120161336MT

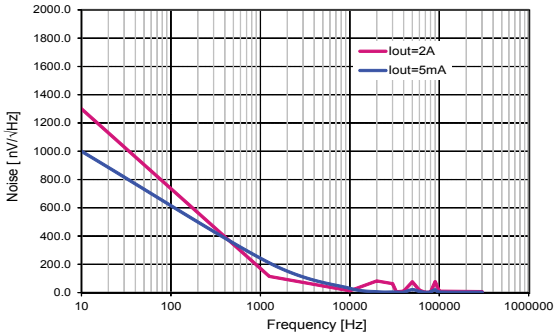
### Figure 38. Output noise spectum ($V_{out}$ = $V_{adj}$, $C_{out}$ = 1 µF)




$V_{IN}$=3.5V, $V_{OUT}$=$V_{ADJ}$, $C_{IN}$=220µF, $C_{OUT}$=1µF tantalum

AMG081120161337MT

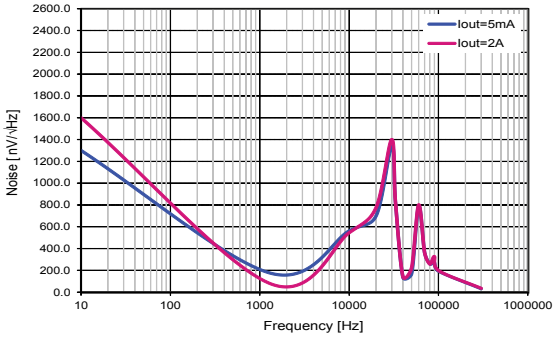
### Figure 39. Output noise spectum ($V_{out}$ = 9 V)




$V_{IN}$=11.5V , $V_{OUT}$=9V, $C_{IN}$=220µF, $C_{OUT}$=220µF tantalum+0.47µF ceramic

AMG081120161338MT

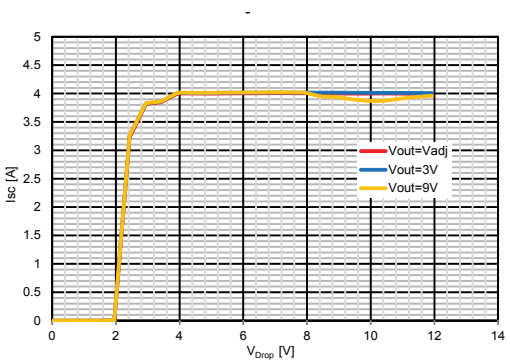
### Figure 40. Output noise spectum ($V_{out}$ = 9 V, $C_{out}$ = 1 µF)




$V_{IN}$=11.5V , $V_{OUT}$=9V, $C_{IN}$=220µF, $C_{OUT}$=1µF tantalum

AMG081120161339MT

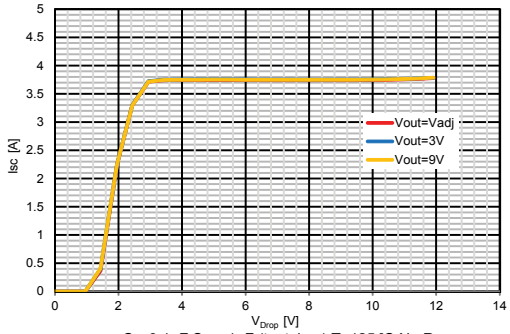
### Figure 41. Short circuit current vs. dropout voltage (T = 25 °C)




$C_{IN}$=0.1µF,$C_{OUT}$=1µF (tantalum),T=25°C,No $R_{SH}$

AMG081120161340MT

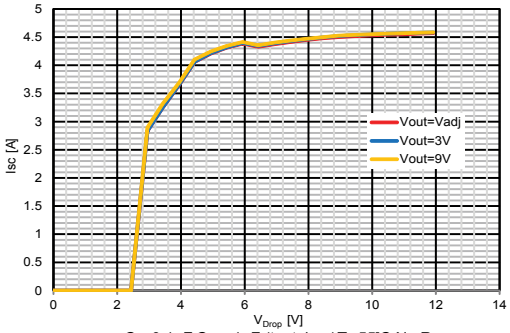
**Figure 42. Short circuit current vs. dropout voltage (T = 125 °C)**




$C_{IN}$=0.1µF $C_{OUT}$=1µF (tantalum),T=125 °C,No $R_{SH}$

AMG081120161341MT

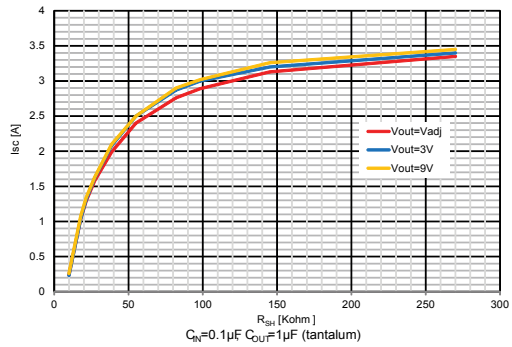
**Figure 43. Short circuit current vs. dropout voltage (T = -55 °C)**




$C_{IN}$=0.1µF $C_{OUT}$=1µF (tantalum),T=55°C,No $R_{SH}$

AMG081120161342MT

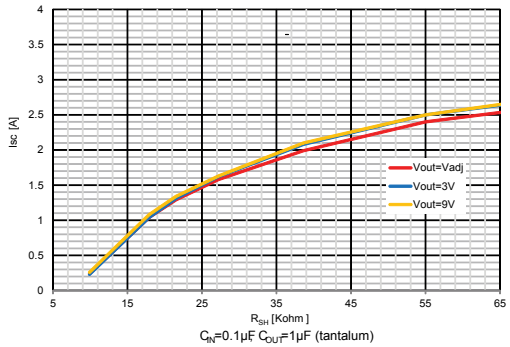
**Figure 44. Short circuit current vs. $R_{SH}$**




$C_{IN}$=0.1µF $C_{OUT}$=1µF (tantalum)

AMG081120161343MT

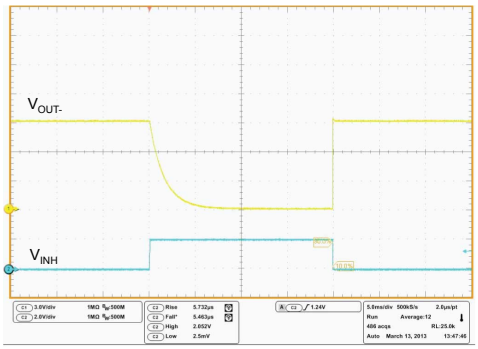
**Figure 45. Short circuit current vs. $R_{SH}$ (zoom)**




$C_{IN}$=0.1µF $C_{OUT}$=1µF (tantalum)

AMG081120161344MT

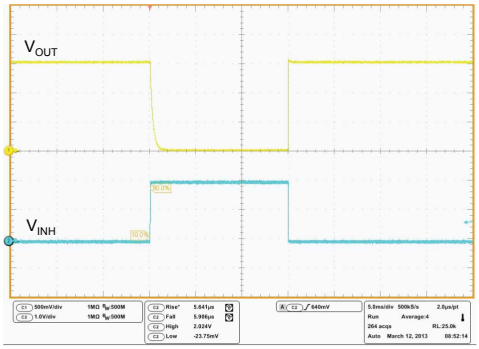
**Figure 46. Enable turn-on/off ($V_{out}$ = 9 V)**




$V_{IN}$=12V; $V_{INH}$ from 0V to 2V; $V_{OUT}$= 9V; $I_{OUT}$=5mA
$C_{IN}$=$C_{OUT}$=1µF; $T_r$=$T_f$=5µs

AMG081120161345MT

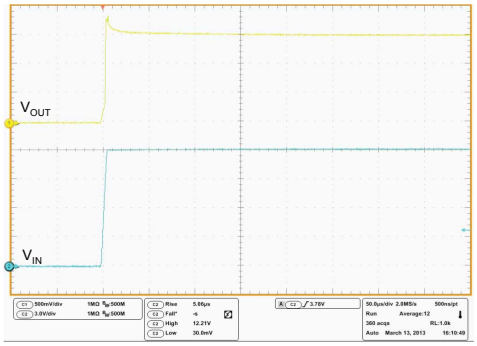
**Figure 47. Enable turn-on/off ($V_{out}$ = 1.5 V)**




$V_{IN}$=4V; $V_{INH}$ from 0V to 2V; $V_{OUT}$= 1.5V; $I_{OUT}$=5mA
$C_{IN}$=$C_{OUT}$=1µF; $T_r$=$T_f$=5µs

AMG081120161346MT

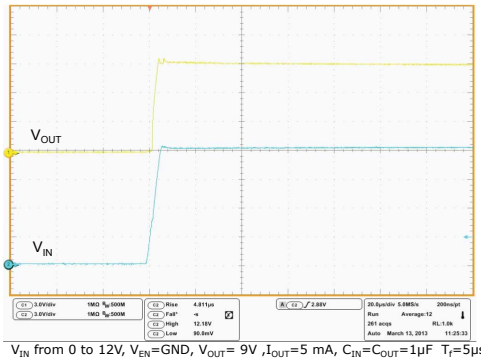
### Figure 48. Turn-on time ($V_{out}$ = 1.5 V)




$V_{IN}$ from 0 to 12V, $V_{EN}$=GND, $V_{OUT}$= 1.5V ,$I_{OUT}$=5 mA, $C_{IN}$=$C_{OUT}$=1µF $T_f$=5µs

AMG081120161347MT

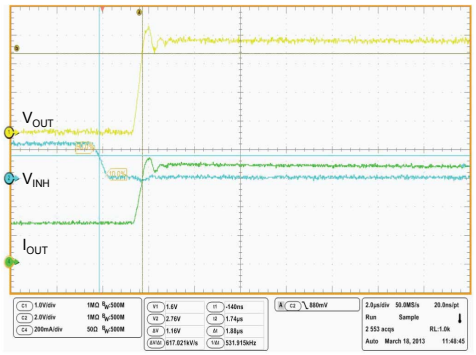
### Figure 49. Turn-on time ($V_{out}$ = 9 V)




$V_{IN}$ from 0 to 12V, $V_{EN}$=GND, $V_{OUT}$= 9V ,$I_{OUT}$=5 mA, $C_{IN}$=$C_{OUT}$=1µF $T_f$=5µs

AMG081120161348MT

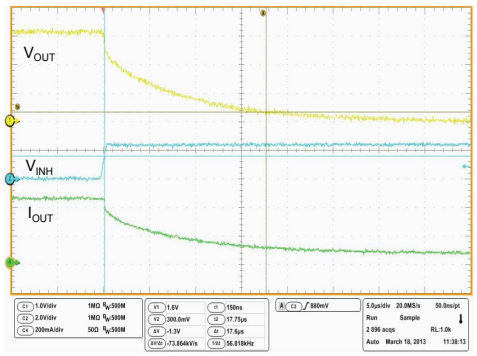
### Figure 50. Inhibit propagation delay (Lo-Hi)




$V_{IN}$=5.5V, $V_{INH}$=from 2.4V to 0V, $I_{OUT}$=400mA,$V_{OUT}$=3V,$C_{IN}$=$C_{OUT}$=1µF, $T_f$=0.5µs

AMG081120161349MT

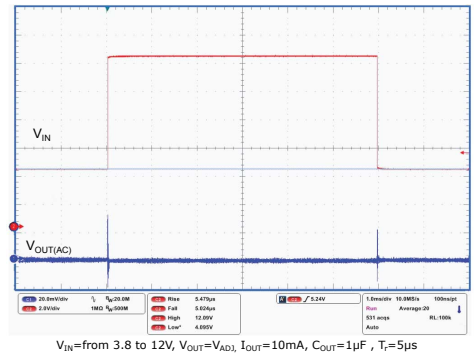
### Figure 51. Inhibit propagation delay (Hi-Lo)




$V_{IN}$=5.5V, $V_{INH}$=from 0V to 2.4V, $I_{OUT}$=400mA,$V_{OUT}$=3V,$C_{IN}$=$C_{OUT}$=1µF, $T_r$=0.5µs

AMG081120161350MT

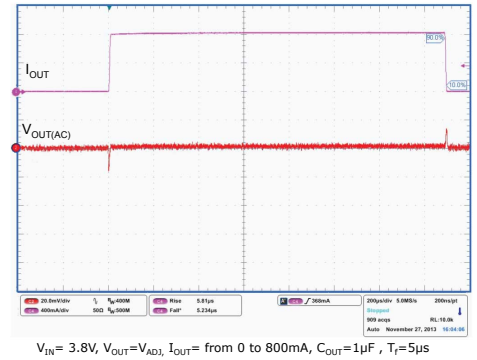
### Figure 52. Line transient




$V_{IN}$=from 3.8 to 12V, $V_{OUT}$=$V_{ADJ}$, $I_{OUT}$=10mA, $C_{OUT}$=1µF , $T_r$=5µs

AMG081120161351MT

### Figure 53. Load transient




$V_{IN}$= 3.8V, $V_{OUT}$=$V_{ADJ}$, $I_{OUT}$= from 0 to 800mA, $C_{OUT}$=1µF , $T_f$=5µs

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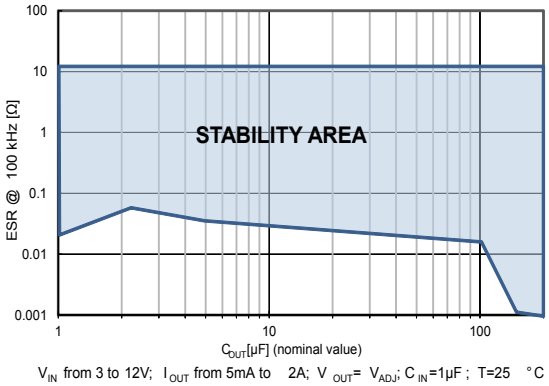
Figure 54. **Stability plan ($V_{out}$ = $V_{adj}$)**




$V_{IN}$ from 3 to 12V; $I_{OUT}$ from 5mA to 2A; $V_{OUT}$= $V_{ADJ}$; $C_{IN}$=1µF ; T=25 °C

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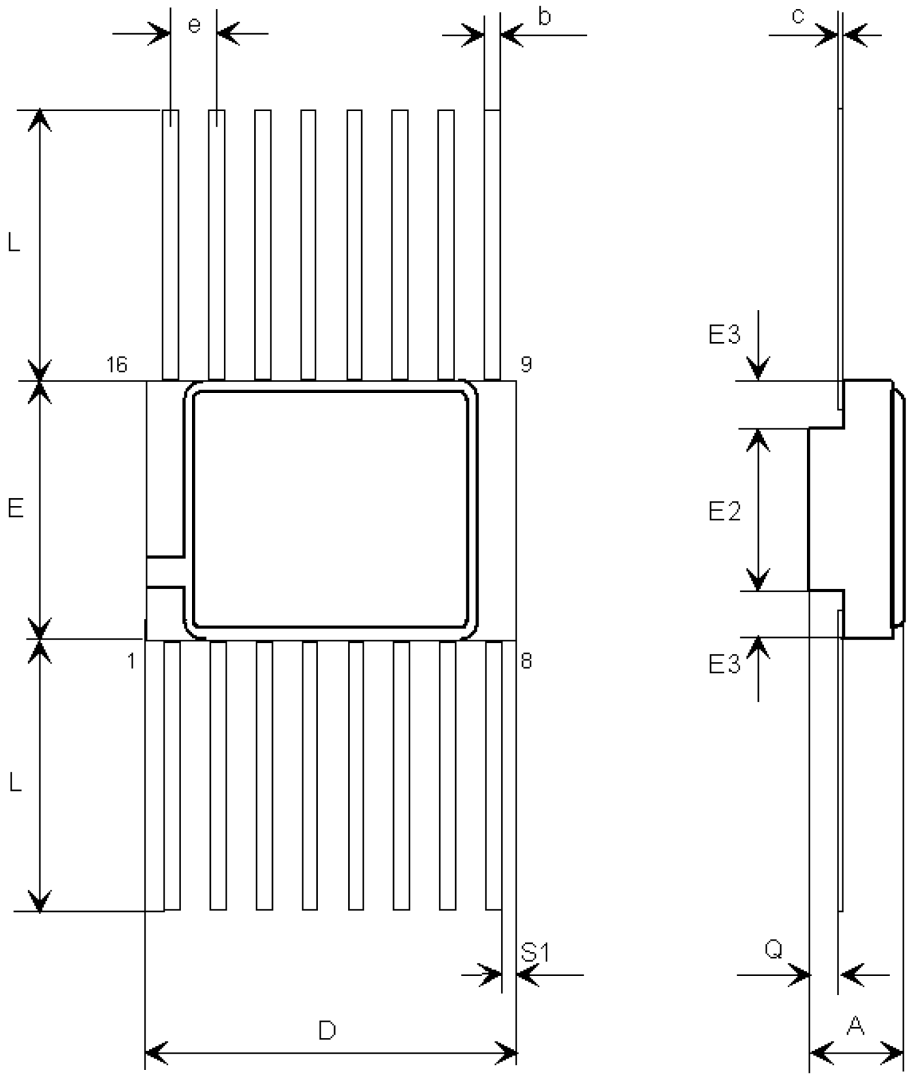
# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 8.1 Flat-16 package information

**Figure 55. FLAT-16 package outline**




7450901_D

Table 5. **FLAT-16 package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.42 | | 2.88 |
| b | 0.38 | | 0.48 |
| c | 0.10 | | 0.18 |
| D | 9.71 | | 10.11 |
| E | 6.71 | | 7.11 |
| E2 | 3.30 | 3.45 | 3.60 |
| E3 | 0.76 | | |
| e | | 1.27 | |
| L | 6.35 | | 7.36 |
| Q | 0.66 | | 1.14 |
| S1 | 0.13 | | |

## 8.2

Figure 56. **SMD5C package outline**

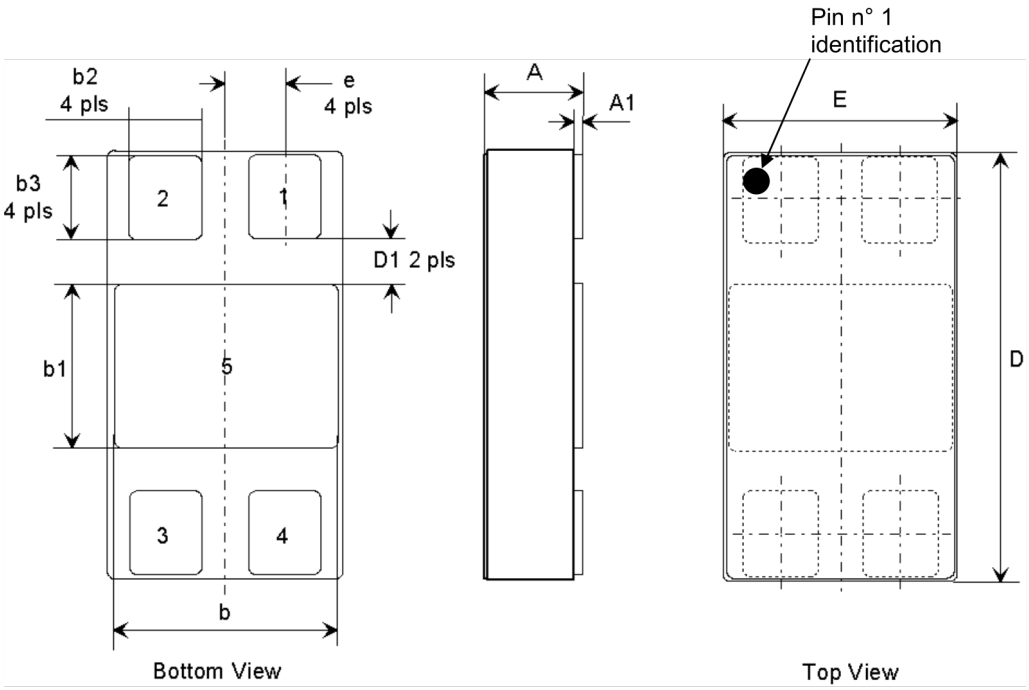



Table 6. **SMD5C package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.99 | 3.15 | 3.30 |
| A1 | 0.25 | 0.38 | 0.51 |
| b | 7.13 | 7.26 | 7.39 |
| b1 | 4.95 | 5.08 | 5.21 |
| b2 | 2.28 | 2.41 | 2.54 |
| b3 | 2.92 | 3.05 | 3.18 |
| D | 13.71 | 13.84 | 13.97 |
| D1 | 0.76 | | |
| E | 7.39 | 7.52 | 7.65 |
| e | | 1.91 | |

# 9 Ordering information

**Table 7. Device summary**

| Order code | Generic SMD (1) | Quality | Package | Lead finish | Vin range | Iout (max) | Temperature range |
|---|---|---|---|---|---|---|---|
| RHFL4913SCA1 | 5962F02524 | Engineering model | SMD5C | Gold | 3 to 12 Volt | 3.0 | -55 to 150 °C |
| RHFL4913SCA07V | | Flight model | | | | | |
| RHFL4913KPA1 | | Engineering model | Flat-16P | Gold | | 2.0 | |
| RHFL4913KPA-01V | | Flight model | | | | | |
| RHFL4913KPA-02V | | Flight model | | Solder Dip | | | |

1. *Standard microcircuit drawing*

**Table 8. Ordering information**

| Order code (1) | SMD pin | Quality level | Package | Lead finish | Marking (2) | Mass | Packing |
|---|---|---|---|---|---|---|---|
| RHFL4913SCA1 | - | Engineering Model | SMD5C | Gold | RHFL4913SCA1 | 2.5 g | Strip pack |
| RHFL4913KPA1 | 5962F0252403VUC | QML-V | | | 5962F0252403VUC | | |
| RHFL4913KPA1 | - | Engineering Model | Flat-16P | Gold | RHFL4913KPA1 | 0.6 g | |
| RHFL4913KPA-01V | 5962F0252401VXC | QML-V | | | 5962F0252401VXC | | |
| RHFL4913KPA-02V | 5962F0252401VXA | QML-V | | Solder Dip | 5962F0252401VXA | | |

1. *Contact ST sales office for information about the specific conditions for:*
   - *Products in die form*
   - *Other quality levels*
   - *Tape and reel packing*
2. *Specific marking only. The full marking includes in addition:*
   - *For the engineering models : ST logo, date code, country of origin (FR)*
   - *For ESCC flight parts : ST logo, date code, country of origin (FR), manufacturer code (CSTM), serial number of the part within the assembly lot*

**Table 9. Environmental characteristics**

| Parameter | Conditions | Value | Unit |
|---|---|---|---|
| Output voltage thermal drift | -55°C to +125°C | 40 | ppm/°C |
| Output voltage radiation drift | From 0 krad to 300 krad at 0.55 rad/s | 8 | ppm/krad |
| Output voltage radiation drift | From 0 krad to 300 krad, Mil Std 883E Method 1019.6 | 6 | ppm/krad |

## Revision history

Table 10. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 29-Oct-2004 | 3 | New order codes added - Tables 4 and 5. |
| 27-May-2005 | 4 | Features, Tables 4, 5 and the Figure 1 has been updated. Add the Mechanical Data SOC-16. |
| 08-Jun-2005 | 5 | Mistake on Table 4 (Q.ty Level), Table 7 has been updated and add DIE Information. |
| 30-Jan-2006 | 6 | Added new package SMD5C and removed old package SOC-16. |
| 26-Jan-2007 | 7 | DIE Information and DIE Pad has been updated par. 6, pages 9 and 10. |
| 23-Nov-2007 | 8 | Pin information for the SMD5C package updated in Table 1; added section 6.3: FPGA power supply lines on page 10. Minor text changes. |
| 22-Sep-2008 | 9 | Modified Application information on page 9. |
| 17-Nov-2008 | 10 | Modified Table 8 on page 26. |
| 21-Jan-2010 | 11 | Modified Table 7 on page 26. |
| 18-Oct-2010 | 12 | Modified Section 6.2 on page 9. |
| 07-Feb-2011 | 13 | Added: note Table 1 on page 3. |
| 07-Dec-2011 | 14 | Removed the note under Table 1 on page 3 and added footnotes 1 and 2. |
| 20-Aug-2012 | 15 | Order code updated in Table 7 on page 26 about the SMD5C package |
| 15-Jan-2014 | 16 | Updated Features in cover page.<br>Added Section 7: Typical characteristics.<br>Modified Table 4: Electrical characteristics.<br>Updated Section 9: Package mechanical data and Section 10: Ordering information.<br>Minor text changes. |
| 05-May-2014 | 17 | Updated Figure 18: Output voltage vs input voltage ($I_{out}$=3 A, T=25 °C and T=125 °C).<br>Minor text changes. |
| 22-Nov-2016 | 18 | Updated description in cover page.<br>Updated Section 9: "Package information".<br>Minor text changes. |
| 30-Mar-2018 | 19 | Updated:<br>- Figure 5. Baseline bias configuration with remote feedback and Figure 6. Local feedback configuration.<br>- Section 6.4 Notes on the 16-pin hermetic package.<br>- Section 9 Ordering information. |
| 27-Apr-2018 | 20 | Updated: Section 3 Maximum ratings. |
| 08-Feb-2019 | 21 | Minor text change in Description on the cover page. |

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