LogiCORE IP LTE DL Channel Encoder v2.1

XMP023 January 18, 2012 **Product Brief**

Introduction

The Xilinx® LogiCORE™ IP LTE DL Channel Encoder core provides designers with an LTE Downlink Channel Encoding block for the *3GPP TS 36.212 v9.0.0 Multiplexing and Channel Coding* specification.

Features

- Channel coding for 3GPP TS 36.212 supports: DL-SCH, PCH, MCH, BCH, CFI, HI, and DCI
- Bit-accurate C model available
- Fully optimized for speed and area
- Fully synchronous design using a single clock
- For use with the Xilinx CORE Generator™ software v13.4

LogiCORE IP Facts Table	
Core Specifics	
Supported Device Family(1)	Virtex®-7, Kintex™-7, Artix™-7, Zynq™-7000, Virtex-6, Virtex-5, Spartan®-6
Supported User Interfaces	Not Supported(2)
Provided with Core	
Documentation	Product Specification Product Brief C-Model User Guide
Design Files	Netlist
Example Design	Not Provided
Test Bench	VHDL
Constraints File	Not Provided
Simulation Model	Verilog, VHDL and UNISIM
Supported S/W Driver(3)	N/A
Tested Design Tools	
Design Entry Tools	CORE Generator tool 13.4
Simulation(4)	Mentor Graphics ModelSim Cadence Incisive Enterprise Simulator (IES) ISE Simulator
Synthesis Tools	Not Provided.
Support	
Provided by Xilinx, Inc.	

1. For a complete listing of supported devices, see the release notes for this core.
2. Interface similar to AXI and can be connected to an AXI4- Stream Interface.
3. Standalone driver details can be found in the EDK or SDK directory (*<install_directory>*/doc/usenglish/xilinx_drivers.htm). Linux OS and driver support information is available from http://wiki.xilinx.com.
4. For the supported version of the tools, see the ISE Design Suite 13: Release Notes Guide

Overview

The LTE DL Channel Encoder core provides a channel encoding solution for the 3GPP 36.212 specification. Figure 1 and Figure 2 illustrate the main blocks in the LTE encoding chain for the two main channel types that are supported by the core. The architecture has been designed to provide efficient use of the FPGA while also offering a low bandwidth processor interface to reduce system-level overhead. Timing-critical operations are performed by the FPGA.

The interface to the core can be attached to any bus-based system. The memory-mapped interface allows for simple integration and validation within the system.

Data is processed sequentially on a transport block basis for each of the two main channel types, where the term "transport block" is used to describe a block of data originating from the MAC layer. Specific processing is applied depending on the type of input block, which is indicated as part of the control signaling provided by the MAC layer.

The following functions are supported by the core:

- CRC
  - 24-bit CRC applied to DL-SCH, PCH, and MCH transport blocks
  - 16-bit CRC applied to BCH and DCI code blocks (with additional scrambling on parity bits)
- Segmentation
  - Code block segmentation applied to DL-SCH, PCH, and MCH transport blocks (that is, data that are turbo encoded), with an additional 24-bit CRC computed on each code block (in cases where segmentation produces more than one code block)
- Encoding
  - Turbo code applied to DL-SCH, PCH, and MCH data
  - Convolutional code applied to BCH and DCI data (single code block)
- Rate Matching
  - Applied on a code block basis to DL-SCH, PCH, MCH, BCH, and DCI data. This function performs appropriate puncturing according to the AMC parameters and redundancy version.
  - Data output on a code block basis for the DL-SCH, PCH, and MCH channels.
- Control Format Indicator Generation
  - The HI or CFI coded outputs are generated according to the type indicated from the control signaling from the MAC layer.

Control and Broadcast Channel Processing

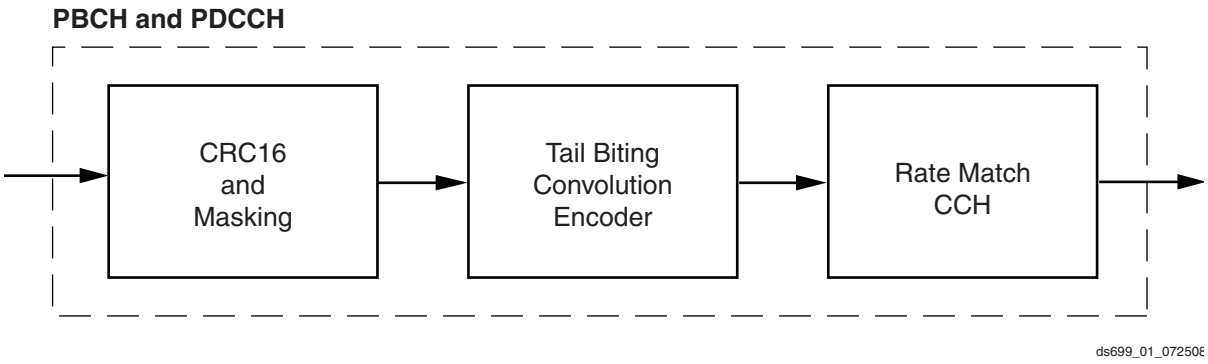

Figure 1: **Downlink Channel Processing for BCH and DCI -CCH Channel Stream**

Shared, Paging, and Multicast Channel Processing

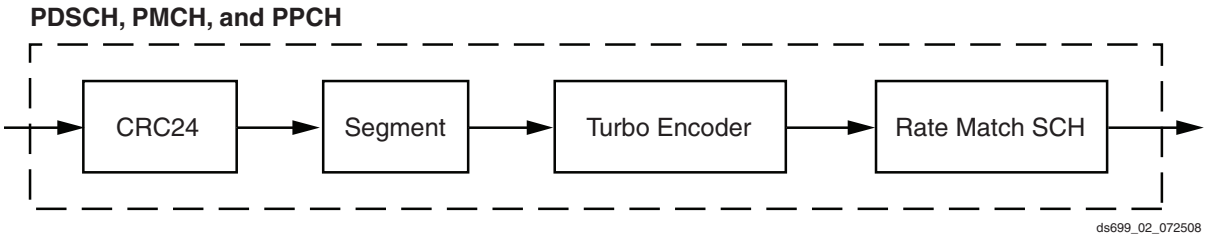

Figure 2: **Downlink Channel Processing for DL-SCH, PCH and MCH -SCH Channel Stream**

Additional Documentation and Supporting Materials

A full data sheet and additional supporting materials (C models and accompanying user guide documentation) are available for this core. Access to this material may be requested by clicking on this registration link: www.xilinx.com/member/lte_dl_channel_enc_eval/index.htm.

Support

Xilinx provides technical support at www.xilinx.com/support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

See the IP Release Notes Guide (XTP025) for further information on this core. There is a link to all the DSP IP and then to the relevant core.

For each core, there is a master Answer Record that contains the Release Notes and Known Issues list for the core being used. The following information is listed for each version of the core:

- New Features
- Bug Fixes
- Known Issues

Ordering Information

The LTE DL Channel Encoder core is provided under the SignOnce IP Site License and can be generated using the Xilinx CORE Generator v13.4. The CORE Generator software is shipped with Xilinx ISE Design Suite development software.

To access the full functionality of the core, including simulation and FPGA bitstream generation, a full license must be obtained from Xilinx. For more information, visit the LTE DL Channel Encoder product page.

Contact your local Xilinx sales representative for pricing and availability of additional Xilinx LogiCORE modules and software. Information about additional Xilinx LogiCORE modules is available on the Xilinx IP Center.

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Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/19/08	1.0	Xilinx initial release.
04/24/09	2.0	Virtex-6 and Spartan-6 support added. Addition of Transport block start and end signals. Modification to CRC output to support v8.5 of RNTI scrambling.
04/19/10	3.0	Added support for latest Spartan-6 and Virtex-6 device variants.
06/22/11	3.1	Added support for 7 Series devices and ISE Design Suite 13.2.
08/15/11	3.2	Updated to include web registration information.
01/18/12	3.3	Updated for ISE Release 13.4.

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