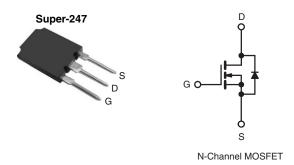
Vishay Siliconix

D Series Power MOSFET

| PRODUCT SUMMARY | | | | | |
|--|------------------------|-------|--|--|--|
| V _{DS} (V) at T _J max. | 550 | | | | |
| R _{DS(on)} max. at 25 °C (Ω) | V _{GS} = 10 V | 0.130 | | | |
| Q _g max. (nC) | 125 | | | | |
| Q _{gs} (nC) | 23 | | | | |
| Q _{gd} (nC) | 37 | | | | |
| Configuration | Single | | | | |



FEATURES

- Optimal Design
 - Low Area specific On-Resistance
 - Low Input Capacitance (Ciss)
 - Reduced Capacitive Switching Losses
 - High Body Diode Ruggedness
 - Avalanche Energy Rated (UIS)
- · Optimal Efficiency and Operation
 - Low Cost
 - Simple Gate Drive Circuitry
 - Low Figure-Of-Merit (FOM): Ron x Qa
 - Fast Switching
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

APPLICATIONS

- Consumer Electronics
 - Displays (LCD or Plasma TV
- Server and Telecom Power Supplies
 - SMPS
- Industrial
 - Welding, Induction Heating, Motor Drives
- · Battery Chargers

| ORDERING INFORMATION | | | | |
|----------------------|---------------|--|--|--|
| Package | Super-247 | | | |
| Lead (Pb)-free | SiHS36N50D-E3 | | | |

| PARAMETER | | | SYMBOL | LIMIT | UNIT | |
|---|---|---|-----------------------------------|---------------|---------|--|
| Drain-Source Voltage | | | V _{DS} | 500 | | |
| Gate-Source Voltage | | | | ± 30 | V | |
| Gate-Source Voltage AC (f > 1 Hz) | | | V_{GS} | 30 | | |
| Continuous Drain Current /T 150 °C\ | V _{GS} at 10 V | T _C = 25 °C T _C = 100 °C | | 36 | | |
| Continuous Drain Current (T _J = 150 °C) | V _{GS} at 10 V | T _C = 100 °C | l _D | 23 | Α | |
| Pulsed Drain Current ^a | | | I _{DM} | 112 | | |
| Linear Derating Factor | | | | 3.6 | W/°C | |
| Single Pulse Avalanche Energy ^b | | | E _{AS} | 332 | mJ | |
| Maximum Power Dissipation | P_{D} | 446 | W | | | |
| Operating Junction and Storage Temperature Range | | | T _J , T _{stg} | - 55 to + 150 | °C | |
| Drain-Source Voltage Slope | in-Source Voltage Slope T _J = 125 °C | | dV/dt | 24 | V/ns | |
| Reverse Diode dV/dt ^d | | | uv/ul | 0.1 | 7 V/ris | |
| Soldering Recommendations (Peak Temperature) for 10 s | | | | 300° | °C | |

- a. Repetitive rating; pulse width limited by maximum junction temperature. b. $V_{DD}=50~V$, starting $T_J=25~^{\circ}C$, L=2.3~mH, $R_g=25~\Omega$, $I_{AS}=17~A$.
- c. 1.6 mm from case.
- d. $I_{SD} \le I_D$, starting $T_J = 25$ °C.



Vishay Siliconix

| THERMAL RESISTANCE RATINGS | | | | | |
|----------------------------------|-------------------|------|------|------|--|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT | |
| Maximum Junction-to-Ambient | R _{thJA} | - | 40 | °C/W | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.28 | C/VV | |

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|--|-----------------------|---|---|------|-------|-------|------|
| Static | | | | | • | | |
| Drain-Source Breakdown Voltage | V _{DS} | V _{GS} : | = 0 V, I _D = 250 μA | 500 | - | - | V |
| V _{DS} Temperature Coefficient | $\Delta V_{DS}/T_{J}$ | Reference | to 25 °C, I _D = 250 μA | - | 0.52 | - | V/°C |
| Gate Threshold Voltage (N) | V _{GS(th)} | V _{DS} = | = V _{GS} , I _D = 250 μA | 3.0 | - | 5.0 | V |
| Gate-Source Leakage | I _{GSS} | | V _{GS} = ± 30 V | - | - | ± 100 | nA |
| - | | V _{DS} = | $V_{DS} = 500 \text{ V}, V_{GS} = 0 \text{ V}$ | | - | 1 | |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 400 \ | /, V _{GS} = 0 V, T _J = 125 °C | - | - | 10 | μA |
| Drain-Source On-State Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 18 A | - | 0.105 | 0.130 | Ω |
| Forward Transconductancea | 9 _{fs} | | = 50 V, I _D = 18 A | - | 12.8 | _ | S |
| Dynamic | | | | | | l | |
| Input Capacitance | C _{iss} | T | V _{GS} = 0 V, | - | 3233 | _ | |
| Output Capacitance | C _{oss} | 1 | $V_{DS} = 100 \text{ V},$ | - | 285 | - | - |
| Reverse Transfer Capacitance | C _{rss} | f = 1 MHz | | - | 25 | - | |
| Effective Output Capacitance, Energy Related ^a | C _{o(er)} | V _{GS} = 0 V, V _{DS} = 0 V to 400 V | | - | 240 | - | pF |
| Effective Output Capacitance, Time Related ^b | C _{o(tr)} | | | - | 352 | - | 1 |
| Total Gate Charge | Qg | | | - | 83 | 125 | |
| Gate-Source Charge | Q _{gs} | V _{GS} = 10 V | | - | 23 | - | nC |
| Gate-Drain Charge | Q _{gd} | | | - | 37 | - | |
| Turn-On Delay Time | t _{d(on)} | | | - | 33 | 66 | |
| Rise Time | t _r | $V_{DD} = 400 \text{ V}, I_{D} = 18 \text{ A}, V_{GS} = 10 \text{ V}, R_{g} = 9.1 \Omega$ | | 1 | 89 | 134 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 79 | 119 | |
| Fall Time | t _f | | | - | 68 | 102 | |
| Gate Input Resistance | R_g | f = 1 MHz, open drain | | - | 1.8 | - | Ω |
| Drain-Source Body Diode Characteristic | s | | | | | | |
| Continuous Source-Drain Diode Current | I _S | MOSFET symbol showing the integral reverse p - n junction diode | | - | - | 36 | |
| Pulsed Diode Forward Current | I _{SM} | | | - | - | 144 | A |
| Diode Forward Voltage | V _{SD} | T _J = 25 °C, I _S = 18 A, V _{GS} = 0 V | | - | - | 1.2 | V |
| Reverse Recovery Time | t _{rr} | 0 1 17 0 1 7 00 1 | | - | 490 | - | ns |
| Reverse Recovery Charge | Q _{rr} | | 5 °C, I _F = I _S = 18 A, | - | 8.2 | - | μC |
| Reverse Recovery Current | I _{RRM} | dl/dt = 100 A/μs, V _R = 20 V | | _ | 31 | _ | A |

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} . b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

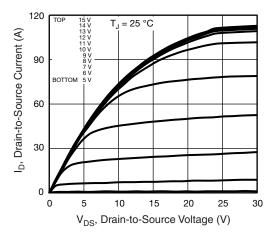


Fig. 1 - Typical Output Characteristics

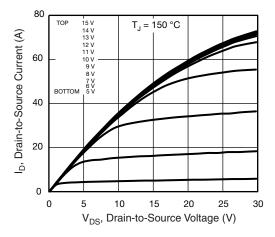


Fig. 2 - Typical Output Characteristics

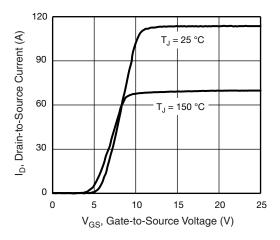


Fig. 3 - Typical Transfer Characteristics

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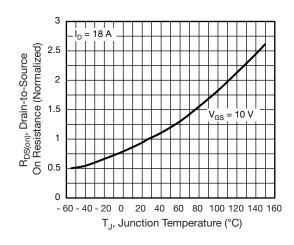


Fig. 4 - Normalized On-Resistance vs. Temperature

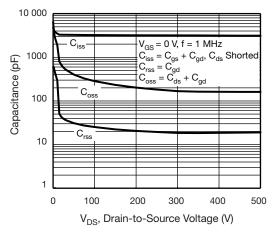


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

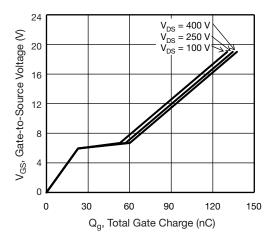


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



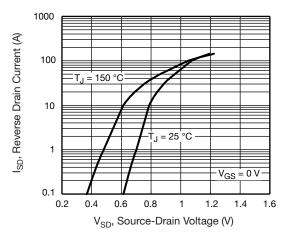


Fig. 7 - Typical Source-Drain Diode Forward Voltage

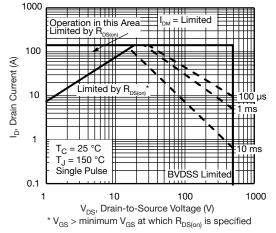


Fig. 8 - Maximum Safe Operating Area

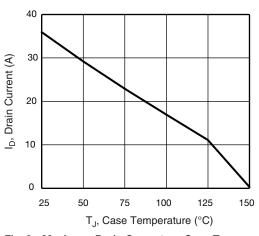


Fig. 9 - Maximum Drain Current vs. Case Temperature

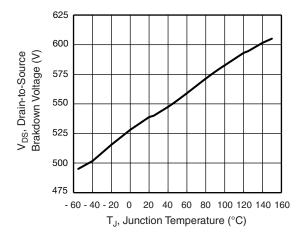


Fig. 10 - Temperature vs. Drain-to-Source Voltage

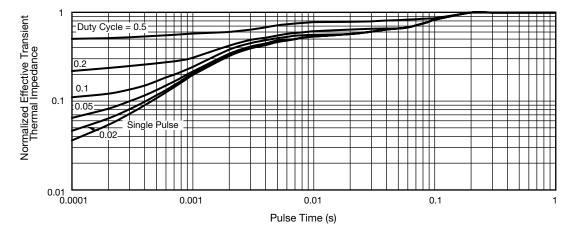


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



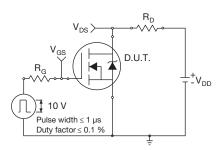


Fig. 12 - Switching Time Test Circuit

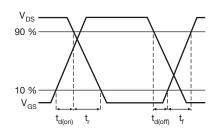


Fig. 13 - Switching Time Waveforms

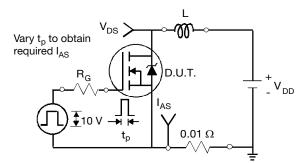


Fig. 14 - Unclamped Inductive Test Circuit

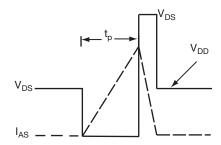


Fig. 15 - Unclamped Inductive Waveforms

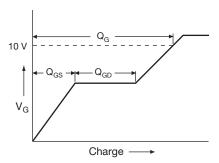


Fig. 16 - Basic Gate Charge Waveform

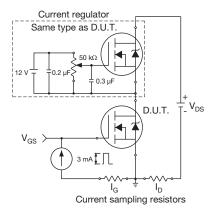
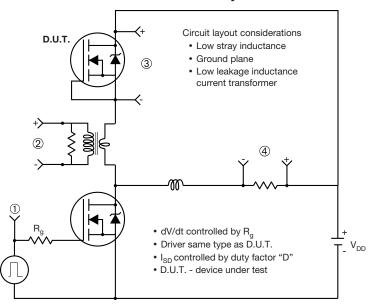


Fig. 17 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



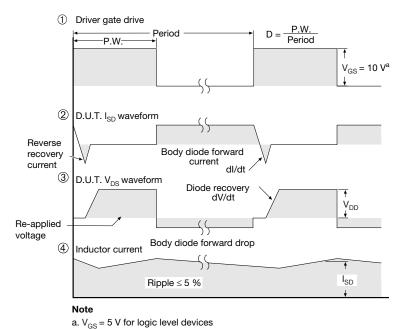
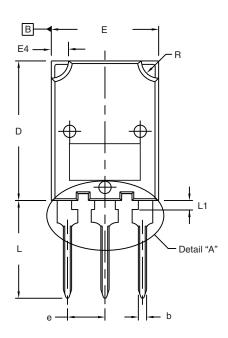


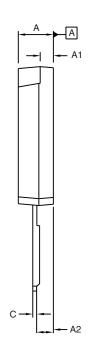
Fig. 18 - For N-Channel

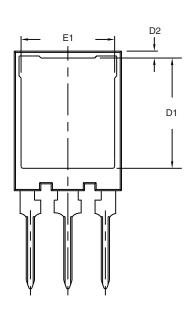
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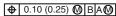
Vishay Siliconix

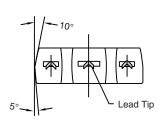
TO-274AA (High Voltage)

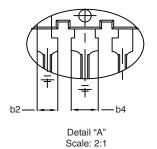












| | MILLIM | IETERS | INC | HES |
|------------------|--------|--------|-------|-------|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| Α | 4.70 | 5.30 | 0.185 | 0.209 |
| A1 | 1.50 | 2.50 | 0.059 | 0.098 |
| A2 | 2.25 | 2.65 | 0.089 | 0.104 |
| b | 1.30 | 1.60 | 0.051 | 0.063 |
| b2 | 1.80 | 2.20 | 0.071 | 0.087 |
| b4 | 3.00 | 3.25 | 0.118 | 0.128 |
| c ⁽¹⁾ | 0.38 | 0.89 | 0.015 | 0.035 |
| D | 19.80 | 20.80 | 0.780 | 0.819 |

| | MILLIM | IETERS | INC | HES |
|------|----------|--------|-----------|-------|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 15.50 | 16.10 | 0.610 | 0.634 |
| D2 | 0.70 | 1.30 | 0.028 | 0.051 |
| Е | 15.10 | 16.10 | 0.594 | 0.634 |
| E1 | 13.30 | 13.90 | 0.524 | 0.547 |
| е | 5.45 BSC | | 0.215 BSC | |
| L | 13.70 | 14.70 | 0.539 | 0.579 |
| L1 | 1.00 | 1.60 | 0.039 | 0.063 |
| R | 2.00 | 3.00 | 0.079 | 0.118 |

ECN: X17-0056-Rev. B, 27-Mar-17

DWG: 5975

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA
- (1) Dimension measured at tip of lead



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Vishay

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