



Dual N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
20	0.225 at $V_{GS} = 4.5$ V	1.5	1.1 nC
	0.270 at $V_{GS} = 2.5$ V	1.5	
	0.345 at $V_{GS} = 1.8$ V	1.5	
	0.960 at $V_{GS} = 1.5$ V	0.5	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-75 Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.75 mm Profile
- Typical ESD Protection 2800 V
- Rated ESD Protection 1400 V
- Compliant to RoHS Directive 2002/95/EC

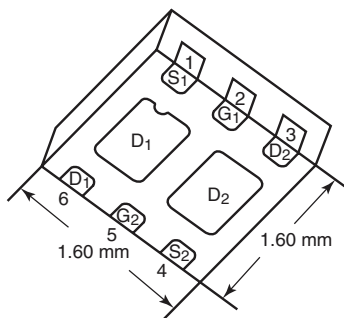


RoHS
COMPLIANT
HALOGEN
FREE

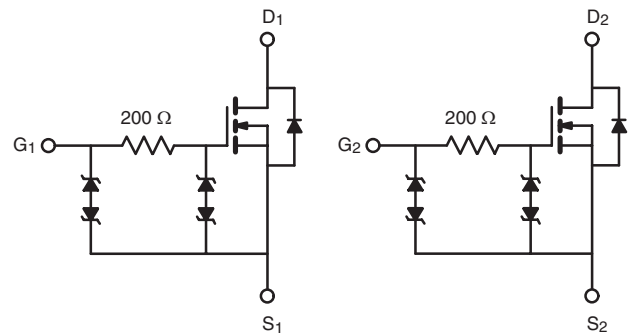
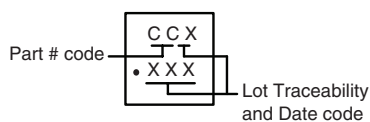
APPLICATIONS

- Load Switch for Portable Devices
- Low Voltage Load Switch

PowerPAK SC75-6L-Dual



Marking Code



Ordering Information: SiB900EDK-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 6	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	A
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	4	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
Maximum Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	W
		$T_C = 70^\circ\text{C}$	
		$T_A = 25^\circ\text{C}$	
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	90	115	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	32	40	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 125 °C/W.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

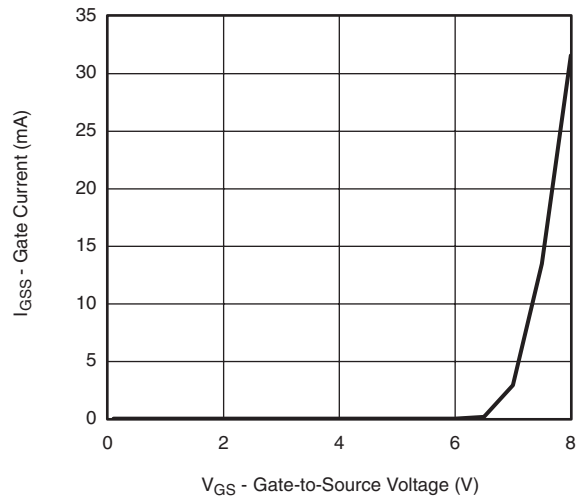
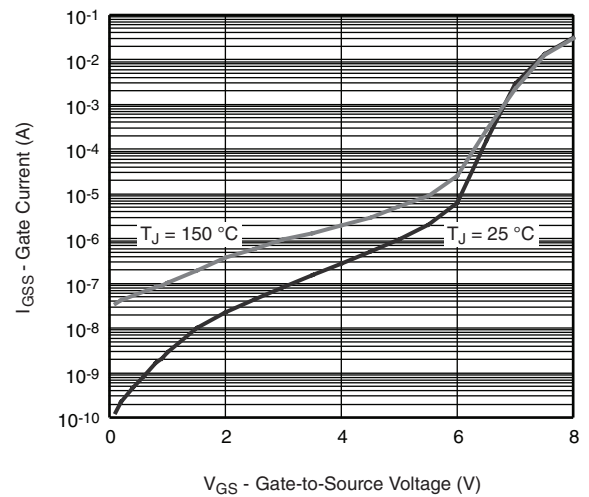
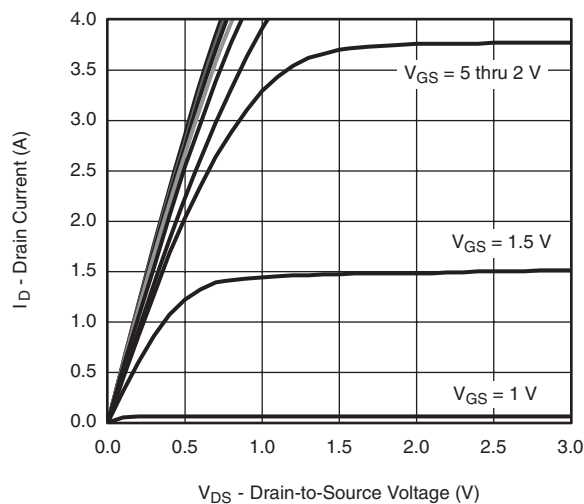
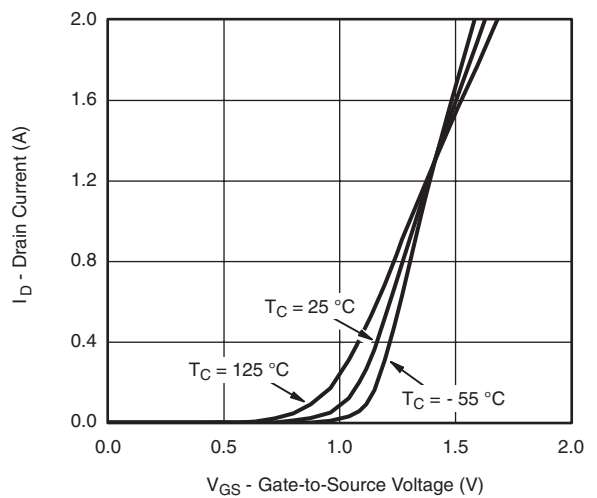
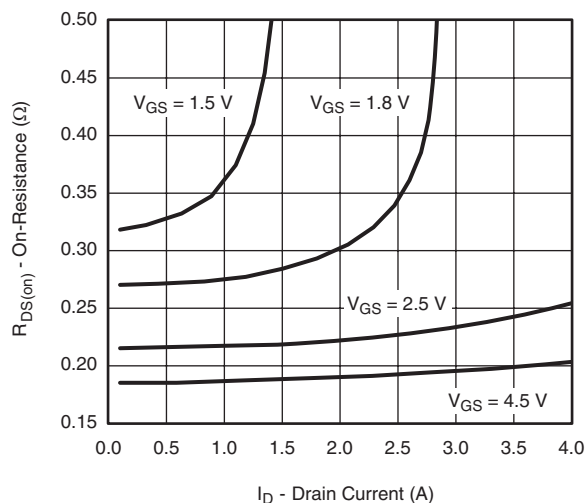
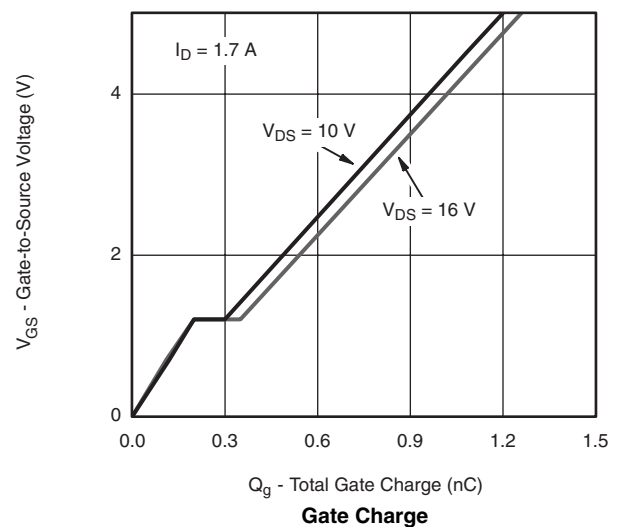
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		21		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 2.3		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.4		1.0	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 3 V			± 1	μA
		V _{DS} = 0 V, V _{GS} = ± 6 V			± 1	mA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	4			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 1.6 A		0.183	0.225	Ω
		V _{GS} = 2.5 V, I _D = 1.5 A		0.220	0.270	
		V _{GS} = 1.8 V, I _D = 1.3 A		0.275	0.345	
		V _{GS} = 1.5 V, I _D = 0.3 A		0.320	0.960	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 1.6 A		3.5		S
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 1.7 A		1.1	1.7	nC
Gate-Source Charge	Q _{gs}			0.2		
Gate-Drain Charge	Q _{gd}			0.1		
Gate Resistance	R _g	f = 1 MHz		200		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 7.7 Ω I _D ≅ 1.3 A, V _{GEN} = 4.5 V, R _g = 1 Ω		20	30	ns
Rise Time	t _r			12	20	
Turn-Off DelayTime	t _{d(off)}			70	105	
Fall Time	t _f			20	30	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			1.5	A
Pulse Diode Forward Current	I _{SM}				4	
Body Diode Voltage	V _{SD}	I _S = 1.3 A, V _{GS} = 0 V		0.9	1.2	V

Notes:

a. Pulse test; pulse width ≤ 300 μ s, duty cycle ≤ 2 %.

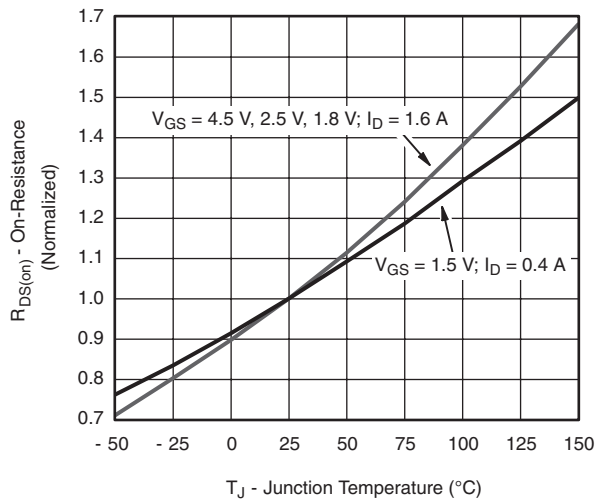
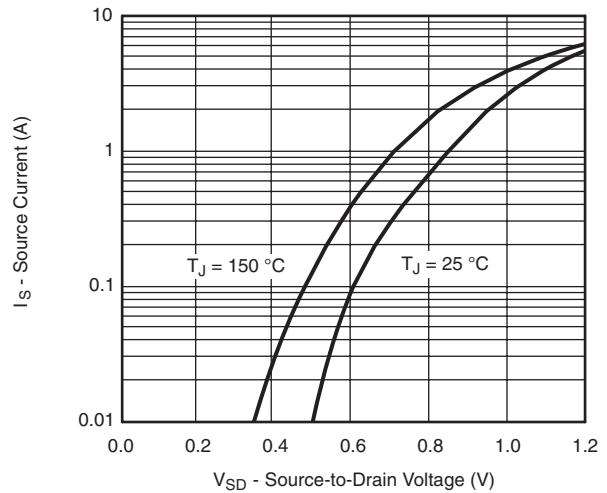
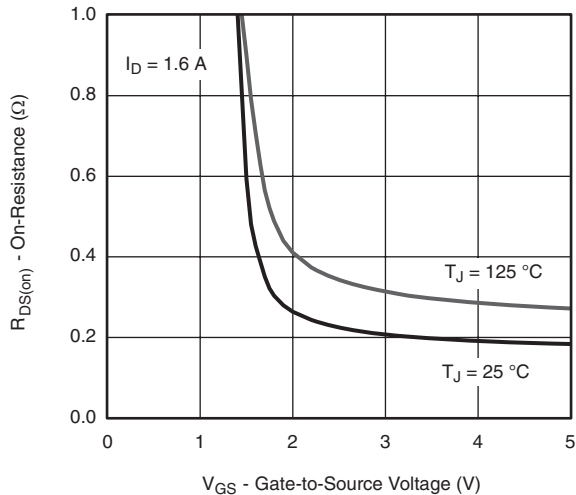
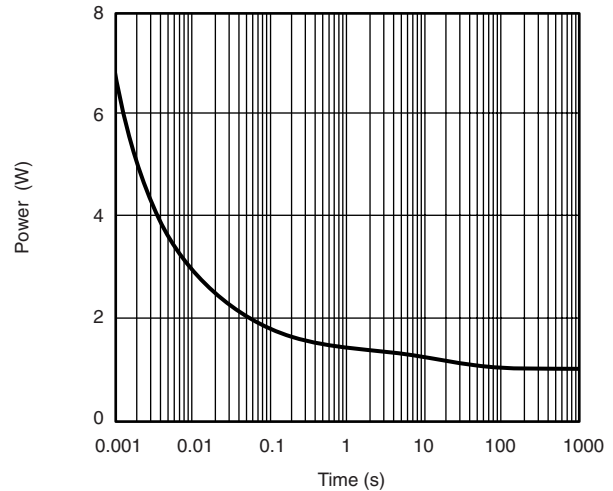
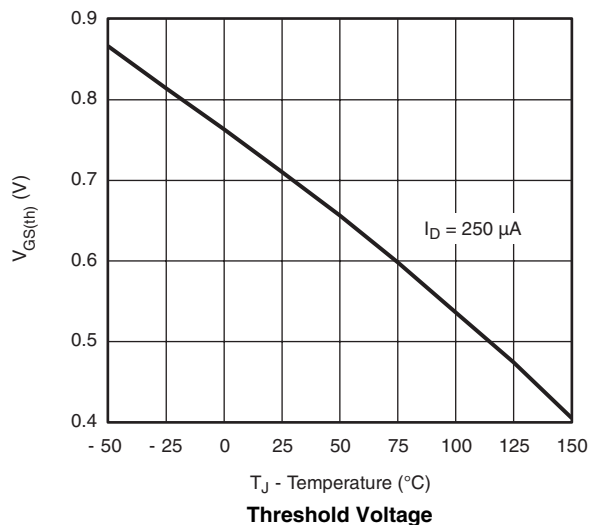
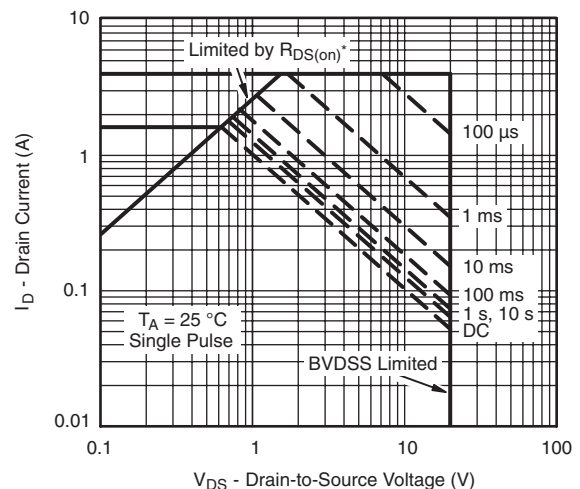
b. Guaranteed by design, not subject to production testing.

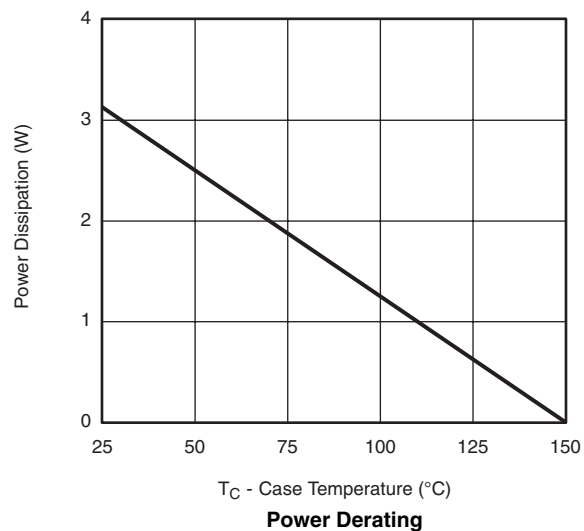
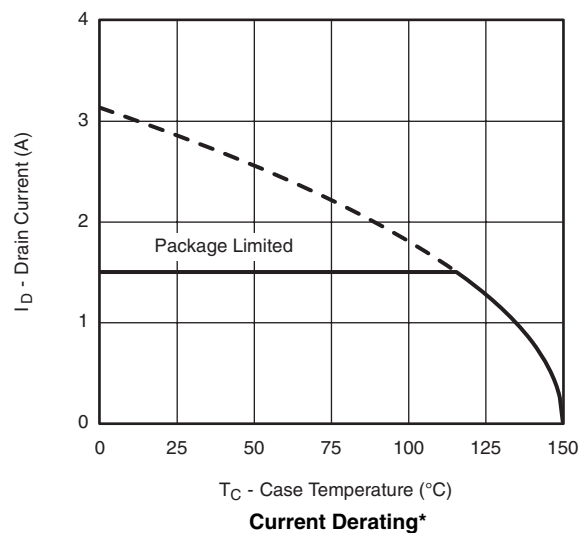
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Gate Current vs. Gate-to-Source Voltage

Gate Current vs. Gate-to-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Gate Charge

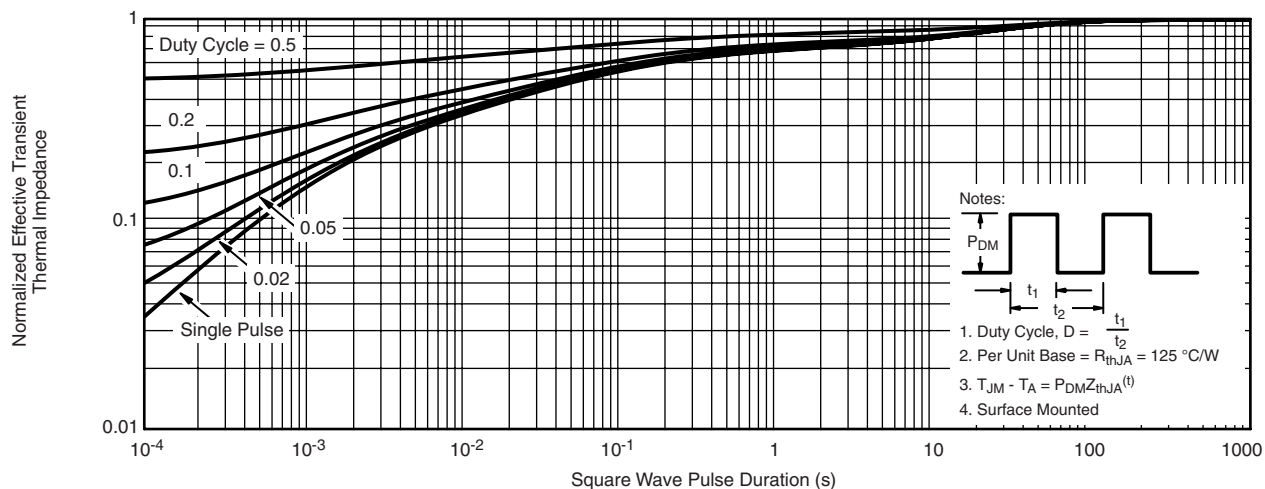
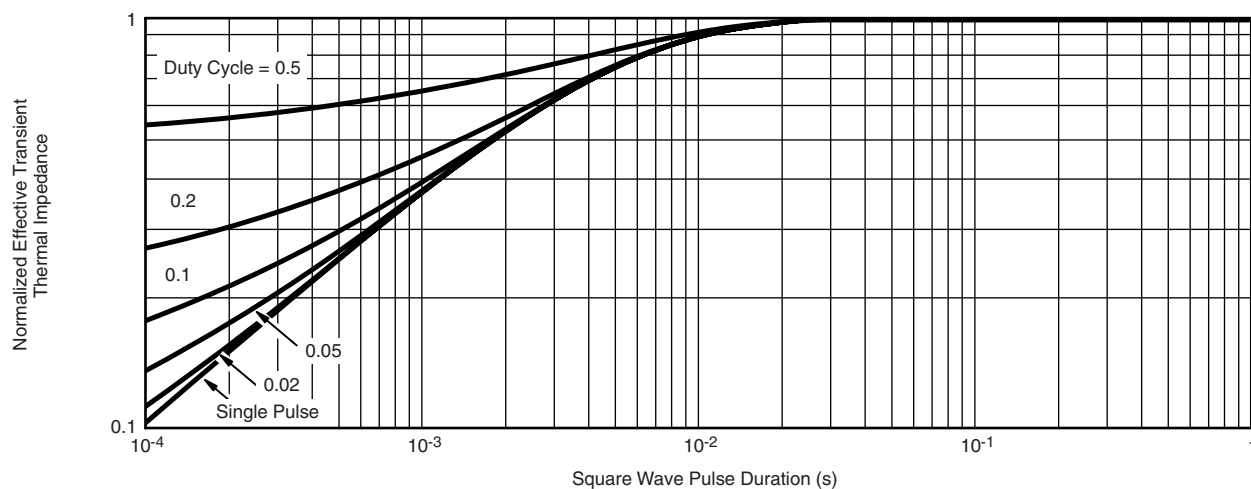
SiB900EDK

Vishay Siliconix

**TYPICAL CHARACTERISTICS** $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted**Normalized On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Single Pulse Power, Junction-to-Ambient****Threshold Voltage*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**


TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

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