

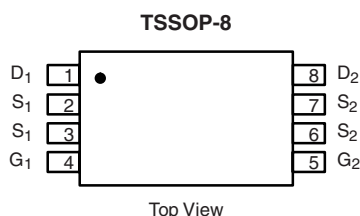
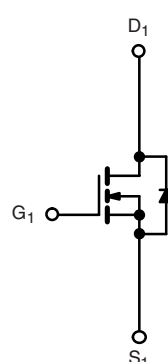
Dual N-Channel 2.5-V (G-S) MOSFET

PRODUCT SUMMARY

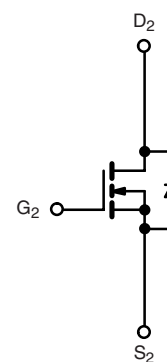
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
20	0.045 at $V_{GS} = 4.5$ V	3.9
	0.055 at $V_{GS} = 3.0$ V	3.5
	0.065 at $V_{GS} = 2.5$ V	3.0

FEATURES

- Halogen-free


RoHS
COMPLIANT

Ordering Information: Si6925ADQ-T1-GE3 (Lead (Pb)-free and Halogen-free)


N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	10 s	Steady State	Unit
Drain-Source Voltage	V_{DS}	20		V
Gate-Source Voltage	V_{GS}	± 12		
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	3.9	3.3	A
		3.1	2.6	
Pulsed Drain Current (10 μ s Pulse Width)	I_{DM}	30		
Continuous Source Current (Diode Conduction) ^a	I_S	1.0	0.72	
Maximum Power Dissipation ^a	P_D	1.13	0.80	W
		0.72	0.51	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	186	110	°C/W
		125	155	
Maximum Junction-to-Foot (Drain)	R_{thJF}	65	85	

Notes:

a. Surface Mounted on FR4 board, $t \leq 10$ s.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>.

SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

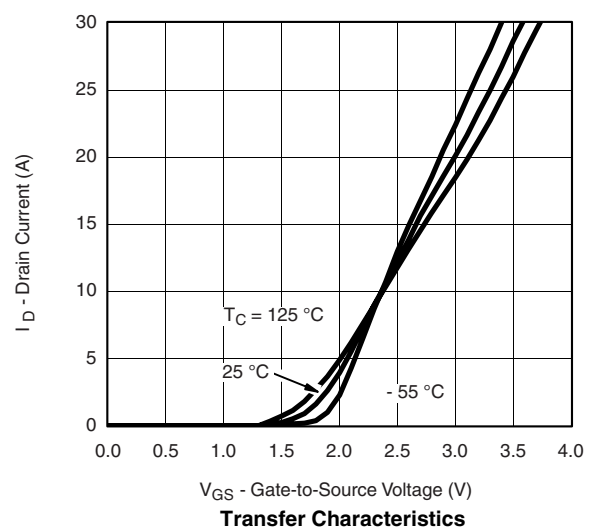
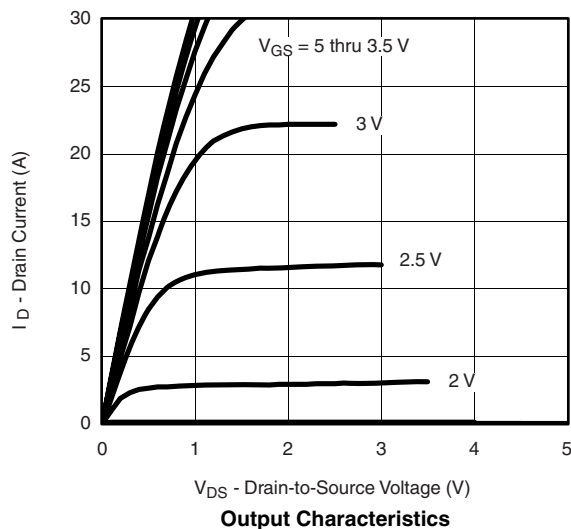
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	0.6		1.8	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 12\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 70^\circ\text{C}$			15	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 4.5\ \text{V}$	10			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 4.5\ \text{V}$, $I_D = 3.9\ \text{A}$		0.035	0.045	Ω
		$V_{GS} = 3.0\ \text{V}$, $I_D = 3.5\ \text{A}$		0.042	0.055	
		$V_{GS} = 2.5\ \text{V}$, $I_D = 3.0\ \text{A}$		0.050	0.065	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 3.9\ \text{A}$		14		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.0\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.75	1.1	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = 6\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 3.9\ \text{A}$		4.0	6	nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.0		
Gate Resistance	R_g			1.9		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 6\ \text{V}$, $R_L = 6\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 4.5\ \text{V}$, $R_g = 6\ \Omega$		40	60	ns
Rise Time	t_r			50	75	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.0\ \text{A}$, $dI/dt = 100\ \text{A}/\mu\text{s}$		20	40	

Notes:

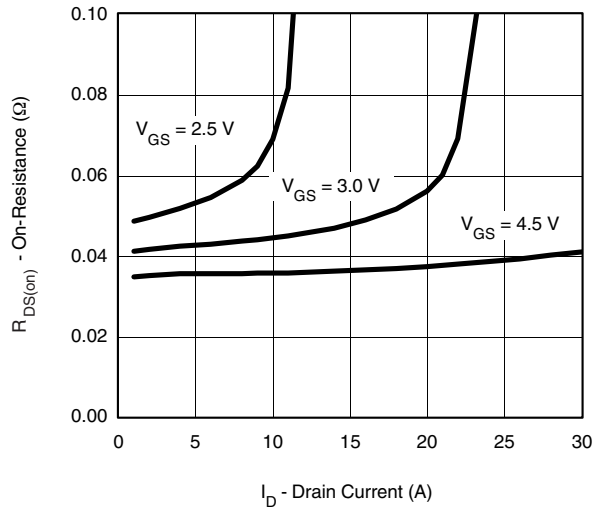
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

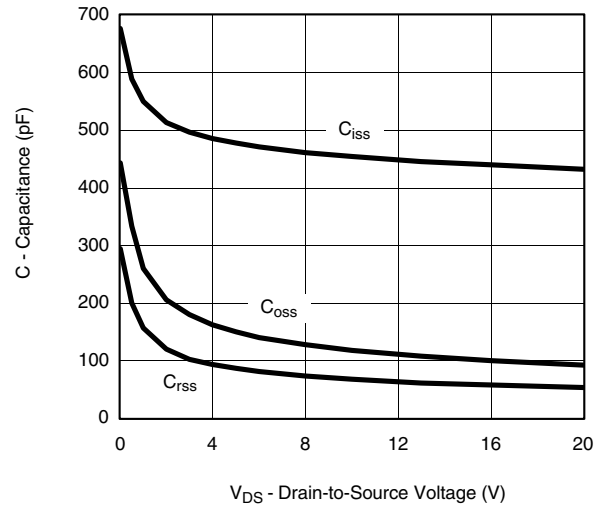
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25°C , unless otherwise noted

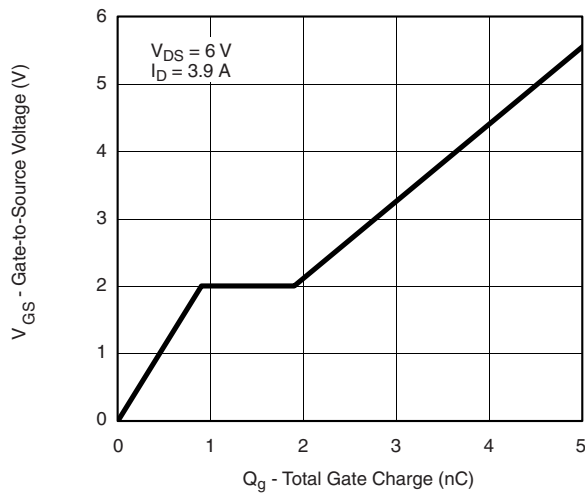
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



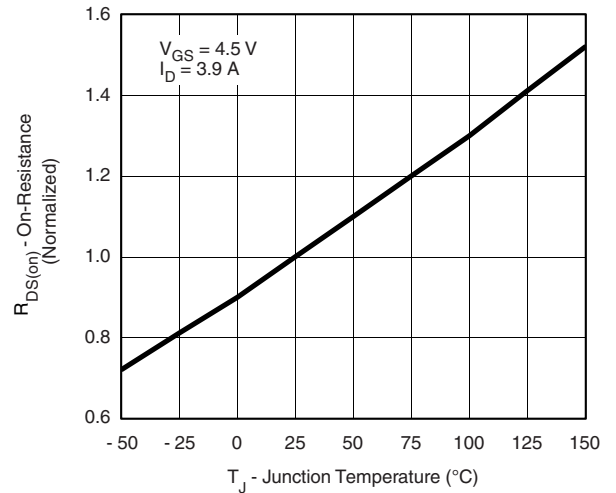
On-Resistance vs. Drain Current



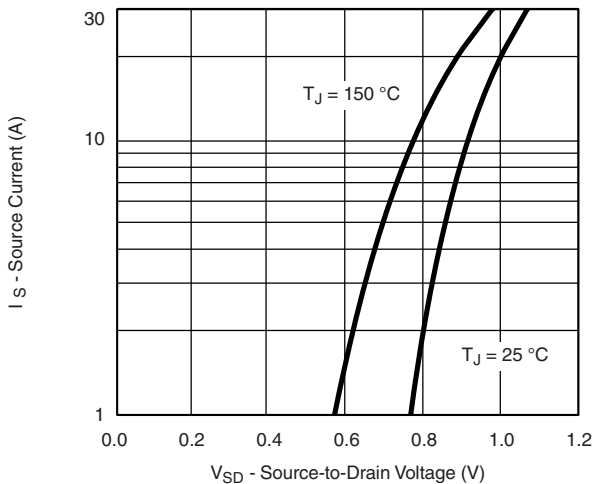
Capacitance



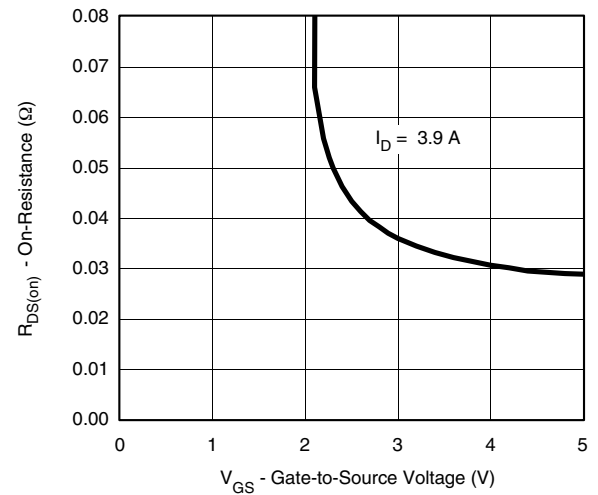
Gate Charge



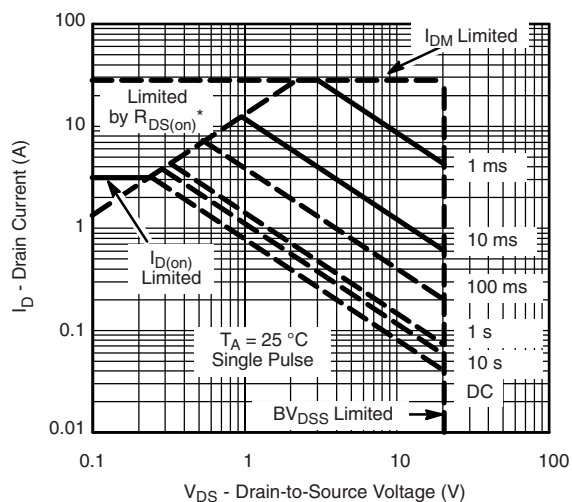
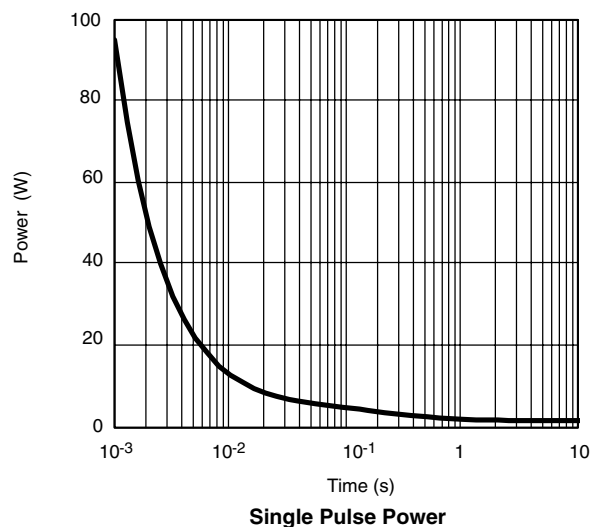
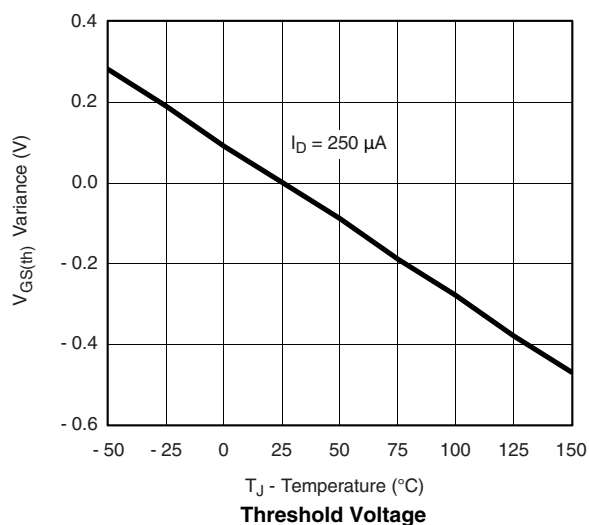
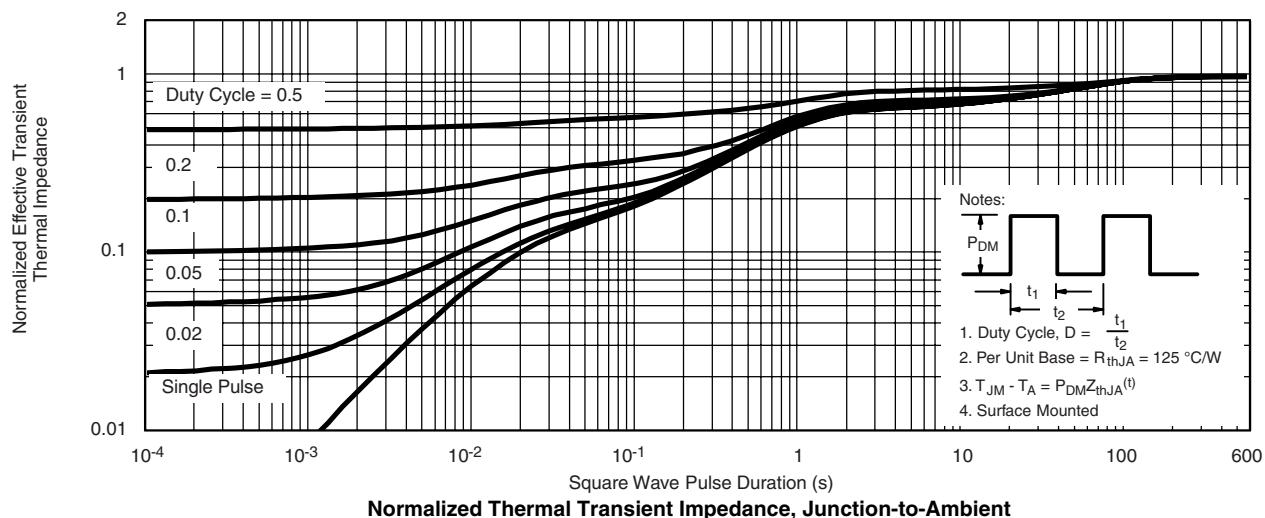
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

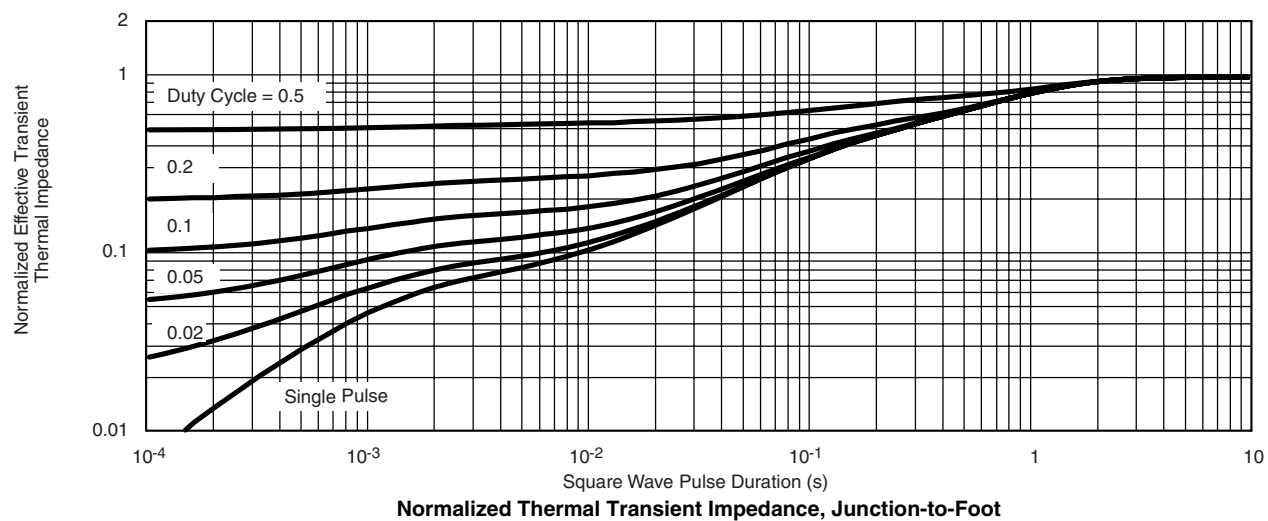


On-Resistance vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Case**



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72623>.



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