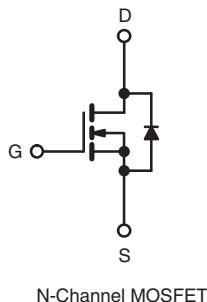
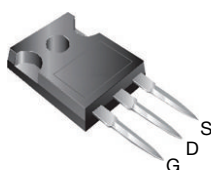


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.21
Q_g (Max.) (nC)	180	
Q_{gs} (nC)	61	
Q_{gd} (nC)	85	
Configuration	Single	

TO-247AC


FEATURES

- Superfast body diode eliminates the need for external diodes in ZVS applications
- Lower gate charge results in simpler drive requirements
- Enhanced dV/dt capabilities offer improved ruggedness
- Higher gate voltage threshold offers improved noise immunity
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

APPLICATIONS

- Zero voltage switching (SMPS)
- Telecom and server power supplies
- Uninterruptible power supplies
- Motor control applications

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFP26N60LPbF
	SiHFP26N60L-E3
SnPb	IRFP26N60L
	SiHFP26N60L

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current	V_{GS} at 10 V	$T_C = 25\text{ }^{\circ}\text{C}$	A
		$T_C = 100\text{ }^{\circ}\text{C}$	
Pulsed Drain Current ^a	I_{DM}	100	
Linear Derating Factor		3.8	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy ^b	E_{AS}	570	mJ
Repetitive Avalanche Current ^a	I_{AR}	26	A
Repetitive Avalanche Energy ^a	E_{AR}	47	mJ
Maximum Power Dissipation	$T_C = 25\text{ }^{\circ}\text{C}$	P_D	470
Peak Diode Recovery dV/dt ^c	dV/dt	21	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature) ^d	for 10 s	300	
Mounting Torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 1.7\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 26\text{ A}$, $dV/dt = 21\text{ V/ns}$ (see fig. 12).
- $I_{SD} \leq 26\text{ A}$, $dI/dt \leq 480\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	40	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.24	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.27	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		600	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.33	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	50	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$		-	-	2.0	mA
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}^b$	-	0.21	0.25	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 16\text{ A}$		13	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	5020	-	pF
Output Capacitance	C_{oss}			-	450	-	
Reverse Transfer Capacitance	C_{rss}			-	34	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 480\text{ V}^c$	-	230	-	
Effective Output Capacitance (Energy related)	$C_{oss\text{ eff. (ER)}}$			-	170	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 26\text{ A}$, $V_{DS} = 480\text{ V}$, see fig. 7 and 15 ^b	-	-	180	nC
Gate-Source Charge	Q_{gs}			-	-	61	
Gate-Drain Charge	Q_{gd}			-	-	85	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}$, $I_D = 26\text{ A}$, $R_g = 4.3\text{ }\Omega$, $V_{GS} = 10\text{ V}$ see fig. 11a and 11b ^b		-	31	-	ns
Rise Time	t_r			-	110	-	
Turn-Off Delay Time	$t_{d(off)}$			-	47	-	
Fall Time	t_f			-	42	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	26	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	100		
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 26\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 26\text{ A}$		-	170	250	ns
		$T_J = 125\text{ }^\circ\text{C}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	210	320	
Body Diode Reverse Recovery Charge	Q_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 26\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	670	1000	nC
		$T_J = 125\text{ }^\circ\text{C}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	1050	1570	
Reverse Recovery Current	I_{RRM}	$T_J = 25\text{ }^\circ\text{C}$		-	7.3	11	A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
 $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

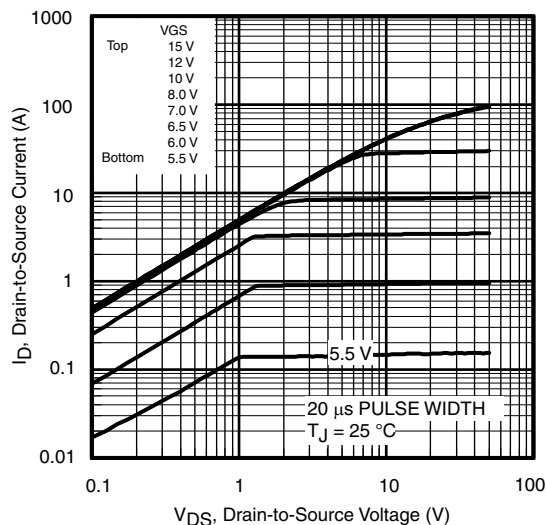


Fig. 1 - Typical Output Characteristics

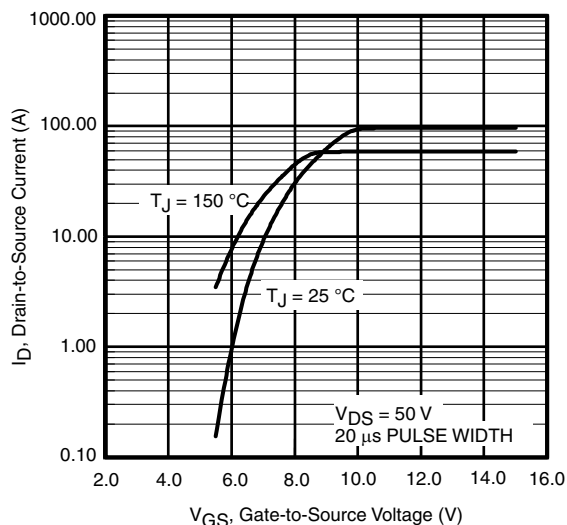


Fig. 3 - Typical Transfer Characteristics

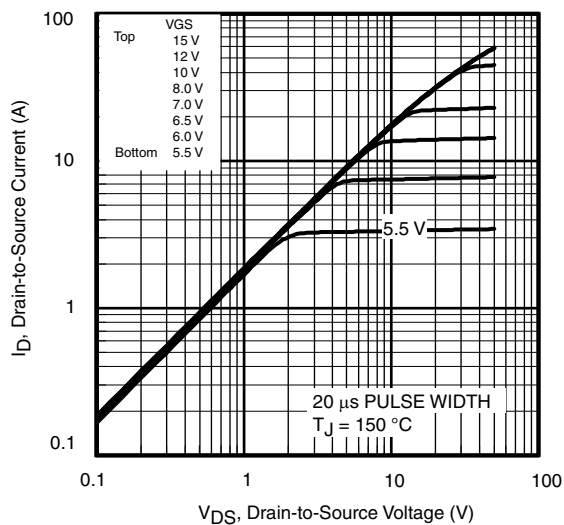


Fig. 2 - Typical Output Characteristics

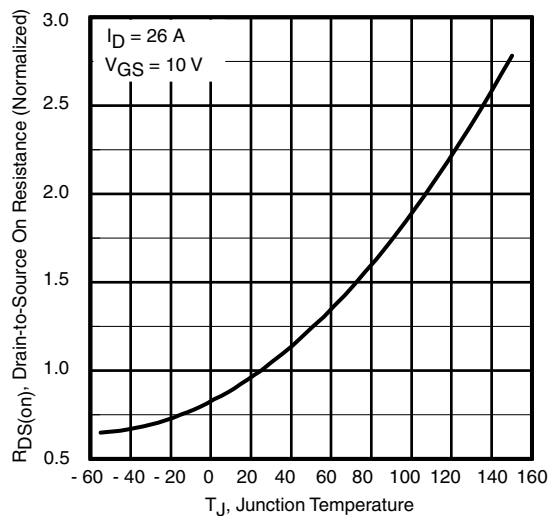
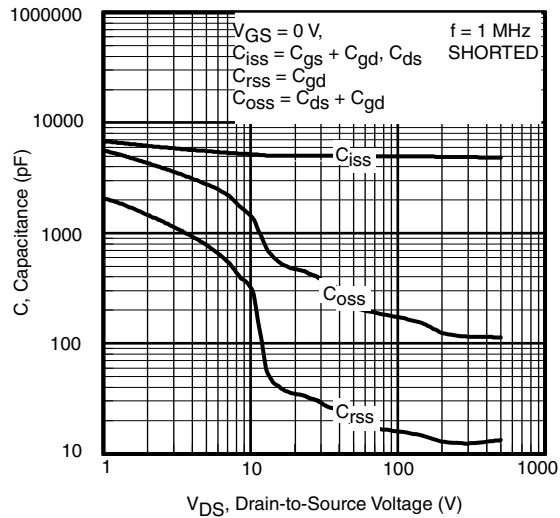
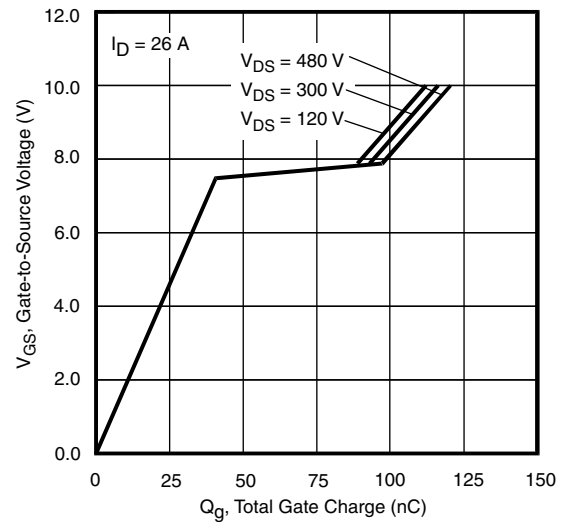
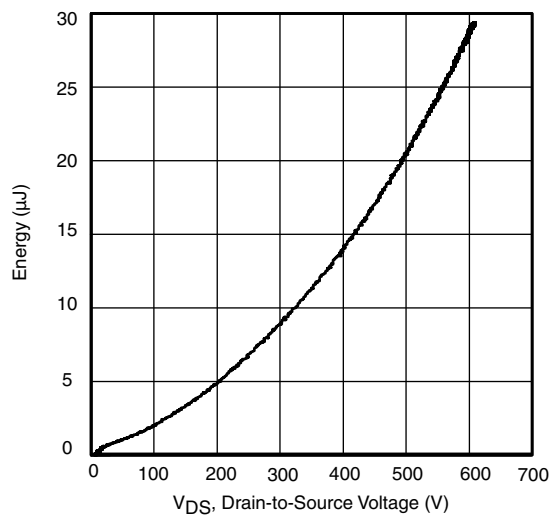
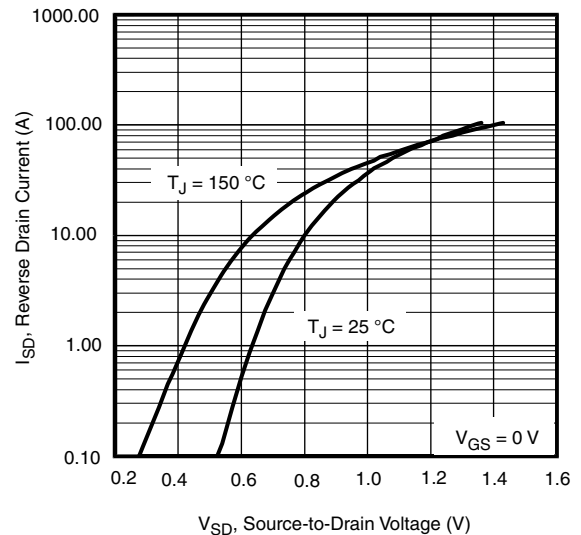
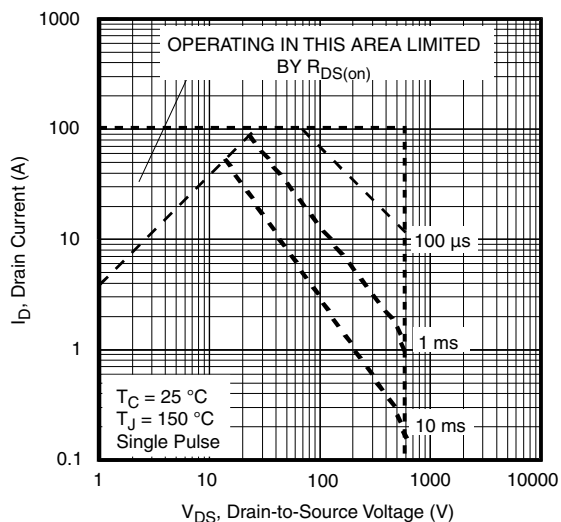
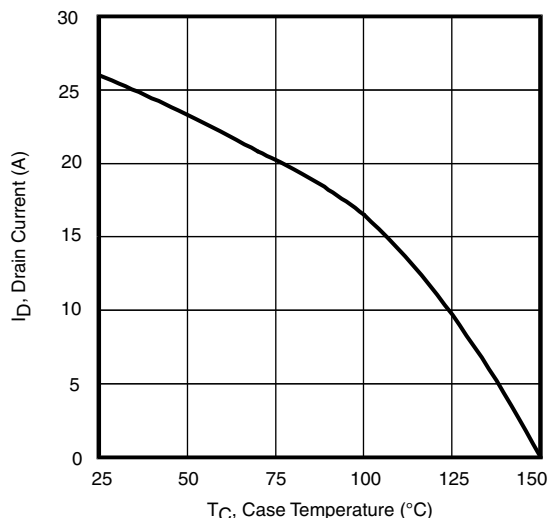
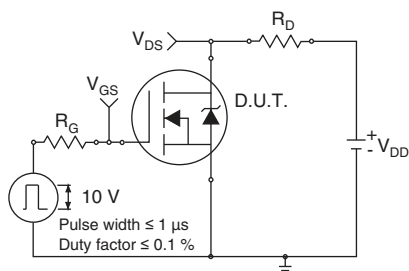
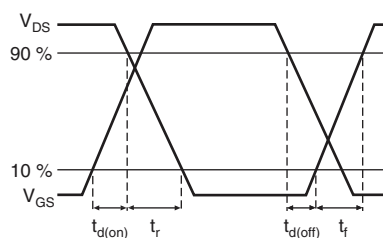
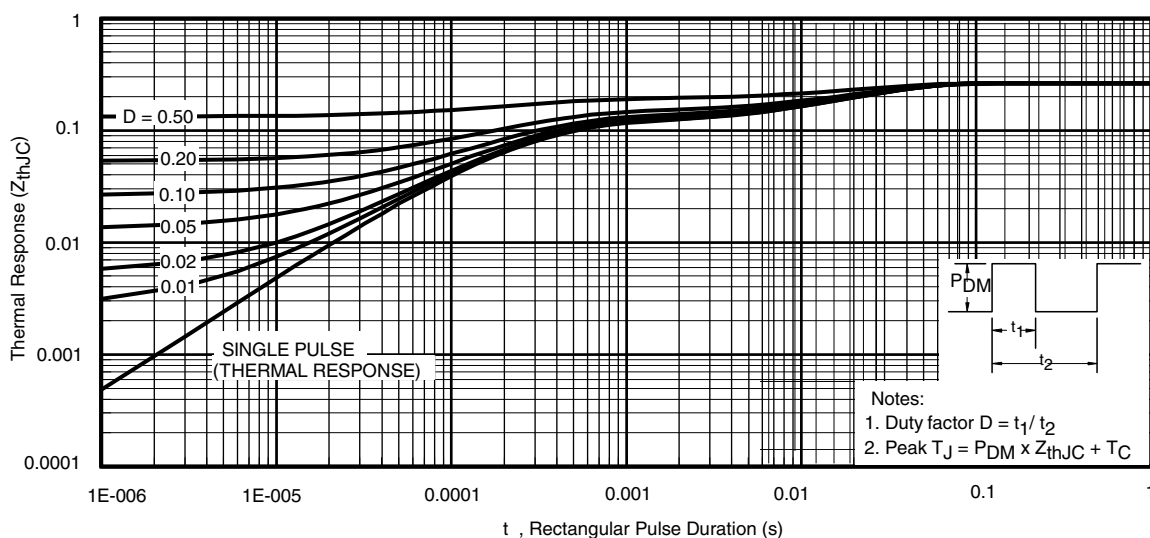
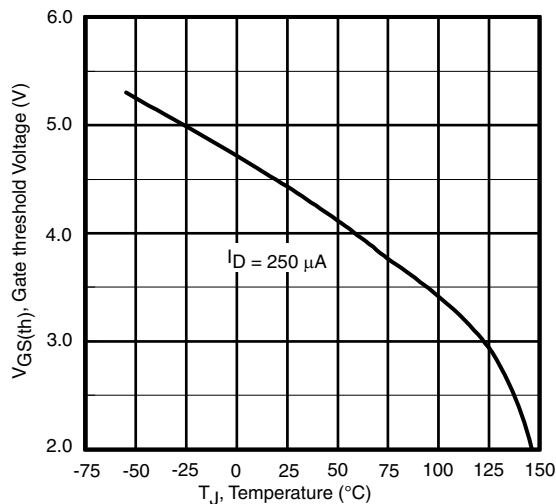
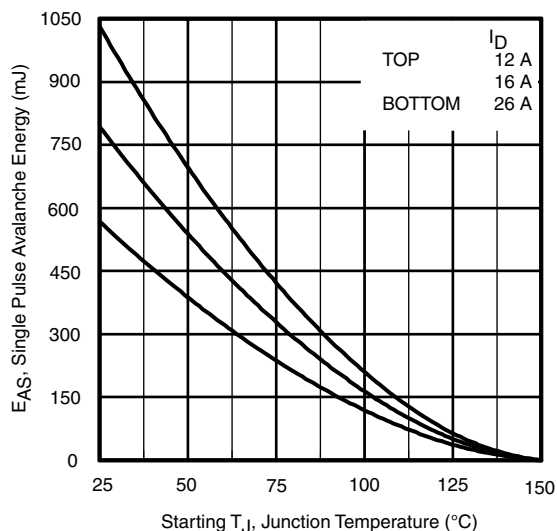
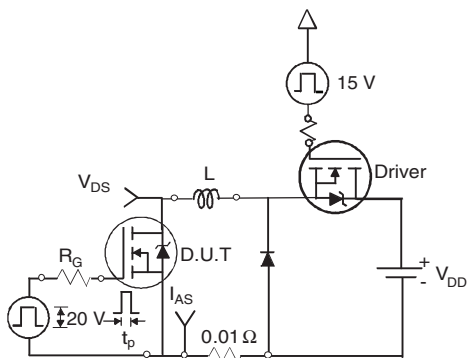
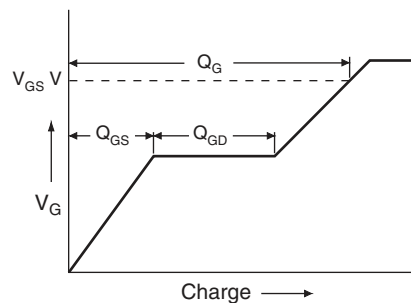
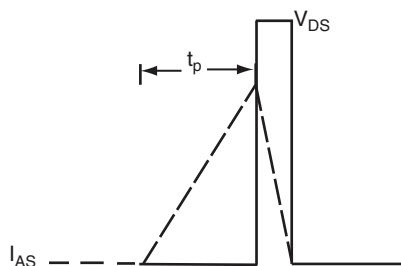
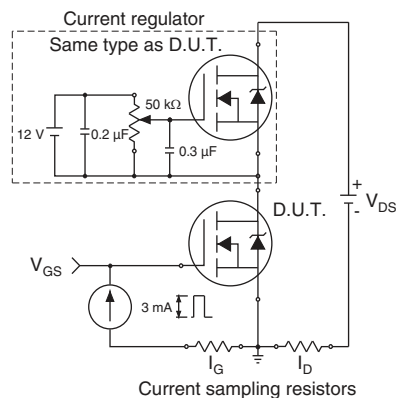
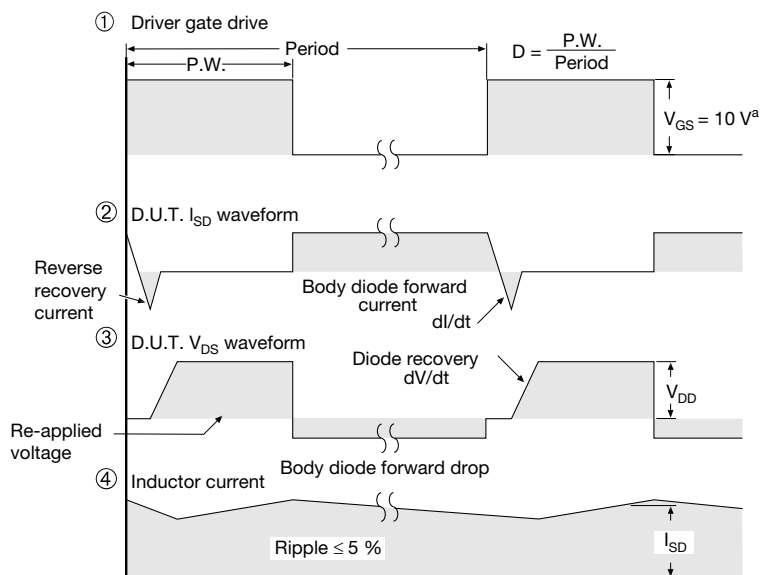
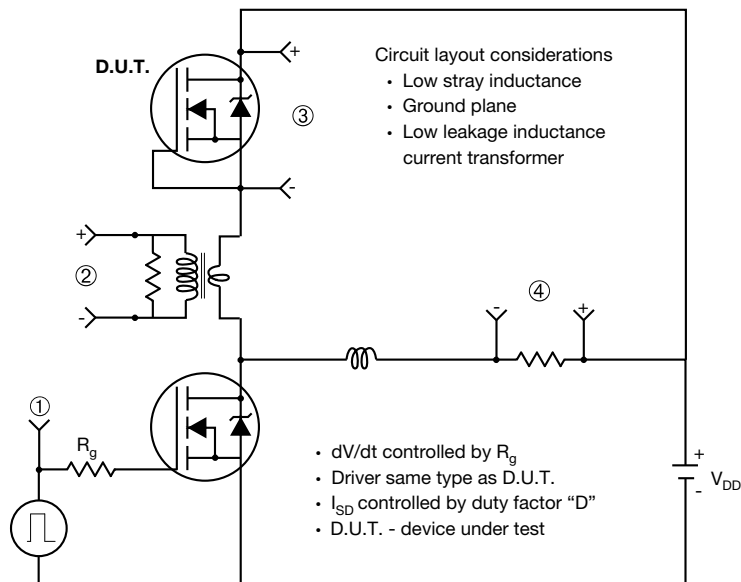


Fig. 4 - Normalized On-Resistance vs. Temperature


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

Fig. 8 - Typical Source-Drain Diode Forward Voltage


Fig. 9 - Maximum Safe Operating Area

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 11a - Switching Time Test Circuit

Fig. 11b - Switching Time Waveforms

Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 13 - Threshold Voltage vs. Temperature

Fig. 14c - Maximum Avalanche Energy vs. Drain Current

Fig. 14a - Unclamped Inductive Test Circuit

Fig. 15a - Basic Gate Charge Waveform

Fig. 14b - Unclamped Inductive Waveforms

Fig. 15b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 16 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91218.



TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9



MILLIMETERS			
DIM.	MIN.	MAX.	NOTES
A	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
c	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

MILLIMETERS			
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
e	5.44 BSC		
L	14.90	15.40	
L1	3.96	4.16	6
Ø P	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	

Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



VERSION 2: FACILITY CODE = Y



	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E19-0614-Rev. E, 08-Jan-2020
DWG: 5971

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Contour of slot optional
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions D1 and E1
- Lead finish uncontrolled in L1
- Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- Outline conforms to JEDEC outline TO-247 with exception of dimension c



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