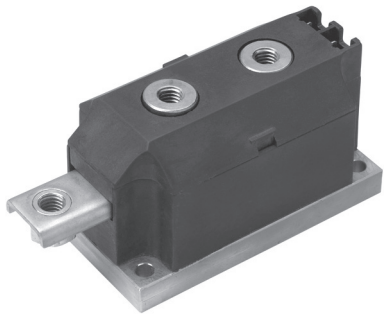
Fast Thyristor/Diode and Thyristor/Thyristor (MAGN-A-PAK Power Modules), 200 A



MAGN-A-PAK

FEATURES

- Fast turn-off thyristor
- Fast recovery diode
- High surge capability
- Electrically isolated baseplate
- 3500 V_{RMS} isolating voltage
- Industrial standard package
- UL approved file E78996
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level

Pb-free
RoHS COMPLIANT

PRODUCT SUMMARY	
$I_{T(AV)}$	200 A
Type	Modules - Thyristor, Fast

DESCRIPTION

This series of MAGN-A-PAK modules are intended for applications such as self-commutated inverters, DC choppers, electronic welders, induction heating and others where fast switching characteristics are required.

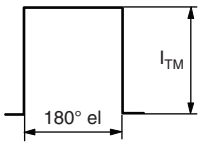
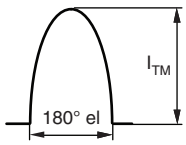
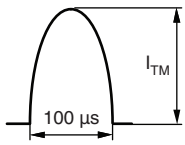
MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{T(AV)}$		200	A
	T_C	85	°C
$I_{T(RMS)}$		444	A
I_{TSM}	50 Hz	7600	
	60 Hz	8000	
I^2t	50 Hz	290	kA^2s
	60 Hz	265	
$I^2\sqrt{t}$		2900	$kA^2\sqrt{s}$
t_q		20/25	µs
t_{rr}		2	
V_{DRM}/V_{RRM}		800/1200	V
T_J	Range	- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE AND OFF-STATE BLOCKING VOLTAGE V	V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT T_J = 125 °C mA
VSK.F200-	08	800	800	50
	12	1200	1200	

For technical questions within your region, please contact one of the following:
DiodesAmericas@vishay.com, DiodesAsia@vishay.com, DiodesEurope@vishay.com

CURRENT CARRYING CAPABILITY

FREQUENCY							UNITS
50 Hz	380	560	630	850	2460	3180	A
400 Hz	460	690	710	1060	1570	2080	
2500 Hz	310	450	530	760	630	860	
5000 Hz	250	360	410	560	410	560	
10 000 Hz	180	280	300	410	-	-	
Recovery voltage V_r	50	50	50	50	50	50	V
Voltage before turn-on V_d	80 % V_{DRM}		80 % V_{DRM}		80 % V_{DRM}		
Rise of on-state current dI/dt	50	50	-	-	-	-	A/µs
Case temperature	85	60	85	60	85	60	°C
Equivalent values for RC circuit	10/0.47		10/0.47		10/0.47		Ω/µF

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction, half sine wave			200	A
					85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch			444	A
Maximum peak, one-cycle non-repetitive on-state, surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial T_J = 125 °C	7600	
		t = 8.3 ms			8000	
		t = 10 ms	100 % V_{RRM} reapplied		6400	
		t = 8.3 ms			6700	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		290	kA^2s
		t = 8.3 ms			265	
		t = 10 ms	100 % V_{RRM} reapplied		205	
		t = 8.3 ms			187	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied			2900	$kA^2\sqrt{s}$
Low level value or threshold voltage	$V_{T(TO)1}$	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J = T_J maximum			1.18	V
High level value of threshold voltage	$V_{T(TO)2}$	(I > π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J = T_J maximum			1.25	
Low level value on-state slope resistance	r_{t1}	(16.7 % x π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J = T_J maximum			0.74	mΩ
High level value on-state slope resistance	r_{t2}	(I > π x $I_{T(AV)}$ < I < π x $I_{T(AV)}$), T_J = T_J maximum			0.70	
Maximum on-state voltage drop	V_{TM}	I_{pk} = 600 A, T_J = T_J maximum, t_p = 10 ms sine pulse			1.73	V
Maximum holding current	I_H	T_J = 25 °C, I_T > 30 A			600	mA
Maximum latching current	I_L	T_J = 25 °C, V_A = 12 V, Ra = 6 Ω, I_g = 1A			1000	

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SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES		UNITS
			K	J	
Maximum non-repetitive rate of rise	dI/dt	Gate drive 20 V, 20 Ω, $t_r \leq 1$ ms, V_D = 80 % V_{DRM}, T_J = 25 °C	800		A/µs
Maximum recovery time	t_{rr}	I_{TM} = 350 A, dI/dt = - 25 A/µs, V_R = 50 V, T_J = 25 °C	2		µs
Maximum turn-off time	t_q	I_{TM} = 750 A; T_J = T_J maximum; dI/dt = - 25 A/µs; V_R = 50 V; dV/dt = 400 V/µs linear to 80 % V_{DRM}	20	25	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T_J = 125 °C, exponential to 67 % V_{DRM}	1000	V/µs
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, T_J = 25 °C, t = 1 s	3000	V
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	T_J = 125 °C, rated V_{DRM}/V_{RRM} applied	50	mA

TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	f = 50 Hz, d% = 50	60	W
Maximum peak average gate power	$P_{G(AV)}$	T_J = 125 °C, f = 50 Hz, d% = 50	10	
Maximum peak positive gate current	I_{GM}	T_J = 125 °C, $t_p \leq 5$ ms	10	A
Maximum peak negative gate voltage	$-V_{GT}$		5	V
Maximum DC gate current required to trigger	I_{GT}	T_J = 25 °C, V_{ak} 12 V, Ra = 6	200	mA
DC gate voltage required to trigger	V_{GT}		3	V
DC gate current not to trigger	I_{GD}	T_J = 125 °C, rated V_{DRM} applied	20	mA
DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		- 40 to 125	°C
Storage temperature range	T_{Stg}		- 40 to 150	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.125	K/W
Maximum thermal resistance, case to heatsink per module	R_{thC-hs}	Mounting surface flat, smooth and greased	0.025	
Mounting torque ± 10 % — MAP to heatsink		A mounting compound is recommended. The torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Use of cable lugs is not recommended, busbar should be used and restrained during tightening. Threads must be lubricated with a compound.	4 to 6 (35 to 53)	N · m (lbf · in)
Mounting torque ± 10 % — busbar to MAP				
Approximate weight			500	g
			17.8	oz.
Case style			MAGN-A-PAK	

ΔR_{thJC} CONDUCTION			
CONDUCTIONS ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	UNITS
180°	0.009	0.006	K/W
120°	0.10	0.011	
90°	0.014	0.015	
60°	0.020	0.020	
30°	0.32	0.033	

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

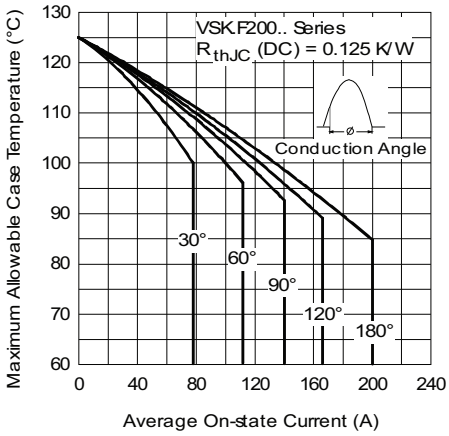


Fig. 1 - Current Ratings Characteristics

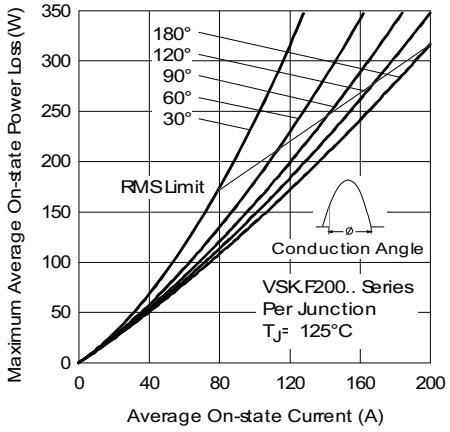


Fig. 3 - On-State Power Loss Characteristics

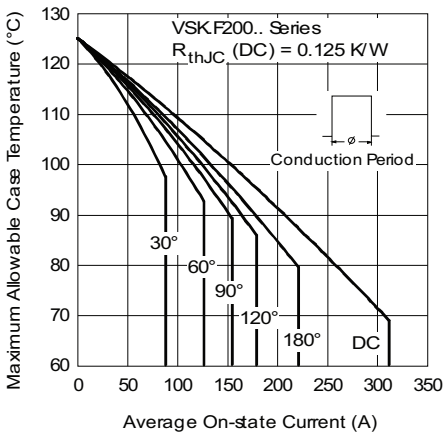


Fig. 2 - Current Ratings Characteristics

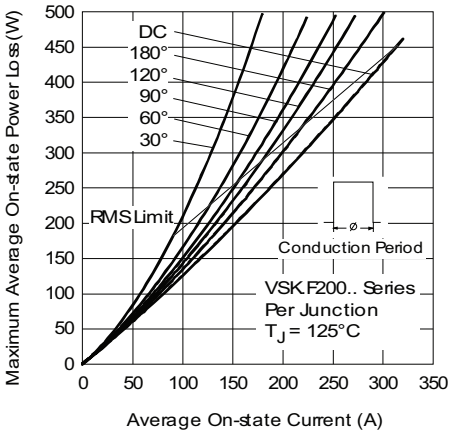


Fig. 4 - On-State Power Loss Characteristics

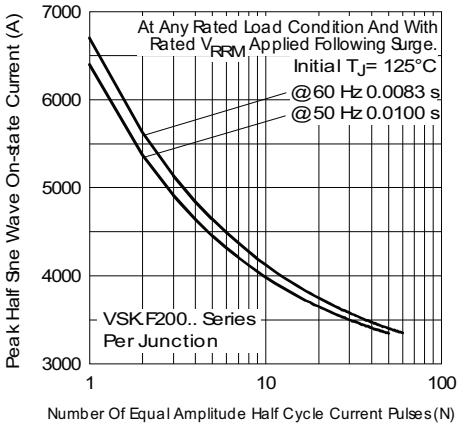


Fig. 5 - Maximum Non-Repetitive Surge Current

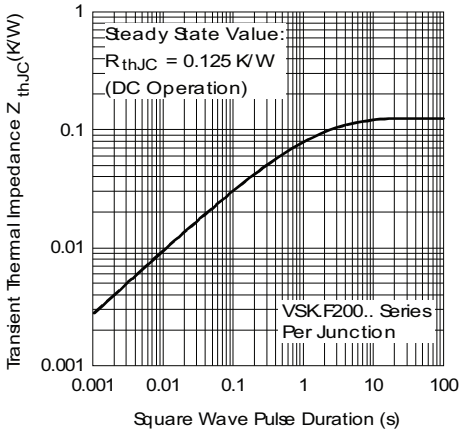


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

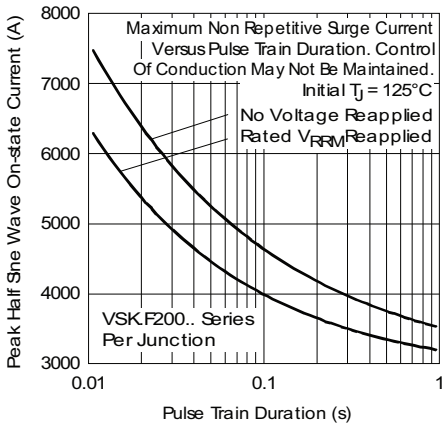


Fig. 6 - Maximum Non-Repetitive Surge Current

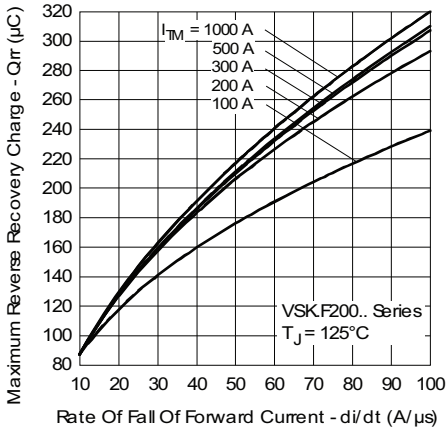


Fig. 9 - Reverse Recovery Charge Characteristics

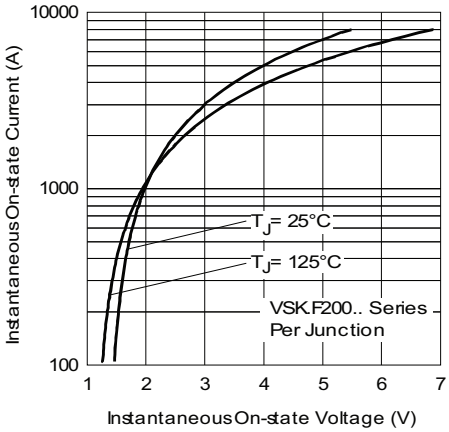


Fig. 7 - On-State Voltage Drop Characteristics

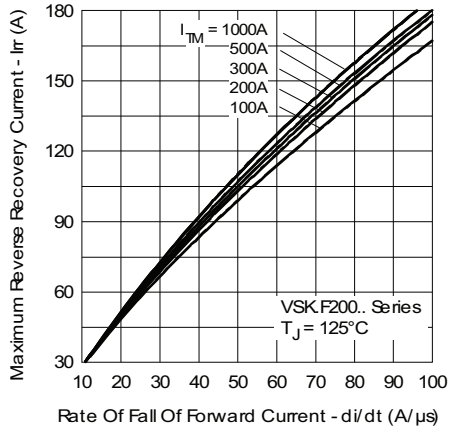


Fig. 10 - Reverse Recovery Current Characteristics

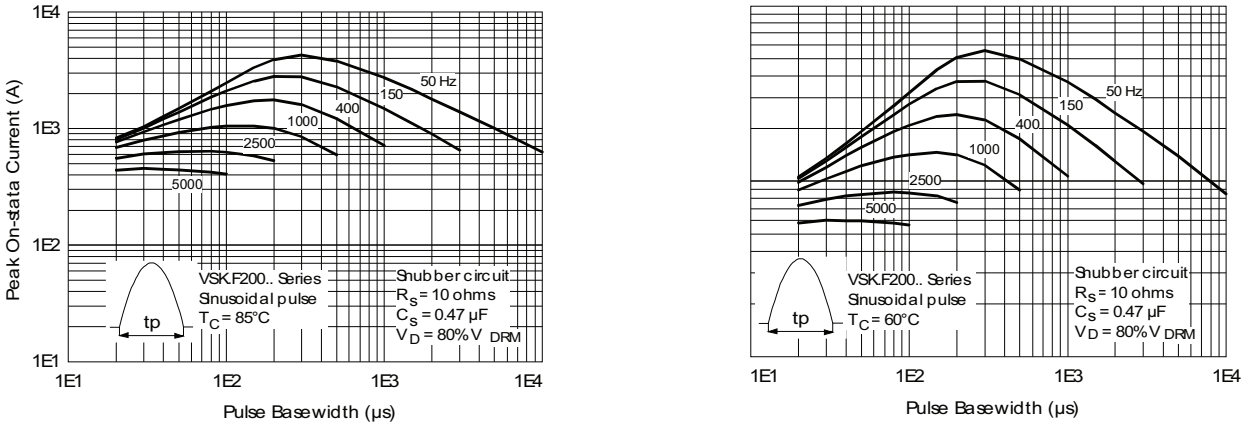


Fig. 11 - Frequency Characteristics

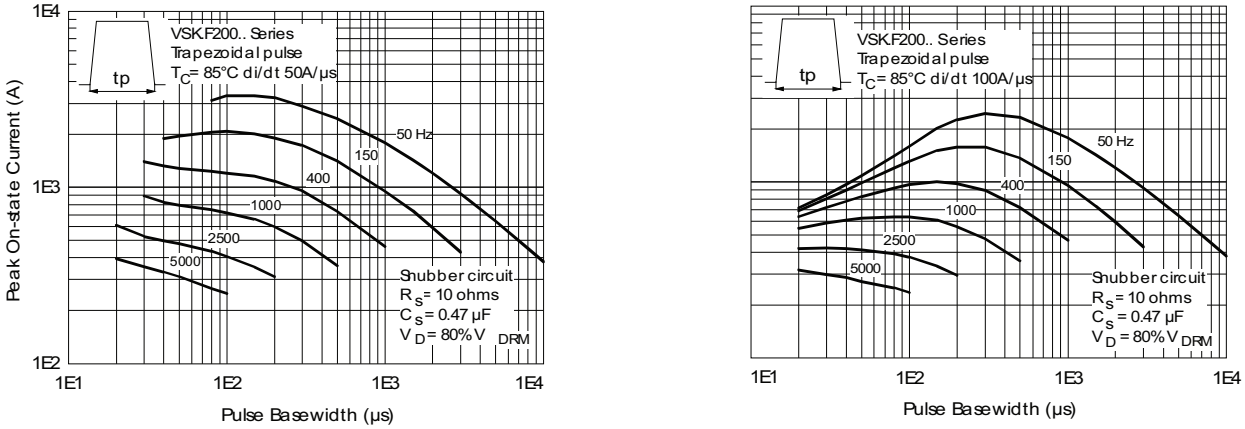


Fig. 12 - Frequency Characteristics

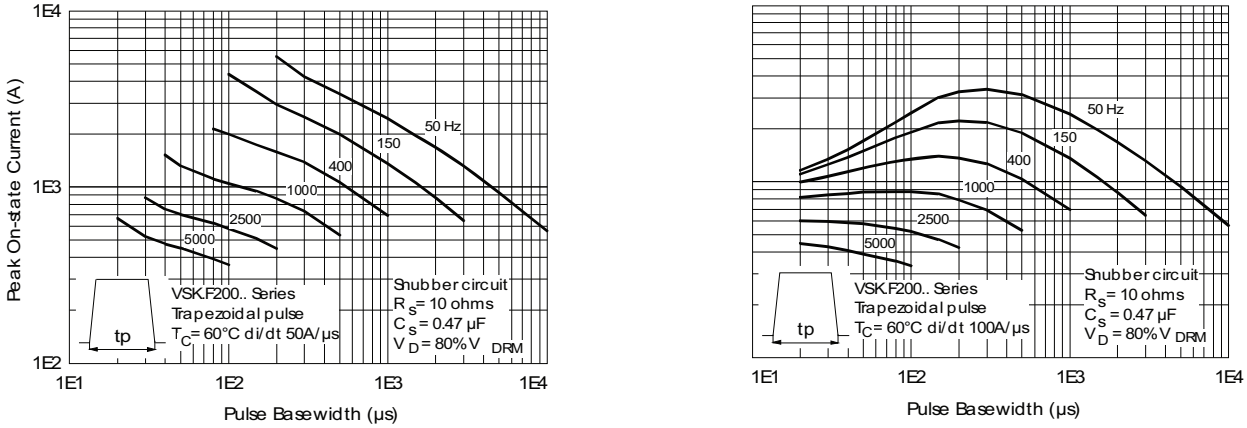


Fig. 13 - Frequency Characteristics

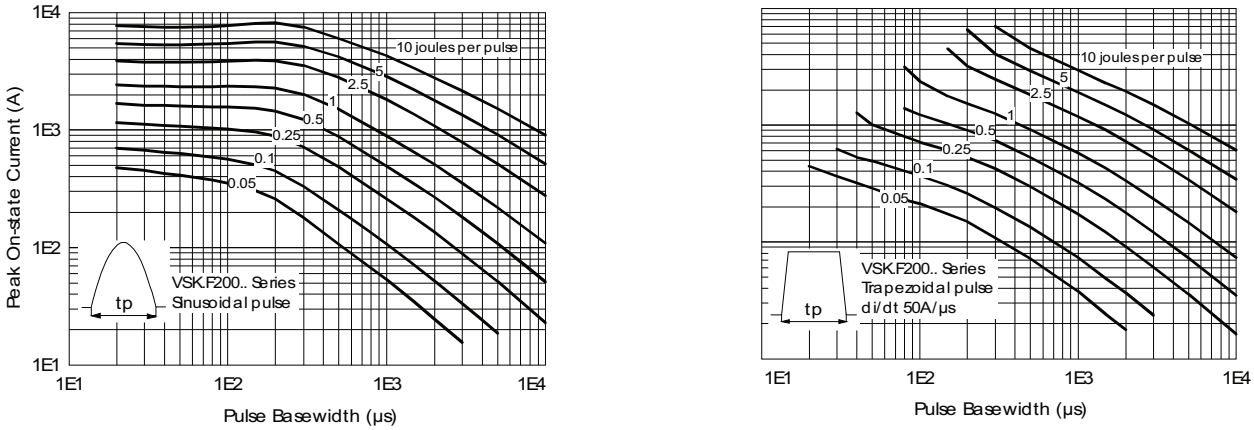


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

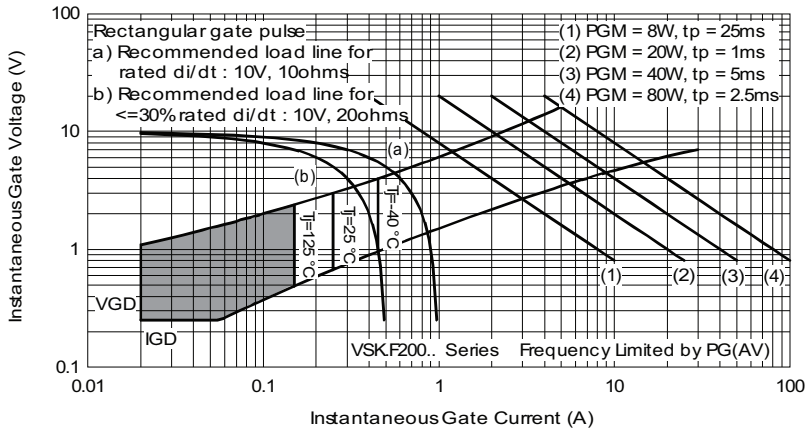


Fig. 15 - Gate Characteristics

ORDERING INFORMATION TABLE

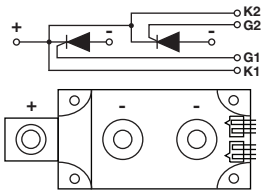
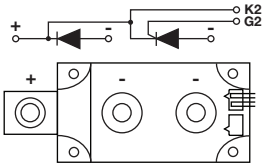
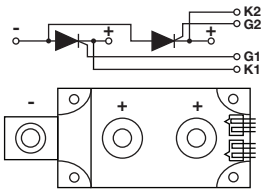
Device code

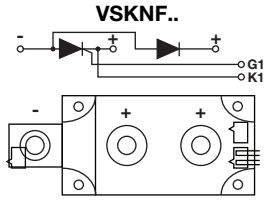
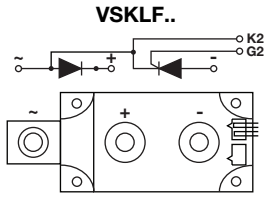
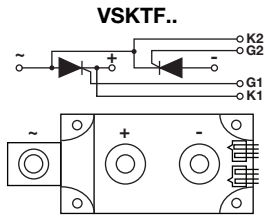
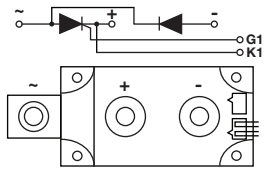
VSK	T	F	200	-	12	H	K	P
1	2	3	4		5	6	7	8

1 - Module type
2 - Circuit configuration (see circuit configuration table)
3 - Fast SCR
4 - Current rating: $I_{T(AV)}$ x 10 rounded
5 - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
6 - dV/dt code: H ≤ 400 V/µs
7 - t_q code: K ≤ 20 µs
J ≤ 25 µs
8 - Lead (Pb)-free

Note

- To order the optional hardware go to www.vishay.com/doc?95172

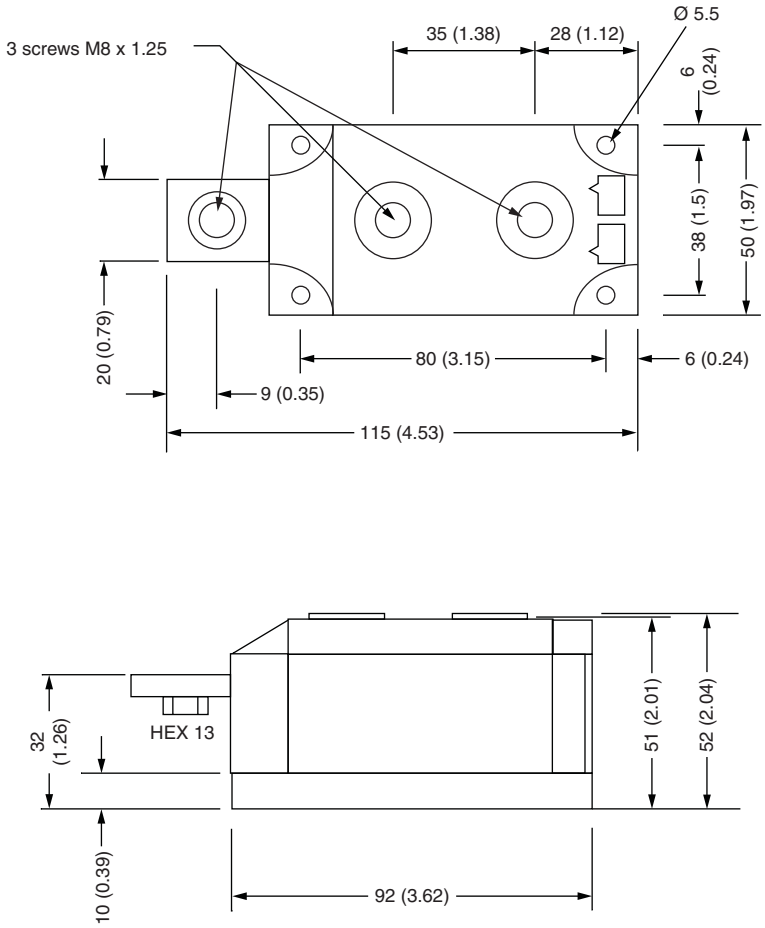
CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
Two SCRs common cathodes	U	**VSKUF..** 
SCR/diode common cathodes	K	**VSKKF..** 
Two SCRs common anodes	V	**VSKVF..** 

CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	**CIRCUIT CONFIGURATION CODE**	**CIRCUIT DRAWING**
SCR/diode common anodes	N	**VSKNF..** 
SCR/diode doubler circuit, negative control	L	**VSKLF..** 
Two SCRs doubler circuit	T	**VSKTF..** 
SCR/diode doubler circuit, positive control	H	**VSKHF..** 

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95086

MAGN-A-PAK

DIMENSIONS in millimeters (inches)



Notes

- Dimensions are nominal
- Full engineering drawings are available on request
- UL identification number for gate and cathode wire: UL 1385
- UL identification number for package: UL 94 V-0

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