

TC7MP245FK, TC7MP245FTG

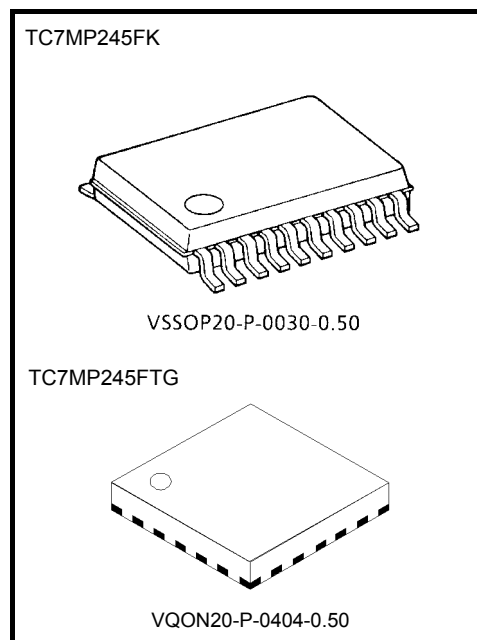
Low-Voltage/Low-Power Octal Bus Transceiver with Bus-hold

The TC7MP245 is a high-performance CMOS octal bus transceiver. By a low power consumption circuit, power consumption has been reduced when a bus terminal is disable state ($\overline{OE}$ =High).

The direction of data transmission is determined by the level of the DIR input. The $\overline{OE}$ input can be used to disable the device so that the busses are effectively isolated.

But, bus of a B bus side at floating state is maintained in an appropriate logic level due to a bus hold circuit to a B bus. Moreover, the bus-hold circuit which is added to a B bus is off when $\overline{OE}$ is low.

All inputs are equipped with protection circuits against static discharge.



Weight:

VSSOP20-P-0030-0.50 : 0.03 g (typ.)

VQON20-P-0404-0.50 : 0.0145 g (typ.)

Features

- Low-voltage operation : $V_{CC} = 1.65$ to 3.6 V
- Low power current consumption : By a new input circuit, power consumption in $\overline{OE}$ =H is reduced largely.
It is most suitable for battery drive products such as personal digital assistant or a cellular phone.
- Quiescent supply current : $I_{CC} = 5 \mu A$ (max) (V_{CC} =3.6V)
- High-speed operation : $t_{pd} = 3.0$ ns (max) (V_{CC} =3.3±0.3V)
 $t_{pd} = 4.6$ ns (max) (V_{CC} =2.5±0.2V)
 $t_{pd} = 10.0$ ns (max) (V_{CC} =1.8±0.15V)
- Output current : I_{OHA}/I_{OLA} (A bus) = ± 12 mA (min) (V_{CC} =3.0V)
 I_{OHB}/I_{OLB} (B bus) = ± 24 mA (min) (V_{CC} =3.0V)
- Latch-up performance : ± 300 mA
- ESD performance : Machine model $\geq \pm 200$ V
Human body model $\geq \pm 2000$ V
- Ultra-small package : VSSOP(US20), VQON20
- Bus hold circuit is built in only the B bus side.(Only in $\overline{OE}$ =H, a former state is maintained.)
- Floating of A-bus and B-bus are permitted.(When $\overline{OE}$ =H)
- Gate IC for control(TC7MP01FK) of DIR and $\overline{OE}$ terminal are prepared.
- 3.6V tolerant function provided on A-bus terminal, DIR and $\overline{OE}$ terminal.

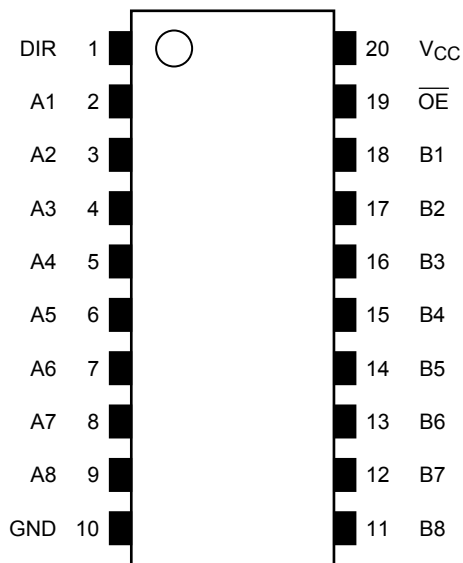
Note 1: At the time bus terminal is enable state, please do not give a signal from the outside.

Note 2: When mounting VQON package, the type of recommended flux is RA or RMA.

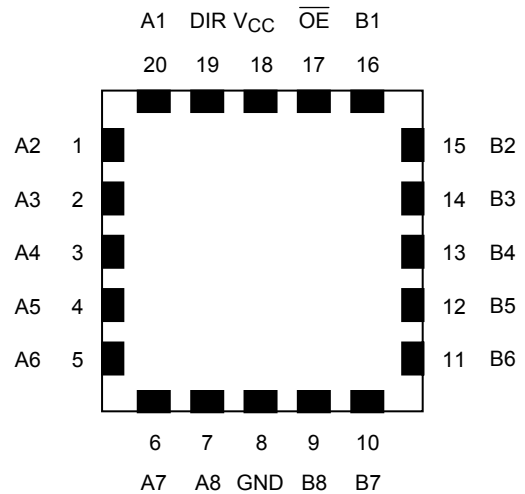
Start of commercial production
2002-03

Pin Assignment (top view)

FK (VSSOP20-P-0030-0.50)



FTG (VQON20-P-0404-0.50)



Truth Table

Input		Bus state	Bus hold circuit (B bus)
DIR	$\overline{\text{OE}}$		
L	L	$B \rightarrow A (B=A)$	OFF
H	L	$A \rightarrow B (A=B)$	OFF
X	H	Z	ON*

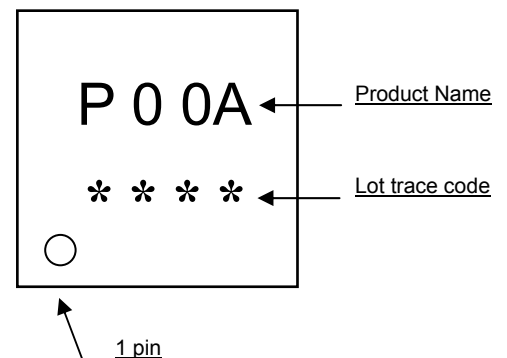
X: Don't care

Z: High impedance

*: Logic state just before becoming disable is maintained.

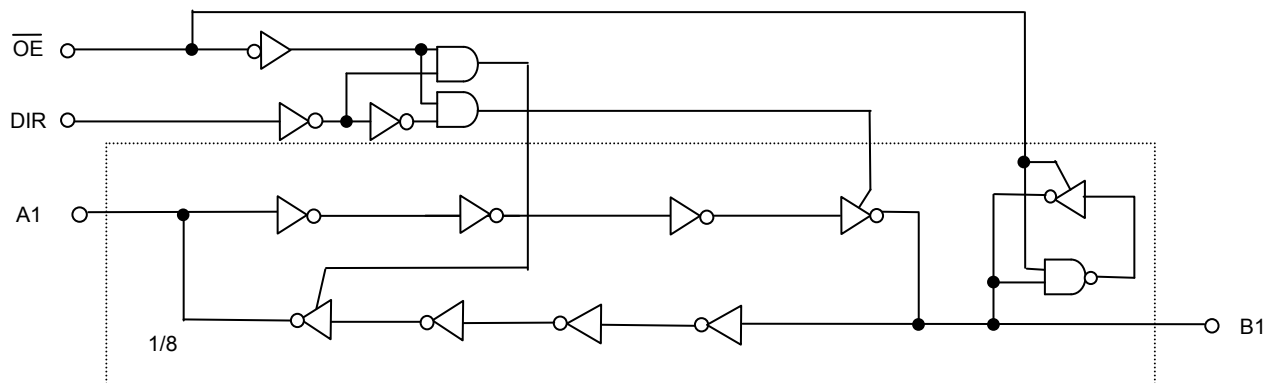
Marking

FTG (VQON20-P-0404-0.50)



Note: When a bus input is in "H" state and an output is switched to "enable" to "disable", Glitch such as "L" state during about 1 to 3ns occurs in an output. It is not generated when a bus input is in "L" state.

System Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.5 to 4.6	V
DC input voltage (DIR, $\overline{OE}$)	V_{IN}	-0.5 to 4.6	V
DC input/output voltage(A bus)	$V_{I/OA}$	-0.5 to 4.6 (Note 2)	V
		-0.5 to $V_{CC}+0.5$ (Note 3)	
DC input/output voltage(B bus)	$V_{I/OB}$	-0.5 to $V_{CC}+0.5$	V
Input diode current(DIR, $\overline{OE}$)	$I_{I/K}$	-50	mA
Input/Output diode current	$I_{I/OK}$	± 50	mA
Output current	I_{OUT}	± 50	mA
DC V_{CC} /ground current	I_{CC}/I_{GND}	± 100	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: $V_{CC}=0\text{V}$, or output off state.

Note 3: $\overline{OE}=\text{"L"}$, DIR="L"

Operating Ranges (Note 1)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.65 to 3.6	V
		1.2 to 3.6 (Note 2)	
DC input voltage (DIR, $\overline{OE}$)	V_{IN}	-0.3 to 3.6	V
DC input/output voltage(A bus)	$V_{I/OA}$	0 to 3.6 (Note 3)	V
		0 to V_{CC} (Note 4)	
DC input/output voltage(B bus)	$V_{I/OB}$	0 to V_{CC}	V
Output current (A bus)	I_{OHA}/I_{OLA}	± 12 (Note 5)	mA
		± 9 (Note 6)	
		± 2 (Note 7)	
Output current (B bus)	I_{OHB}/I_{OLB}	± 24 (Note 5)	mA
		± 18 (Note 6)	
		± 4 (Note 7)	
Operating temperature	T_{opr}	-40 to 85	$^{\circ}\text{C}$
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs and bus inputs must be tied to either V_{CC} or GND. Please connect both bus inputs and the bus outputs with V_{CC} or GND when the I/O of the bus terminal changes by the function. In this case, please note that the output is not short-circuited.

Note 2: Data retention only

Note 3: $V_{CC}=0\text{V}$, or output off state

Note 4: $\overline{OE}=\text{"L"}$, DIR="L"

Note 5: $V_{CC}=3.0$ to 3.6V

Note 6: $V_{CC}=2.3$ to 2.7V

Note 7: $V_{CC}=1.65$ to 1.95V

Note 8: $V_{IN}=0.8$ to 2.0V, $V_{CC}=3.0\text{V}$

Electrical Characteristics
DC Characteristics (Ta=-40 to 85°C, 2.7V<V_{CC} ≤ 3.6V)

Parameter		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
DC input voltage	H-level	V _{IH}	-		2.7 to 3.6	2.0	-	V
	L-level	V _{IL}	-		2.7 to 3.6	-	0.8	
Output voltage (A bus)	H-level	V _{OHA}	V _{IN} = V _{IH}	I _{OHA} =-100uA	2.7 to 3.6	V _{CC} -0.2	-	V
				I _{OH} =-6mA	2.7	2.2	-	
				I _{OH} =-9mA	3.0	2.4	-	
				I _{OH} =-12mA	3.0	2.2	-	
	L-level	V _{OLA}	V _{IN} = V _{IL}	I _{OLA} =100uA	2.7 to 3.6	-	0.2	
				I _{OL} =6mA	2.7	-	0.4	
				I _{OL} =9mA	3.0	-	0.4	
				I _{OL} =12mA	3.0	-	0.55	
Output voltage (B bus)	H-level	V _{OHB}	V _{IN} = V _{IH}	I _{OHB} =-100uA	2.7 to 3.6	V _{CC} -0.2	-	V
				I _{OHB} =-12mA	2.7	2.2	-	
				I _{OHB} =-18mA	3.0	2.4	-	
				I _{OHB} =-24mA	3.0	2.2	-	
	L-level	V _{OLB}	V _{IN} = V _{IL}	I _{OLB} =100uA	2.7 to 3.6	-	0.2	
				I _{OLB} =12mA	2.7	-	0.4	
				I _{OLB} =18mA	3.0	-	0.4	
				I _{OLB} =24mA	3.0	-	0.55	
Input leakage current(DIR,/OE)		I _{IN}	V _{IN} = 0 to 3.6 V		2.7 to 3.6	-	±5.0	μA
Power off leakage current		I _{OFF}	A,DIR,/OE= 0 to 3.6 V		0	-	5.0	μA
3-state output off-state current		I _{OZA}	V _{INA} = V _{IH} or V _{IL} V _{out} = 0 to 3.6V		2.7 to 3.6	-	±5.0	μA
		I _{OZB}	V _{INB} = V _{IH} or V _{IL} V _{out} = 0 or V _{CC}		2.7 to 3.6	-	±5.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		2.7 to 3.6	-	5.0	μA
Increase in ICC per input		ΔI _{CC}	V _{IN} = V _{CC} - 0.6 V (per input)		2.7 to 3.6	-	750	μA
Bushold input minimum drive hold current		I _{IHOLD}	V _{IN} = 0.8 V		3.0	75	-	μA
			V _{IN} = 2.0 V			-75	-	
Bushold input over-drive current to change state		I _{IOD}	V _{IN} = “L”→”H”		3.6	-	550	μA
			V _{IN} = “H”→”L”			-	-550	

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (Ta=-40 to 85°C, 2.3V ≤ V_{CC} ≤ 2.7V)

Parameter		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
DC input voltage	H-level	V _{IH}	-		2.3 to 2.7	1.6	-	V
	L-level	V _{IL}	-		2.3 to 2.7	-	0.7	
Output voltage (A bus)	H-level	V _{OHA}	V _{IN} = V _{IH}	I _{OHA} =-100uA	2.3 to 2.7	V _{CC} -0.2	-	V
				I _{OHA} =-3mA	2.3	2.0	-	
				I _{OHA} =-6mA	2.3	1.8	-	
				I _{OHA} =-9mA	2.3	1.7	-	
	L-level	V _{OLA}	V _{IN} = V _{IL}	I _{OLA} =100uA	2.3 to 2.7	-	0.2	
				I _{OLA} =6mA	2.3	-	0.4	
				I _{OLA} =9mA	2.3	-	0.6	
Output voltage (B bus)	H-level	V _{OHB}	V _{IN} = V _{IH}	I _{OHB} =-100uA	2.3 to 2.7	V _{CC} -0.2	-	V
				I _{OHB} =-6mA	2.3	2.0	-	
				I _{OHB} =-12mA	2.3	1.8	-	
				I _{OHB} =-18mA	2.3	1.7	-	
	L-level	V _{OLB}	V _{IN} = V _{IL}	I _{OLB} =100uA	2.3 to 2.7	-	0.2	
				I _{OLB} =12mA	2.3	-	0.4	
				I _{OLB} =18mA	2.3	-	0.6	
Input leakage current(DIR,/OE)		I _{IN}	V _{IN} = 0 to 3.6 V		2.3 to 2.7	-	±5.0	μA
Power off leakage current		I _{OFF}	A,DIR,/OE=0 to 3.6 V		0	-	5.0	μA
3-state output off-state current		I _{OZA}	V _{INA} =V _{IH} or V _{IL} V _{out} =0 to 3.6V		2.3 to 2.7	-	±5.0	μA
		I _{OZB}	V _{INB} =V _{IH} or V _{IL} V _{out} =0 or V _{CC}		2.3 to 2.7	-	±5.0	μA
Quiescent supply current		I _{CC}	V _{IN} =V _{CC} or GND		2.3 to 2.7	-	5.0	μA
Bushold input minimum drive hold current		I _{IHOLD}	V _{IN} = 0.7 V		2.3	45	-	μA
			V _{IN} = 1.6 V			-45	-	
Bushold input over-drive current to change state (Note)		I _{IOD}	V _{IN} = "L"→"H"		2.7	-	400	μA
			V _{IN} = "H"→"L"			-	-400	

Note: It is a necessary electric current to change the input in "L" or "H".

DC Characteristics (Ta=-40 to 85°C, 1.65V ≤ V_{CC}<2.3V)

Parameter		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
DC input voltage	H-level	V _{IH}	-		1.65 to 2.3	V _{CC} ×0.7	-	V
	L-level	V _{IL}	-		1.65 to 2.3	-	V _{CC} ×0.2	
Output voltage (A bus)	H-level	V _{OHA}	V _{IN} = V _{IH}	I _{OHA} =-100uA	1.65	V _{CC} -0.2	-	V
				I _{OHA} =-2mA	1.65	1.3	-	
	L-level	V _{OLA}	V _{IN} = V _{IL}	I _{OLA} =2mA	1.65	-	0.2	
Output voltage (B bus)	H-level	V _{OHB}	V _{IN} = V _{IH}	I _{OHB} =-100uA	1.65	V _{CC} -0.2	-	V
				I _{OHB} =-4mA	1.65	1.3	-	
	L-level	V _{OLB}	V _{IN} = V _{IL}	I _{OLB} =4mA	1.65	-	0.2	
Input leakage current(DIR,/OE)		I _{IN}	V _{IN} =0 to 3.6 V		1.65 to 2.3	-	±5.0	μA
Power off leakage current		I _{OFF}	A,DIR,/OE=0 to 3.6 V		0	-	5.0	μA
3-state output off-state current		I _{OZA}	V _{INA} =V _{IH} or V _{IL} V _{out} =0 to 3.6 V		1.65 to 2.3	-	±5.0	μA
		I _{OZB}	V _{INB} =V _{IH} or V _{IL} V _{out} =0 or V _{CC}		1.65 to 2.3	-	±5.0	μA
Quiescent supply current		I _{CC}	V _{IN} =V _{CC} or GND		1.65 to 2.3	-	5.0	μA
Bushold input minimum drive hold current		I _I (HOLD)	V _{IN} =0.33 V		1.65	20	-	μA
			V _{IN} =1.16 V			-20	-	
Bushold input over-drive current to change state (Note)		I _I (OD)	V _{IN} = “L”→”H”		1.95	-	300	μA
			V _{IN} = “H”→”L”			-	-300	

Note: It is a necessary electric current to change the input in "L" or "H".

AC Characteristics (Ta=-40 to 85°C, Input: $t_r = t_f = 2.0 \text{ ns}$, $C_L = 30 \text{ pF}$, $R_L = 500 \Omega$)

Parameter	Symbol	Test Condition	$V_{CC}(V)$	Min	Max	Unit
Propagation delay time	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8±0.15	1.0	10.0	ns
			2.5±0.2	0.8	4.6	
			3.3±0.3	0.6	3.0	
3-state output enable time	t_{pZL} t_{pZH}	Figure 1, Figure 3	1.8±0.15	1.0	15.0	ns
			2.5±0.2	0.8	7.8	
			3.3±0.3	0.6	5.6	
3-state output disable time	t_{pLZ} t_{pHZ}	Figure 1, Figure 3	1.8±0.15	1.0	6.5	ns
			2.5±0.2	0.8	4.3	
			3.3±0.3	0.6	3.9	
Output to output skew	t_{osLH} t_{osHL}	(Note)	1.8±0.15	-	0.5	ns
			2.5±0.2	-	0.5	
			3.3±0.3	-	0.5	

For $C_L=50\text{pF}$, add approximately 300ps to the AC maximum specification.

Note: Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Capacitive Characteristics (Ta=25°C)

Characteristics	Symbol	Test Condition	$V_{CC}(V)$	Typ.	Unit
Input capacitance	C_{IN}		1.8,2.5,3.3	6	pF
Bus I/O capacitance	$C_{I/O}$		1.8,2.5,3.3	7	pF
Power dissipation capacitance (A bus input)	C_{PDA}	$\overline{OE} = "L"$, $f_{INA}=100\text{MHz}$ Table 1 (Note)	1.8,2.5,3.3	20	pF
		$\overline{OE} = "H"$, $f_{INA}=100\text{MHz}$ Table 1 (Note)		0	pF
Power dissipation capacitance (B bus input)	C_{PDB}	$\overline{OE} = "L"$, $f_{INB}=100\text{MHz}$ Table 1 (Note)	1.8,2.5,3.3	16	pF
		$\overline{OE} = "H"$, $f_{INB}=100\text{MHz}$ Table 1 (Note)		1	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot V_{IN} + I_{CC}/8(\text{per bit})$$

Table1 CPD Test Condition

[illegible]

Symbol explanation-

$$V = V_{CC}(+3.3V)$$

G = GND (0V)

H = Logic 1 (VCC)

L = Logic 0 (GND)

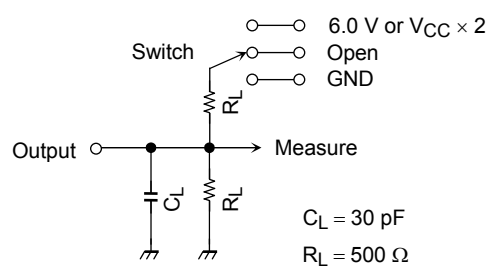
X = Don't care(Fixed to V_{CC} or GND)

O = Open

C = Connect a condenser(30pF) between output terminal and GND.

P = Input pulse with 50% duty cycle.

AC Test Circuit



Parameter	Switch
t _{pLH} , t _{pHL}	Open
t _{pLZ} , t _{pZL}	6.0 V @V _{CC} = 3.3 ± 0.3 V V _{CC} × 2 @V _{CC} = 2.5 ± 0.2 V @V _{CC} = 1.8 ± 0.15 V
t _{pHZ} , t _{pZH}	GND

Figure 1

AC Waveform

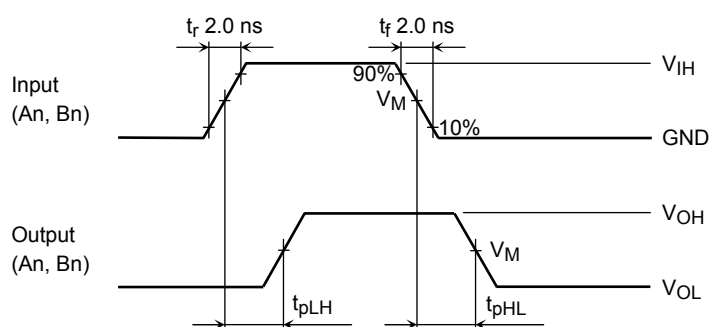
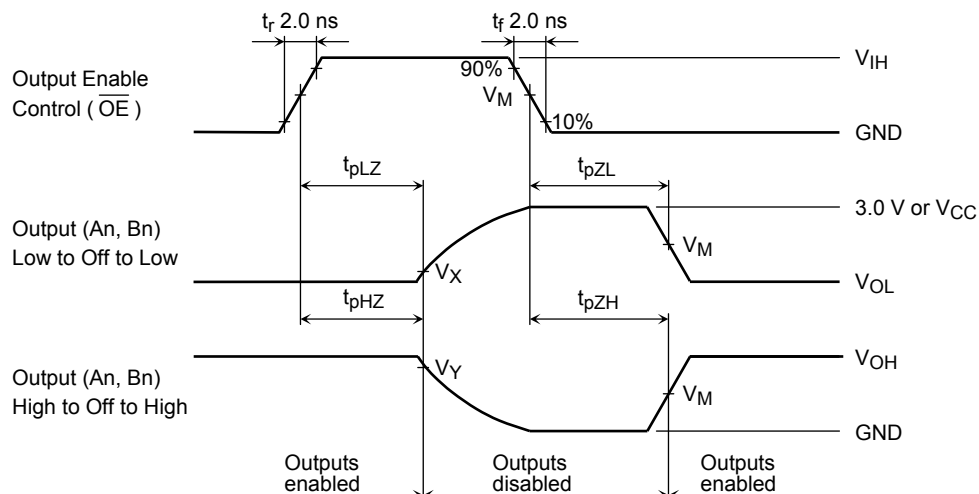


Figure 2 t_{pLH} , t_{pHL}

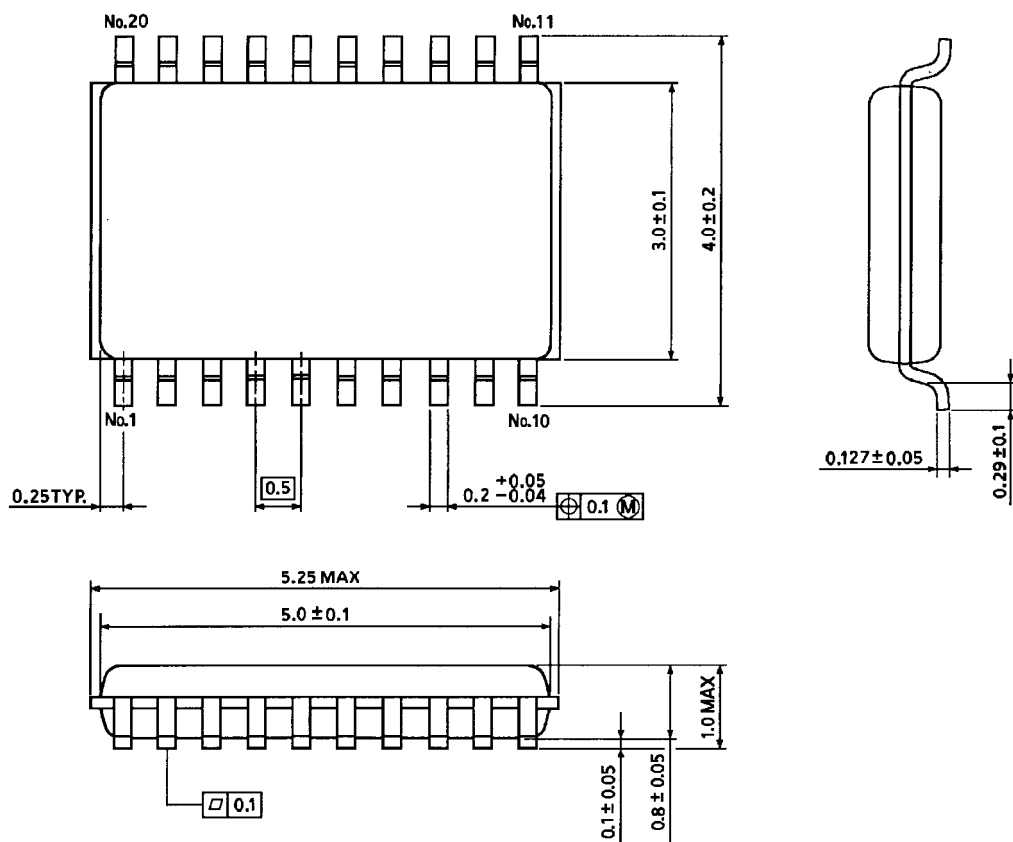

Figure 3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 ± 0.15 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V	$V_{OL} + 0.15$ V
V_Y	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V	$V_{OH} - 0.15$ V

Package Dimensions

VSSOP20-P-0030-0.50

Unit : mm

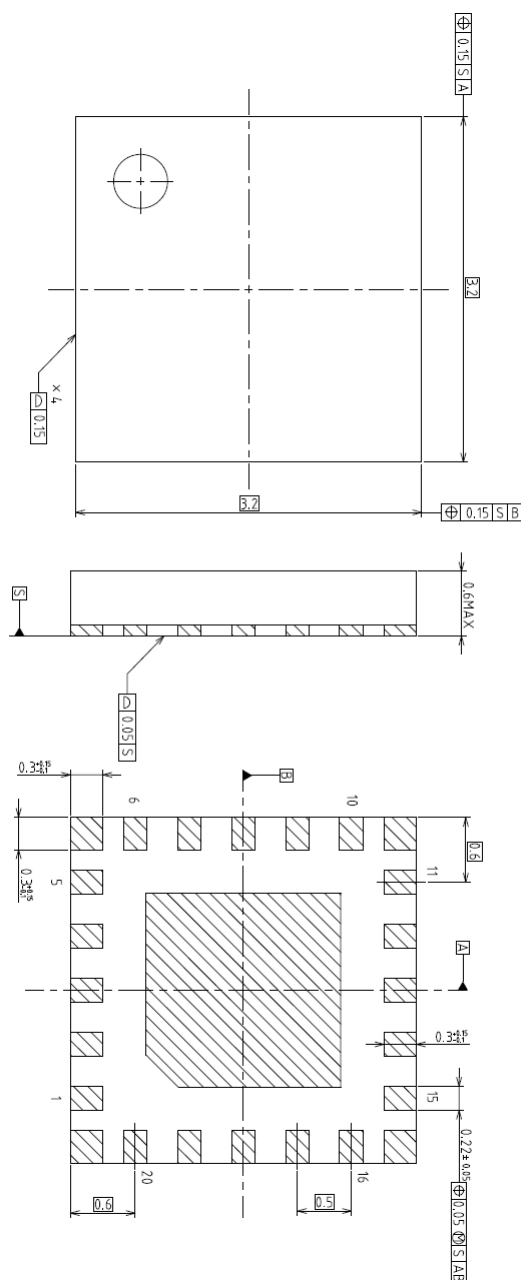


Weight: 0.03 g (typ.)

Package Dimensions

Unit : mm

VQON20-P-0404-0.5



Weight: 0.0145 g (typ.)

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