

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC373F, TC74VHC373FK

## Octal D-Type Latch with 3-State Output

The TC74VHC373 is an advanced high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

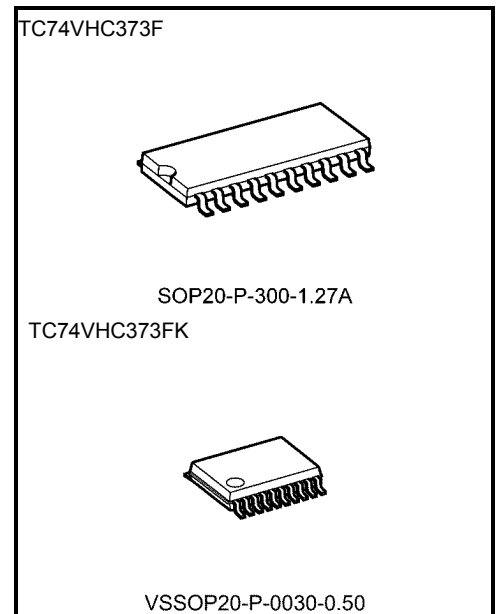
This 8-bit D-type latch is controlled by a latch enable input (LE) and an output enable input ( $\overline{OE}$ ).

When the  $\overline{OE}$  input is high, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## Features

- High speed:  $t_{pd} = 5.0 \text{ ns (typ.)}$  at  $V_{CC} = 5 \text{ V}$
- Low power dissipation:  $I_{CC} = 4 \text{ }\mu\text{A (max)}$  at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC}(\text{opr}) = 2 \text{ to } 5.5 \text{ V}$
- Low noise:  $V_{OLP} = 0.8 \text{ V (max)}$
- Pin and function compatible with 74ALS373

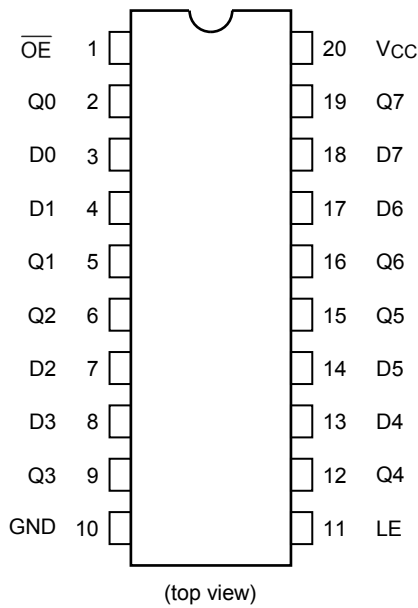


### Weight

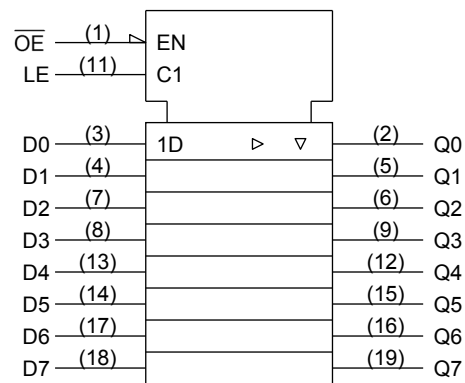
SOP20-P-300-1.27A	: 0.22 g (typ.)
VSSOP20-P-0030-0.50	: 0.03 g (typ.)

Start of commercial production  
1991-05

### Pin Assignment



### IEC Logic Symbol



### Truth Table

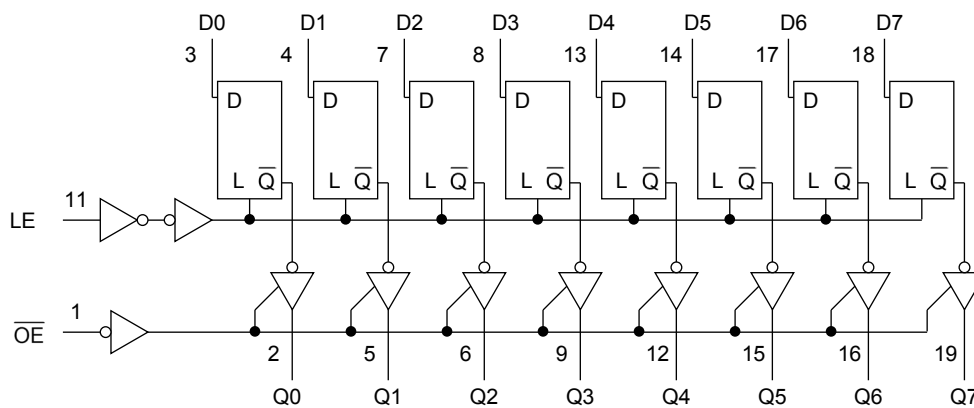
Inputs			Output
$\overline{OE}$	LE	D	
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Qn: Q outputs are latched at the time when the LE input is taken to a low logic level.

### System Diagram



### Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V <sub>CC</sub>	-0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	-0.5 to 7.0	V
DC output voltage	V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5	V
Input diode current	I <sub>IK</sub>	-20	mA
Output diode current	I <sub>OK</sub>	±20	mA
DC output current	I <sub>OUT</sub>	±25	mA
DC V <sub>CC</sub> /ground current	I <sub>CC</sub>	±75	mA
Power dissipation	P <sub>D</sub>	180	mW
Storage temperature	T <sub>stg</sub>	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.  
 Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.  
 Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	2.0 to 5.5	V
Input voltage	V <sub>IN</sub>	0 to 5.5	V
Output voltage	V <sub>OUT</sub>	0 to V <sub>CC</sub>	V
Operating temperature	T <sub>opr</sub>	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V <sub>CC</sub> = 3.3 ± 0.3 V) 0 to 20 (V <sub>CC</sub> = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
 Unused inputs must be tied to either V<sub>CC</sub> or GND.

### Electrical Characteristics

#### DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				V <sub>CC</sub> (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V <sub>IH</sub>	—	2.0 3.0 to 5.5	1.50 V <sub>CC</sub> × 0.7	— —	— —	1.50 V <sub>CC</sub> × 0.7	— —	V	
Low-level input voltage	V <sub>IL</sub>	—	2.0 3.0 to 5.5	— —	— —	0.50 V <sub>CC</sub> × 0.3	— —	0.50 V <sub>CC</sub> × 0.3	V	
High-level output voltage	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —	V
			I <sub>OH</sub> = -4 mA	3.0	2.58	—	—	2.48	—	
			I <sub>OH</sub> = -8 mA	4.5	3.94	—	—	3.80	—	
Low-level output voltage	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 μA	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I <sub>OL</sub> = 4 mA	3.0	—	—	0.36	—	0.44	
			I <sub>OL</sub> = 8 mA	4.5	—	—	0.36	—	0.44	
3-state output off-state current	I <sub>OZ</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND	5.5	—	—	±0.25	—	±2.50	μA	
Input leakage current	I <sub>IN</sub>	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5	—	—	±0.1	—	±1.0	μA	
Quiescent supply current	I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5	—	—	4.0	—	40.0	μA	

#### Timing Requirements (input: tr = tf = 3 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = -40 to 85°C	Unit
				V <sub>CC</sub> (V)	Typ.	Limit	
Minimum pulse width (LE)	t <sub>w</sub> (H)	—	3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	ns
Minimum set-up time	t <sub>s</sub>	—	3.3 ± 0.3 5.0 ± 0.5	— —	4.0 4.0	4.0 4.0	ns
Minimum hold time	t <sub>h</sub>	—	3.3 ± 0.3 5.0 ± 0.5	— —	1.0 1.0	1.0 1.0	ns

### AC Electrical Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
		VCC (V)	CL (pF)	Min	Typ.	Max	Min	Max		
Propagation delay time (LE-Q)	$t_{pLH}$	—	$3.3 \pm 0.3$	15	—	7.0	11.0	1.0	13.0	ns
				50	—	9.5	14.5	1.0	16.5	
	$5.0 \pm 0.5$		15	—	4.9	7.2	1.0	8.5		
			50	—	6.4	9.2	1.0	10.5		
Propagation delay time (D-Q)	$t_{pLH}$	—	$3.3 \pm 0.3$	15	—	7.3	11.4	1.0	13.5	ns
				50	—	9.8	14.9	1.0	17.0	
	$5.0 \pm 0.5$		15	—	5.0	7.2	1.0	8.5		
			50	—	6.5	9.2	1.0	10.5		
3-state output enable time	$t_{pZL}$	$R_L = 1 \text{ k}\Omega$	$3.3 \pm 0.3$	15	—	7.3	11.4	1.0	13.5	ns
				50	—	9.8	14.9	1.0	17.0	
	$5.0 \pm 0.5$		15	—	5.5	8.1	1.0	9.5		
			50	—	7.0	10.1	1.0	11.5		
3-state output disable time	$t_{pLZ}$	$R_L = 1 \text{ k}\Omega$	$3.3 \pm 0.3$	50	—	9.5	13.2	1.0	15.0	ns
			$5.0 \pm 0.5$	50	—	6.5	9.2	1.0	10.5	
Output to output skew	$t_{osLH}$	(Note 1)	$3.3 \pm 0.3$	50	—	—	1.5	—	1.5	ns
			$5.0 \pm 0.5$	50	—	—	1.0	—	1.0	
Input capacitance	$C_{IN}$	—		—	4	10	—	10	pF	
Output capacitance	$C_{OUT}$	—		—	6	—	—	—	pF	
Power dissipation capacitance	$C_{PD}$	—		(Note 2)	—	27	—	—	pF	

Note 1: Parameter guaranteed by design.

$$t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|$$

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per latch)}$$

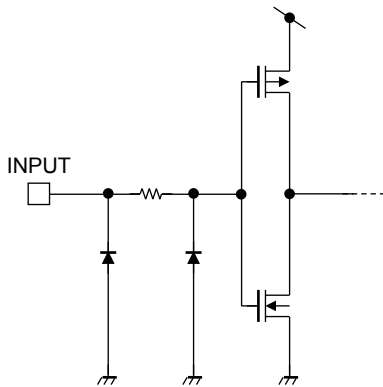
And the total CPD when n pcs. of Latch operate can be gained by the following equation:

$$C_{PD}(\text{total}) = 14 + 13 \cdot n$$

### Noise Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V <sub>CC</sub> (V)	Typ.	Max	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	0.5	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-0.5	-0.8	V
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

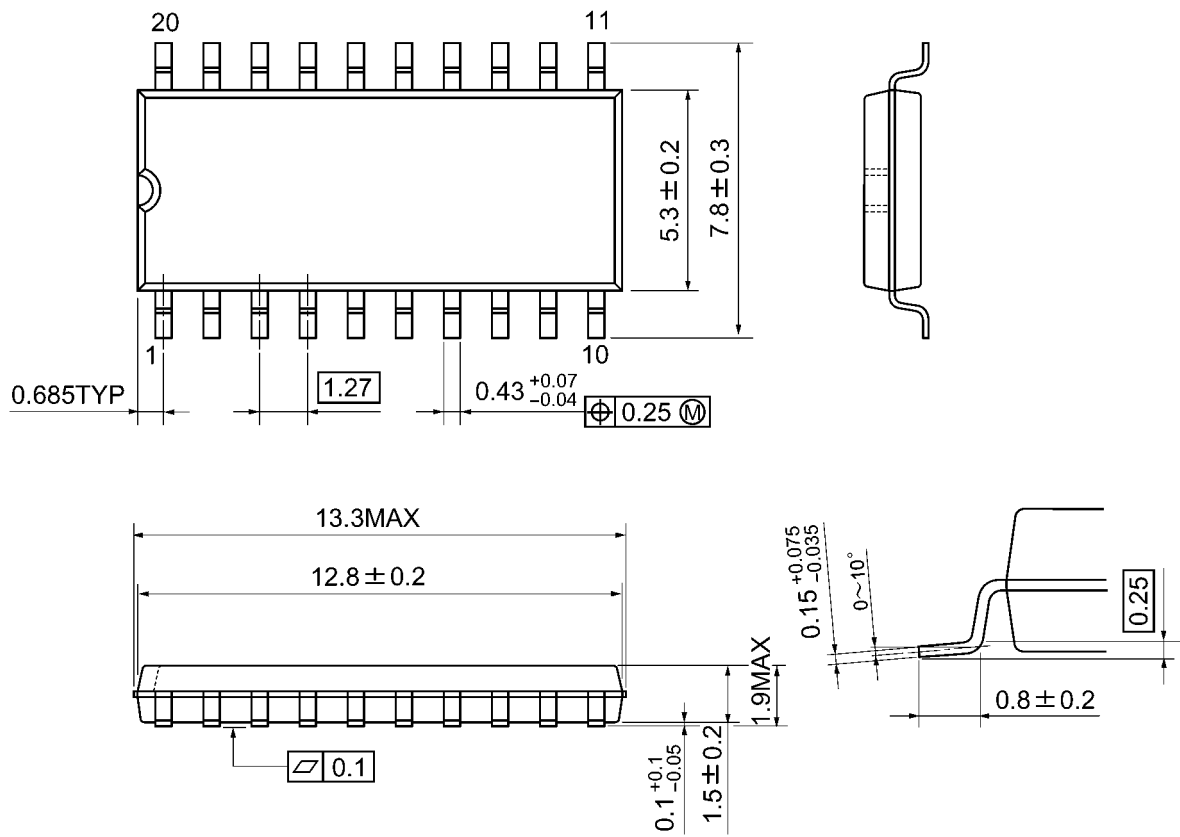
### Input Equivalent Circuit



### Package Dimensions

SOP20-P-300-1.27A

Unit: mm

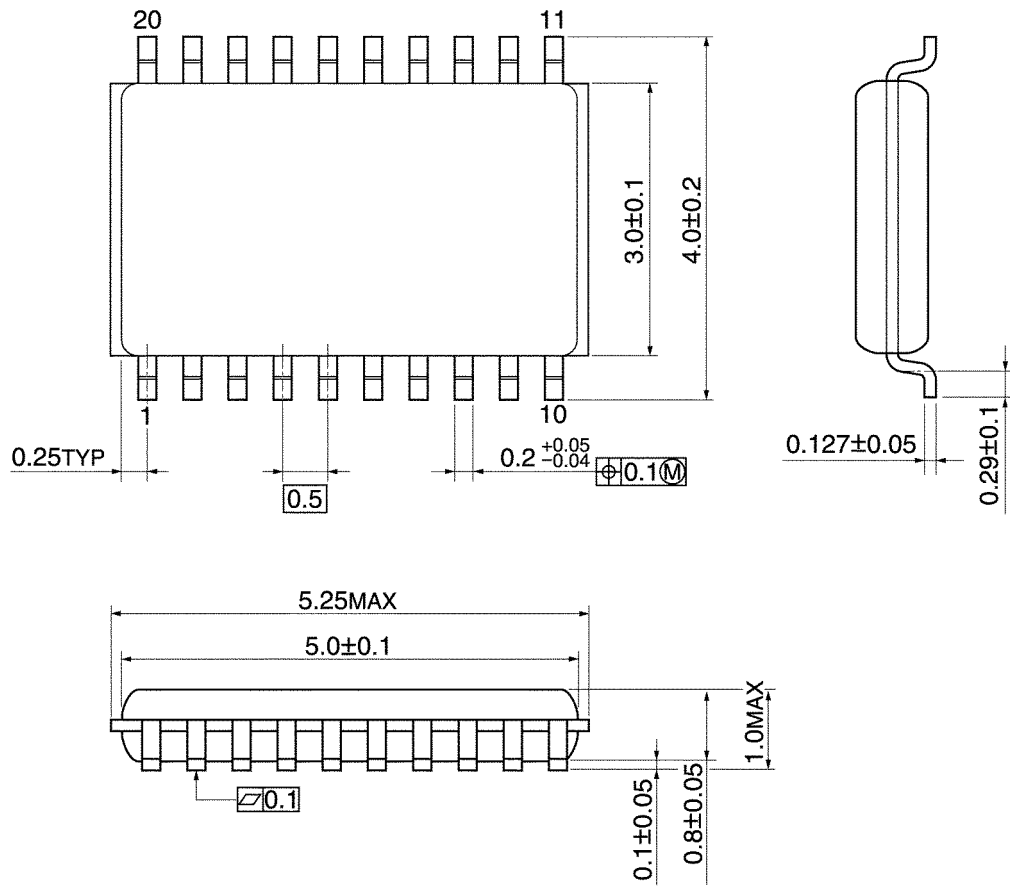


Weight: 0.22 g (typ.)

### Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)



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