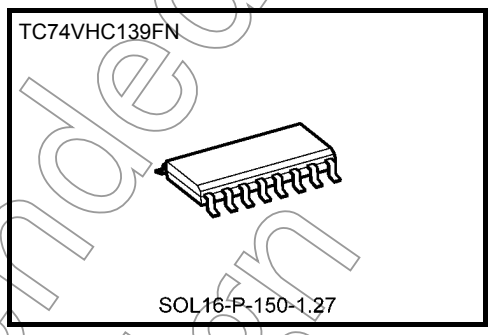
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC139FN

## Dual 2-to-4 Line Decoder

Note: xxxFN (JEDEC SOP) is not available in Japan.




Weight
SOL16-P-150-1.27 : 0.13 g (typ.)

The TC74VHC139 is an advanced high speed CMOS 2 to 4 LINE DECODER/DEMULTIPLEXER fabricated with silicon gate C2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The active low enable input can be used for gating or it can be used as a data input for demultiplexing applications.

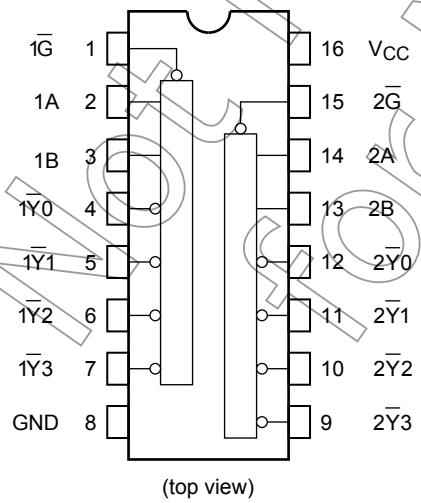
When the enable input is held High, all four outputs are fixed at a high logic level independent of the other inputs.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## Features

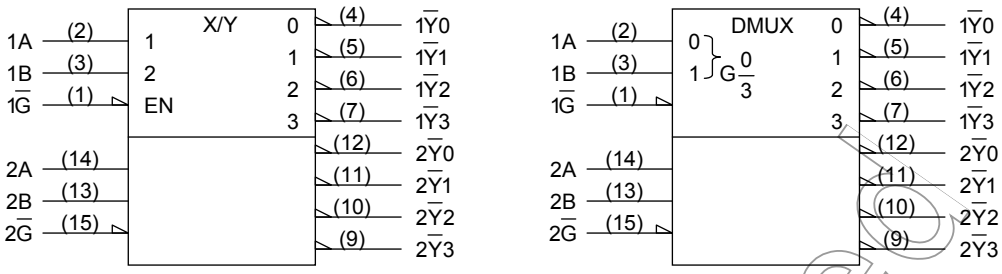
- High speed: $t_{pd}$ = 5.0 ns (typ.) at $V_{CC}$ = 5 V
- Low power dissipation: $I_{CC}$ = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% $V_{CC\ (min)}$
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC\ (opr)}$ = 2 V to 5.5 V
- Pin and function compatible with 74ALS139

## Pin Assignment




(top view)

## IEC Logic Symbol

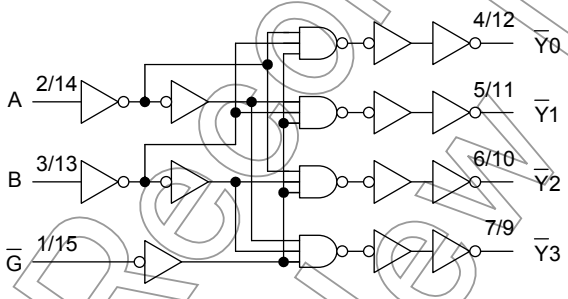



## Truth Table

| Inputs | | | Outputs | | | | Selected Output |
|---|---|---|---|---|---|---|---|
| Enable | Select | | $\overline{Y}0$ | $\overline{Y}1$ | $\overline{Y}2$ | $\overline{Y}3$ | |
| $\overline{G}$ | B | A | | | | | |
| H | X | X | H | H | H | H | None |
| L | L | L | L | H | H | H | $\overline{Y}0$ |
| L | L | H | H | L | H | H | $\overline{Y}1$ |
| L | H | L | H | H | L | H | $\overline{Y}2$ |
| L | H | H | H | H | H | L | $\overline{Y}3$ |

X: Don't care

## System Diagram




## Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage range | $V_{CC}$ | −0.5 to 7.0 | V |
| DC input voltage | $V_{IN}$ | −0.5 to 7.0 | V |
| DC output voltage | $V_{OUT}$ | −0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | −20 | mA |
| Output diode current | $I_{OK}$ | ±20 | mA |
| DC output current | $I_{OUT}$ | ±25 | mA |
| DC $V_{CC}$/ground current | $I_{CC}$ | ±75 | mA |
| Power dissipation | $P_D$ | 180 | mW |
| Storage temperature | $T_{stg}$ | −65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.0 to 5.5 | V |
| Input voltage | $V_{IN}$ | 0 to 5.5 | V |
| Output voltage | $V_{OUT}$ | 0 to VCC | V |
| Operating temperature | $T_{opr}$ | −40 to 85 | °C |
| Input rise and fall time | dt/dv | 0 to 100 ($V_{CC}$ = 3.3 ± 0.3 V)<br>0 to 20 ($V_{CC}$ = 5 ± 0.5 V) | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either $V_{CC}$ or GND.

## Electrical Characteristics

### DC Characteristics

| Characteristics | Symbol | Test Condition | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | $V_{CC}$ (V) | Min | Typ. | Max | Min | Max | |
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | — | 1.50 | — | V |
| | | | | 3.0 to 5.5 | $V_{CC}$ × 0.7 | — | — | $V_{CC}$ × 0.7 | — | |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | — | 0.50 | — | 0.50 | V |
| | | | | 3.0 to 5.5 | — | — | $V_{CC}$ × 0.3 | — | $V_{CC}$ × 0.3 | |
| High-level output voltage | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −50 μA | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V |
| | | | | 3.0 | 2.9 | 3.0 | — | 2.9 | — | |
| | | | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | |
| | | | $I_{OH}$ = −4 mA | 3.0 | 2.58 | — | — | 2.48 | — | |
| | | | $I_{OH}$ = −8 mA | 4.5 | 3.94 | — | — | 3.80 | — | |
| Low-level output voltage | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V |
| | | | | 3.0 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 3.0 | — | — | 0.36 | — | 0.44 | |
| | | | $I_{OL}$ = 8 mA | 4.5 | — | — | 0.36 | — | 0.44 | |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = 5.5 V or GND | | 0 to 5.5 | — | — | ±0.1 | — | ±1.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 5.5 | — | — | 4.0 | — | 40.0 | μA |

### AC Characteristics (input: $t_r = t_f = 3$ ns)

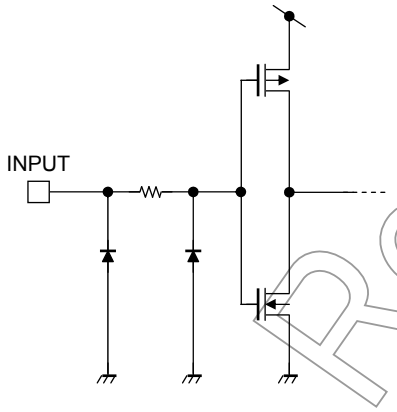
| Characteristics | Symbol | Test Condition | | | Ta = 25°C | | | Ta = −40 to 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ (V) | $C_L$ (pF) | Min | Typ. | Max | Min | Max | |
| Propagation delay time (A, B-Y) | $t_{pLH}$ $t_{pHL}$ | — | 3.3 ± 0.3 | 15 | — | 7.2 | 11.0 | 1.0 | 13.0 | ns |
| | | | | 50 | — | 9.7 | 14.5 | 1.0 | 16.5 | |
| | | | 5.0 ± 0.5 | 15 | — | 5.0 | 7.2 | 1.0 | 8.5 | |
| | | | | 50 | — | 6.5 | 9.2 | 1.0 | 10.5 | |
| Propagation delay time ($\overline{G}$-Y) | $t_{pLH}$ $t_{pHL}$ | — | 3.3 ± 0.3 | 15 | — | 6.4 | 9.2 | 1.0 | 11.0 | ns |
| | | | | 50 | — | 8.9 | 12.7 | 1.0 | 14.5 | |
| | | | 5.0 ± 0.5 | 15 | — | 4.4 | 6.3 | 1.0 | 7.5 | |
| | | | | 50 | — | 5.9 | 8.3 | 1.0 | 9.5 | |
| Input capacitance | $C_{IN}$ | — | | | — | 4 | 10 | — | 10 | pF |
| Power dissipation capacitance | $C_{PD}$ | (Note) | | | — | 26 | — | — | — | pF |

Note: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

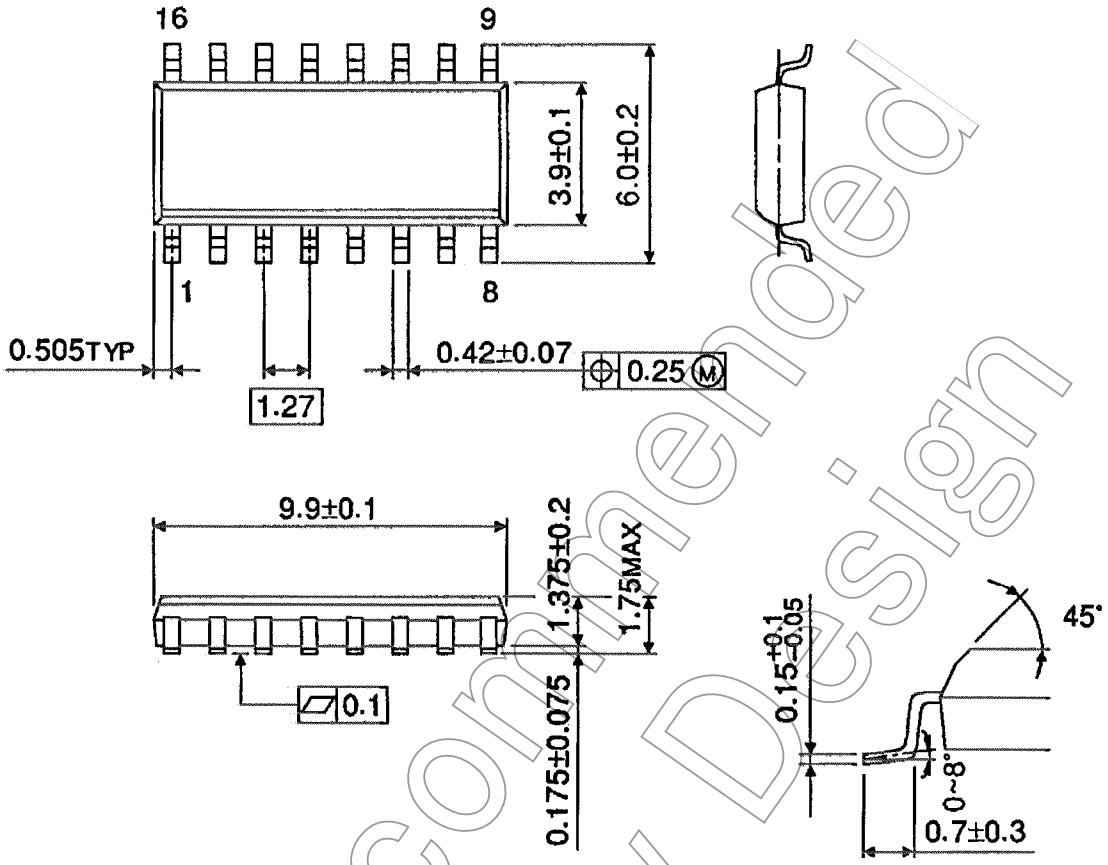
$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per decoder)}$$

## Input Equivalent Circuit



## Package Dimensions (Note)

SOL16-P-150-1.27 Unit : mm




Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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