

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74LCX74F, TC74LCX74FK

Low-Voltage Dual D-Type Flip-Flop with 5-V Tolerant Inputs and Outputs

The TC74LCX74 is a high-performance CMOS D-type flip-flop. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

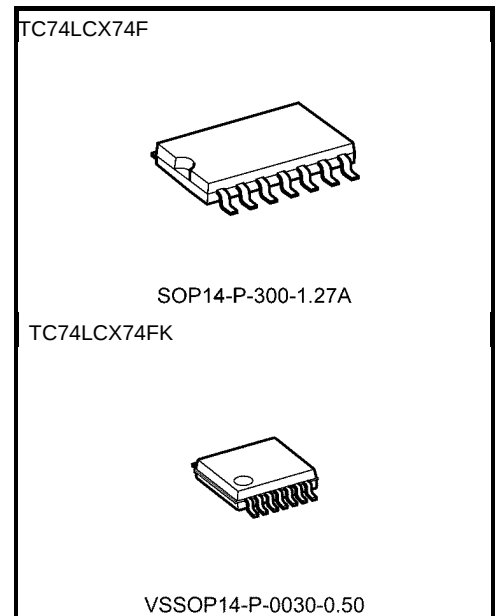
The device is designed for low-voltage (3.3 V) V_{CC} applications, but it could be used to interface to 5-V supply environment for inputs.

The signal level applied to the D input is transferred to Q output during the positive going transition of the CK pulse. $\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input low.

All inputs are equipped with protection circuits against static discharge.

Features

- Low-voltage operation: $V_{CC} = 1.65$ to 3.6 V
- High-speed operation: $t_{pd} = 7.0$ ns (max) ($V_{CC} = 3.0$ to 3.6 V)
- Output current: $|I_{OH}|/I_{OL} = 24$ mA (min) ($V_{CC} = 3.0$ V)
- Latch-up performance: $> \pm 500$ mA
- Available in JEITA SOP, VSSOP (US)
- Power-down protection is provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 74 type



Weight

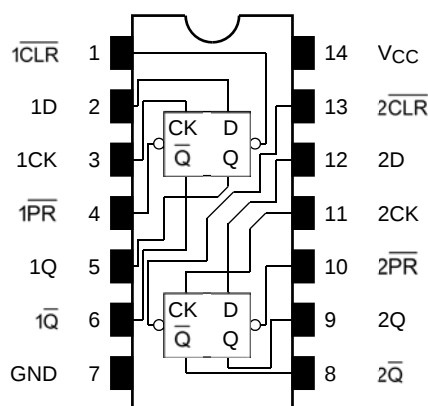
SOP14-P-300-1.27A : 0.18 g (typ.)

VSSOP14-P-0030-0.50 : 0.02 g (typ.)

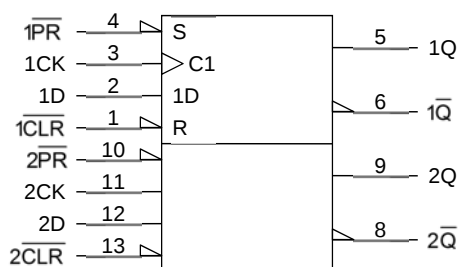
Note: The Electrical Characteristics of $V_{CC} = 1.8 \pm 0.15$ V is only applicable for products which manufactured from January 2009 onward.

Start of commercial production
1994-10

Pin Assignment (top view)



IEC Logic Symbol



Truth Table

Inputs				Outputs		Function
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Qn	Q̄n	No change

X: Don't care

Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	−0.5 to 7.0	V
DC input voltage	V _{IN}	−0.5 to 7.0	V
DC output voltage	V _{OUT}	−0.5 to 7.0 (Note 2)	V
		−0.5 to V _{CC} + 0.5 (Note 3)	
Input diode current	I _{IK}	−50	mA
Output diode current	I _{OK}	±50 (Note 4)	mA
DC output current	I _{OUT}	±50	mA
Power dissipation	P _D	180	mW
DC V _{CC} /ground current	I _{CC} /I _{GND}	±100	mA
Storage temperature	T _{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: V_{CC} = 0 V

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V _{CC}	1.65 to 3.6	V
		1.5 to 3.6 (Note 2)	
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to 5.5 (Note 3)	V
		0 to V _{CC} (Note 4)	
Output current	I _{OH} /I _{OL}	±24 (Note 5)	mA
		±12 (Note 6)	
Operating temperature	T _{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either V_{CC} or GND.

Note 2: Data retention only

Note 3: V_{CC} = 0 V

Note 4: High or low state

Note 5: V_{CC} = 3.0 to 3.6 V

Note 6: V_{CC} = 2.7 to 3.0 V

Note 7: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition		V _{CC} (V)	Min	Max	Unit
Input voltage	H-level	V _{IH}	—		1.65 to 2.3	V _{CC} × 0.9	—	V
					2.3 to 2.7	1.7	—	
					2.7 to 3.6	2.0	—	
	L-level	V _{IL}	—		1.65 to 2.3	—	V _{CC} × 0.1	
					2.3 to 2.7	—	0.7	
					2.7 to 3.6	—	0.8	
Output voltage	H-level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = −100 μA	1.65 to 3.6	V _{CC} −0.2	—	V
				I _{OH} = −4 mA	1.65	1.05	—	
				I _{OH} = −8 mA	2.3	1.7	—	
				I _{OH} = −12 mA	2.7	2.2	—	
				I _{OH} = −18 mA	3.0	2.4	—	
				I _{OH} = −24 mA	3.0	2.2	—	
	L-level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100 μA	1.65 to 3.6	—	0.2	
				I _{OL} = 4 mA	1.65	—	0.45	
				I _{OL} = 8 mA	2.3	—	0.7	
				I _{OL} = 12 mA	2.7	—	0.4	
				I _{OL} = 16 mA	3.0	—	0.4	
				I _{OL} = 24 mA	3.0	—	0.55	
Input leakage current		I _{IN}	V _{IN} = 0 to 5.5 V		1.65 to 3.6	—	±5.0	μA
Power-off leakage current		I _{OFF}	V _{IN} /V _{OUT} = 5.5 V		0	—	10.0	μA
Quiescent supply current		I _{CC}	V _{IN} = V _{CC} or GND		1.65 to 3.6	—	10.0	μA
			V _{IN} = 3.6 to 5.5 V		1.65 to 3.6	—	±10.0	
Increase in I _{CC} per input		ΔI _{CC}	V _{IH} = V _{CC} − 0.6 V (per 1 input)		2.7 to 3.6	—	500	

AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V _{CC} (V)	Min	Max	Unit
Maximum clock frequency	f _{max}	Figure 1, Figure 2	1.8 ± 0.15	50	—	MHz
			2.5 ± 0.2	100	—	
			2.7	100	—	
			3.3 ± 0.3	150	—	
Propagation delay time (CK-Q, $\bar{Q}$)	t _{PLH} t _{PHL}	Figure 1, Figure 2	1.8 ± 0.15	—	22.0	ns
			2.5 ± 0.2	—	9.0	
			2.7	—	8.0	
			3.3 ± 0.3	1.5	7.0	
Propagation delay time ($\bar{CLR}$, $\overline{PR}$ -Q, $\bar{Q}$)	t _{PLH} t _{PHL}	Figure 1, Figure 4	1.8 ± 0.15	—	22.0	ns
			2.5 ± 0.2	—	9.0	
			2.7	—	8.0	
			3.3 ± 0.3	1.5	7.0	
Minimum pulse width (CK)	t _w (H) t _w (L)	Figure 1, Figure 2	1.8 ± 0.15	10.0	—	ns
			2.5 ± 0.2	5.0	—	
			2.7	3.3	—	
			3.3 ± 0.3	3.3	—	
Minimum pulse width ($\bar{CLR}$, $\overline{PR}$)	t _w (L)	Figure 1, Figure 4	1.8 ± 0.15	10.0	—	ns
			2.5 ± 0.2	5.0	—	
			2.7	3.6	—	
			3.3 ± 0.3	3.3	—	
Minimum setup time	t _s	Figure 1, Figure 2	1.8 ± 0.15	10.0	—	ns
			2.5 ± 0.2	5.0	—	
			2.7	2.5	—	
			3.3 ± 0.3	2.5	—	
Minimum hold time	t _h	Figure 1, Figure 2	1.8 ± 0.15	1.5	—	ns
			2.5 ± 0.2	1.5	—	
			2.7	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum removal time	t _{rem}	Figure 1, Figure 3	1.8 ± 0.15	10.0	—	ns
			2.5 ± 0.2	5.0	—	
			2.7	3.0	—	
			3.3 ± 0.3	2.5	—	
Output to output skew	t _{osLH} t _{osHL}	(Note)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

Note: Parameter guaranteed by design.
 (t_{osLH} = |t_{PLHm} - t_{PLHn}|, t_{osHL} = |t_{PHLm} - t_{PHLn}|)

Dynamic Switching Characteristics (Ta = 25°C, input: tr = tf = 2.5 ns, CL = 50 pF, RL = 500 Ω)

Characteristics	Symbol	Test Condition	VCC (V)	Typ.	Unit
Quiet output maximum dynamic VOL	VOLP	VIH = 3.3 V, VIL = 0 V	3.3	0.8	V
Quiet output minimum dynamic VOL	VOLV	VIH = 3.3 V, VIL = 0 V	3.3	0.8	V

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	VCC (V)	Typ.	Unit
Input capacitance	CIN	—	3.3	7	pF
Output capacitance	COUT	—	0	8	pF
Power dissipation capacitance	CPD	fIN = 10 MHz (Note)	3.3	25	pF

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC} (opr) = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per bit)}$$

AC Test Circuit

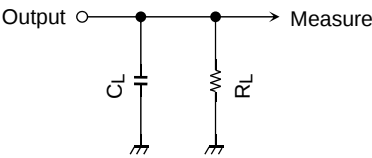


Figure 1

AC Waveform

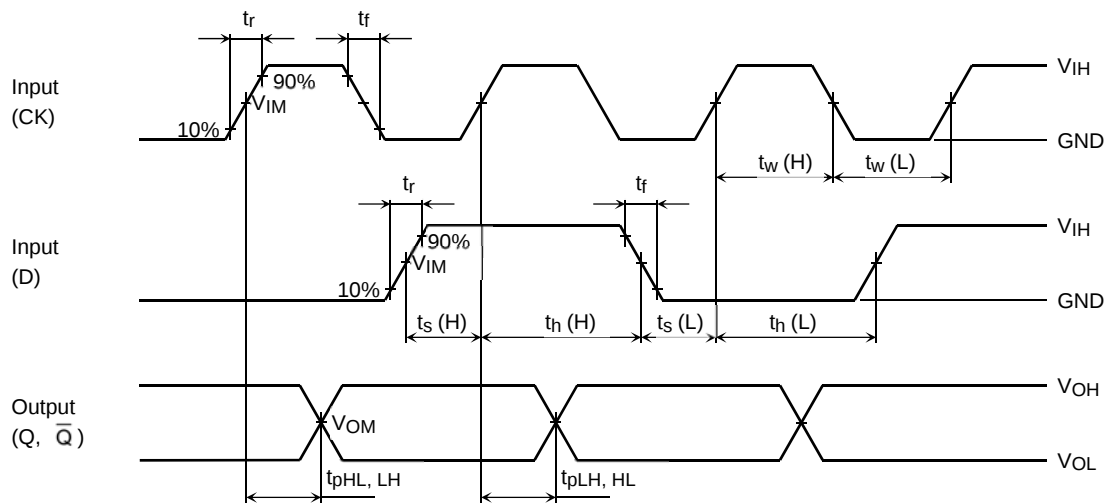


Figure 2 t_{pLH} , t_{pHL} , t_w , t_s , t_h

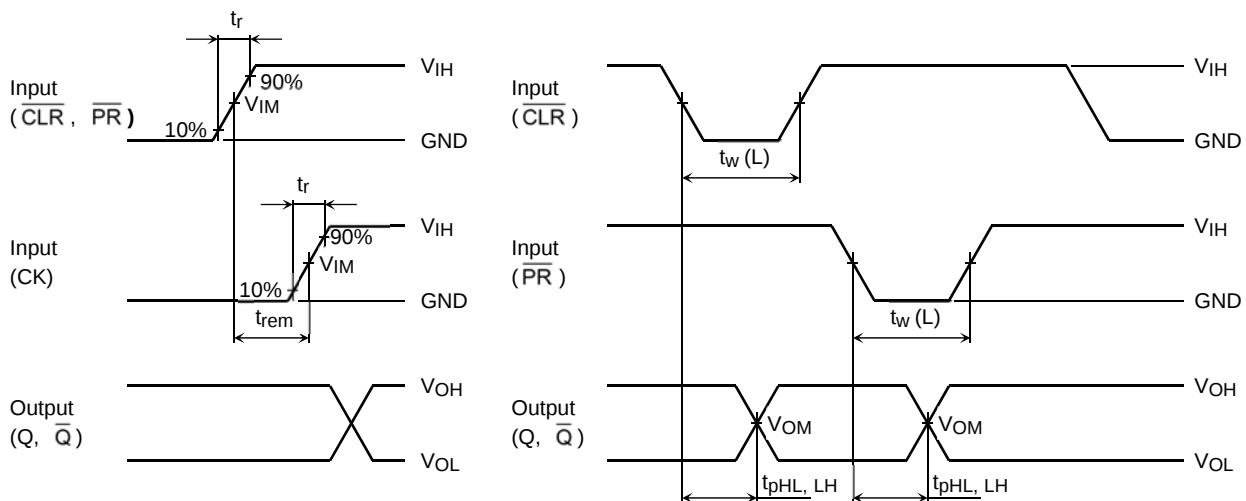


Figure 3 t_{rem}

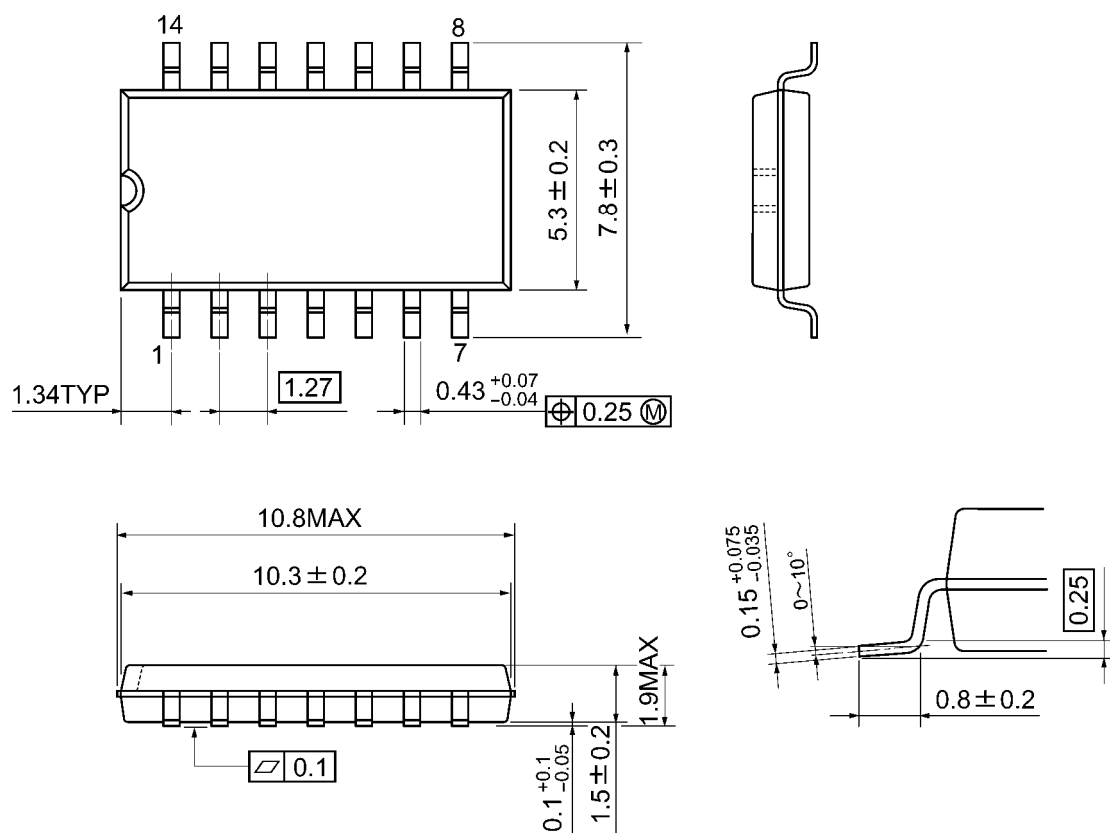
Figure 4 t_{pLH} , t_{pHL}

	Symbol	V_{CC}		
		$3.3 \pm 0.3 \text{ V}$ 2.7 V	$2.5 \pm 0.2 \text{ V}$	$1.8 \pm 0.15 \text{ V}$
Input	V_{IH}	2.7 V	V_{CC}	V_{CC}
	V_{IM}	1.5 V	$V_{CC}/2$	$V_{CC}/2$
	t_r , t_f	2.5 ns	2.0 ns	2.0 ns
Output	V_{OM}	1.5 V	$V_{OH}/2$	$V_{OH}/2$
Load	C_L	50 pF	30 pF	30 pF
	R_L	500 Ω	500 Ω	1 k Ω

Package Dimensions

SOP14-P-300-1.27A

Unit: mm

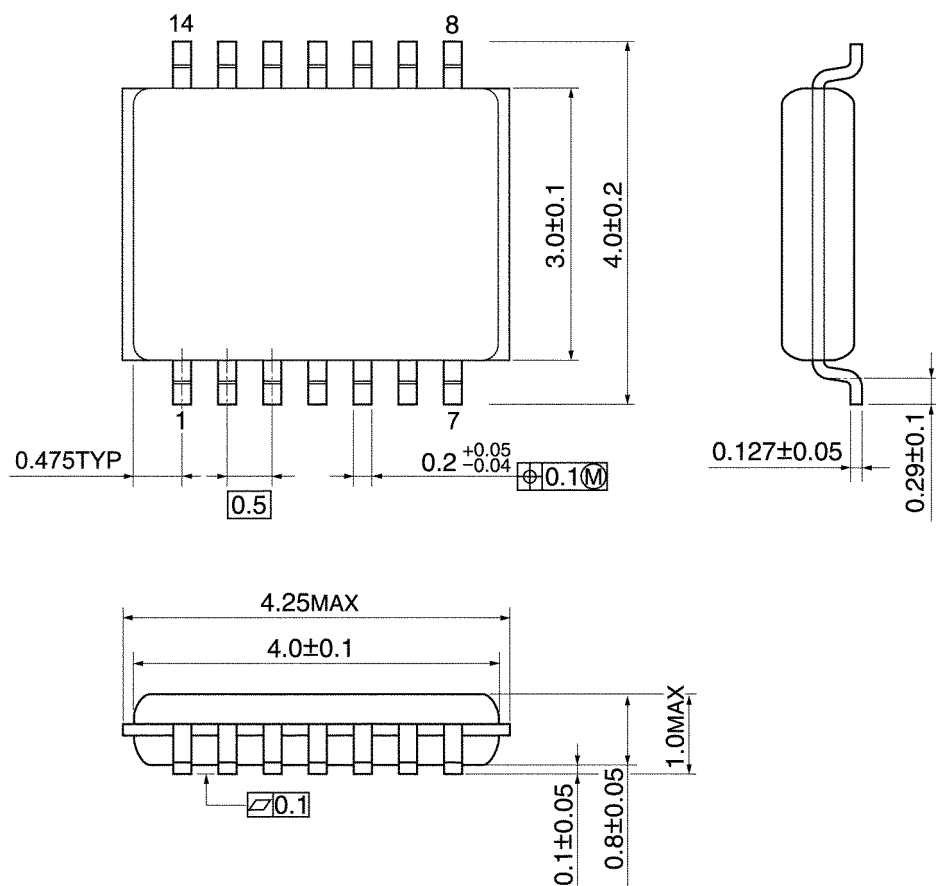


Weight: 0.18 g (typ.)

Package Dimensions

VSSOP14-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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