

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74LCX273F, TC74LCX273FK

Low-Voltage Octal D-Type Flip-Flop with Clear with 5-V Tolerant Inputs and Outputs

The TC74LCX273 is a high-performance CMOS octal D-type flip-flop. Designed for use in 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low-power dissipation.

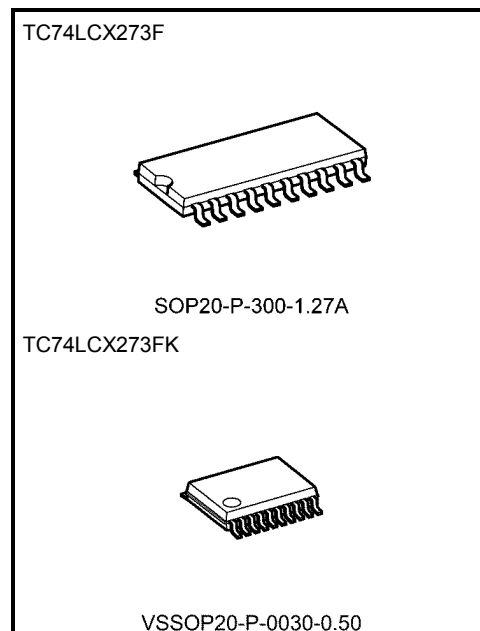
The device is designed for low-voltage (3.3 V)  $V_{CC}$  applications, but it could be used to interface to 5-V supply environment for both inputs and outputs.

This 8 bit D-type flip-flop is controlled by a clock input (CK) and a clear input ( $\overline{CLR}$ ). When the  $\overline{CLR}$  input is low, the eight outputs are at a low logic level.

All inputs are equipped with protection circuits against static discharge.

## Features

- Low-voltage operation:  $V_{CC} = 1.65$  to  $3.6$  V
- High-speed operation:  $t_{pd} = 8.5$  ns (max) ( $V_{CC} = 3.0$  to  $3.6$  V)
- Output current:  $|I_{OH}|/I_{OL} = 24$  mA (min) ( $V_{CC} = 3.0$  V)
- Latch-up performance:  $> \pm 500$  mA
- Available in JEITA SOP, VSSOP (US)
- Power-down protection is provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 273 type

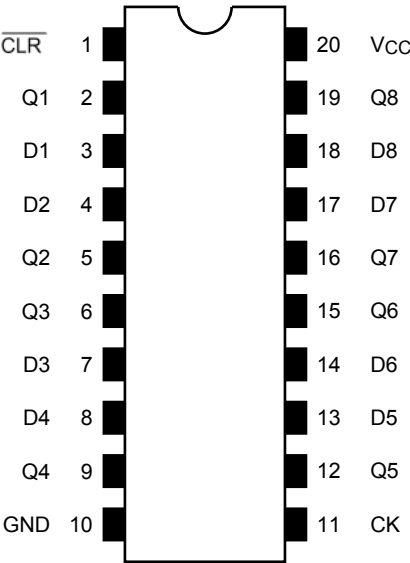


Weight	
SOP20-P-300-1.27A	: 0.22 g ( typ.)
VSSOP20-P-0030-0.50	: 0.03 g ( typ.)

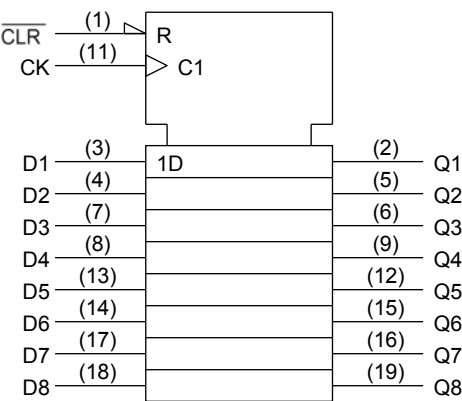
Note: The Electrical Characteristics of  $V_{CC} = 1.8 \pm 0.15$  V is only applicable for products which manufactured from January 2009 onward.

Start of commercial production  
2000-02

Pin Assignment (top view)



IEC Logic Symbol

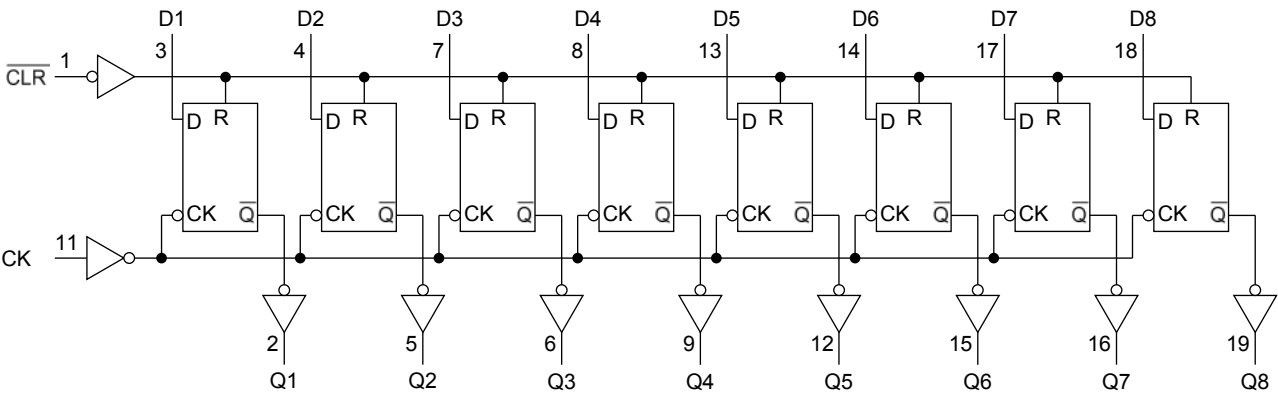


Truth Table

Inputs			Outputs	Function
$\overline{\text{CLR}}$	D	CK	Q	
L	X	X	L	Clear
H	L	$\uparrow$	L	—
H	H	$\uparrow$	H	—
H	X	$\downarrow$	Qn	No change

X: Don't care

System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V <sub>CC</sub>	−0.5 to 7.0	V
DC input voltage	V <sub>IN</sub>	−0.5 to 7.0	V
DC output voltage	V <sub>OUT</sub>	−0.5 to 7.0 (Note 2)	V
		−0.5 to V <sub>CC</sub> + 0.5 (Note 3)	
Input diode current	I <sub>IK</sub>	−50	mA
Output diode current	I <sub>OK</sub>	±50 (Note 4)	mA
DC output current	I <sub>OUT</sub>	±50	mA
Power dissipation	P <sub>D</sub>	180	mW
DC V <sub>CC</sub> /ground current	I <sub>CC</sub> /I <sub>GND</sub>	±100	mA
Storage temperature	T <sub>stg</sub>	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: V<sub>CC</sub> = 0 V

Note 3: High or low state. I<sub>OUT</sub> absolute maximum rating must be observed.

Note 4: V<sub>OUT</sub> < GND, V<sub>OUT</sub> > V<sub>CC</sub>

## Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V <sub>CC</sub>	1.65 to 3.6	V
		1.5 to 3.6 (Note 2)	
Input voltage	V <sub>IN</sub>	0 to 5.5	V
Output voltage	V <sub>OUT</sub>	0 to 5.5 (Note 3)	V
		0 to V <sub>CC</sub> (Note 4)	
Output current	I <sub>OH</sub> /I <sub>OL</sub>	±24 (Note 5)	mA
		±12 (Note 6)	
Operating temperature	T <sub>opr</sub>	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 7)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either V<sub>CC</sub> or GND.

Note 2: Data retention only

Note 3: V<sub>CC</sub> = 0 V

Note 4: High or low state

Note 5: V<sub>CC</sub> = 3.0 to 3.6 V

Note 6: V<sub>CC</sub> = 2.7 to 3.0 V

Note 7: V<sub>IN</sub> = 0.8 to 2.0 V, V<sub>CC</sub> = 3.0 V

### Electrical Characteristics

#### DC Characteristics (Ta = -40 to 85°C)

Characteristics		Symbol	Test Condition		V <sub>CC</sub> (V)	Min	Max	Unit
Input voltage	H-level	V <sub>IH</sub>			1.65 to 2.3	V <sub>CC</sub> × 0.9	—	V
					2.3 to 2.7	1.7	—	
					2.7 to 3.6	2.0	—	
	L-level	V <sub>IL</sub>			1.65 to 2.3	—	V <sub>CC</sub> × 0.1	
					2.3 to 2.7	—	0.7	
					2.7 to 3.6	—	0.8	
Output voltage	H-level	V <sub>OH</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = −100 μA	1.65 to 3.6	V <sub>CC</sub> − 0.2	—	V
				I <sub>OH</sub> = −4 mA	1.65	1.05	—	
				I <sub>OH</sub> = −8 mA	2.3	1.7	—	
				I <sub>OH</sub> = −12 mA	2.7	2.2	—	
				I <sub>OH</sub> = −18 mA	3.0	2.4	—	
				I <sub>OH</sub> = −24 mA	3.0	2.2	—	
	L-level	V <sub>OL</sub>	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 100 μA	1.65 to 3.6	—	0.2	
				I <sub>OL</sub> = 4 mA	1.65	—	0.45	
				I <sub>OL</sub> = 8 mA	2.3	—	0.7	
				I <sub>OL</sub> = 12 mA	2.7	—	0.4	
				I <sub>OL</sub> = 16 mA	3.0	—	0.4	
				I <sub>OL</sub> = 24 mA	3.0	—	0.55	
Input leakage current		I <sub>IN</sub>	V <sub>IN</sub> = 0 to 5.5 V	1.65 to 3.6	—	±5.0	μA	
Power-off leakage current		I <sub>OFF</sub>	V <sub>IN</sub> /V <sub>OUT</sub> = 5.5 V	0	—	10.0	μA	
Quiescent supply current		I <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> or GND	1.65 to 3.6	—	10.0	μA	
			V <sub>IN</sub> = 3.6 to 5.5 V	1.65 to 3.6	—	±10.0		
Increase in I <sub>CC</sub> per input		ΔI <sub>CC</sub>	V <sub>IN</sub> = V <sub>CC</sub> − 0.6 V (per 1 input)	2.7 to 3.6	—	500		

## AC Characteristics (Ta = -40 to 85°C)

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Min	Max	Unit
Maximum clock frequency	f <sub>MAX</sub>	(Figure 1, Figure 2)	1.8 ± 0.15	50	—	MHz
			2.5 ± 0.2	100	—	
			2.7	150	—	
			3.3 ± 0.3	150	—	
Propagation delay time (CK-Q)	t <sub>PLH</sub> t <sub>PHL</sub>	(Figure 1, Figure 2)	1.8 ± 0.15	—	30.0	ns
			2.5 ± 0.2	—	10.5	
			2.7	—	9.5	
			3.3 ± 0.3	1.5	8.5	
Propagation delay time ( $\overline{\text{CLR}}$ -Q)	t <sub>PHL</sub>	(Figure 1, Figure 3)	1.8 ± 0.15	—	30.0	ns
			2.5 ± 0.2	—	10.5	
			2.7	—	9.5	
			3.3 ± 0.3	1.5	8.5	
Minimum pulse width (CK)	t <sub>w</sub> (H) t <sub>w</sub> (L)	(Figure 1, Figure 2)	1.8 ± 0.15	10.0	—	ns
			2.5 ± 0.2	5.0	—	
			2.7	3.3	—	
			3.3 ± 0.3	3.3	—	
Minimum pulse width ( $\overline{\text{CLR}}$ )	t <sub>w</sub> (L)	(Figure 3)	1.8 ± 0.15	10.0	—	ns
			2.5 ± 0.2	5.0	—	
			2.7	3.3	—	
			3.3 ± 0.3	3.3	—	
Minimum setup time	t <sub>s</sub>	(Figure 1, Figure 2)	1.8 ± 0.15	10.0	—	ns
			2.5 ± 0.2	5.0	—	
			2.7	2.5	—	
			3.3 ± 0.3	2.5	—	
Minimum hold time	t <sub>h</sub>	(Figure 1, Figure 2)	1.8 ± 0.15	1.5	—	ns
			2.5 ± 0.2	1.5	—	
			2.7	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum removal time	t <sub>rem</sub>	(Figure 4)	1.8 ± 0.15	8.0	—	ns
			2.5 ± 0.2	4.0	—	
			2.7	2.5	—	
			3.3 ± 0.3	2.0	—	
Output to output skew	t <sub>osLH</sub> t <sub>osHL</sub>	(Note)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

Note: Parameter guaranteed by design.  
 (t<sub>osLH</sub> = |t<sub>pLHm</sub> - t<sub>pLHn</sub>|, t<sub>osHL</sub> = |t<sub>pHLm</sub> - t<sub>pHLn</sub>|)

### Dynamic Switching Characteristics

( $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 2.5\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 500\ \Omega$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V	3.3	0.8	V

### Capacitive Characteristics ( $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Test Condition	V <sub>CC</sub> (V)	Typ.	Unit
Input capacitance	C <sub>IN</sub>	—	3.3	7	pF
Output capacitance	C <sub>OUT</sub>		0	8	pF
Power dissipation capacitance	CPD	f <sub>IN</sub> = 10 MHz (Note)	3.3	25	pF

Note: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

### AC Test Circuit

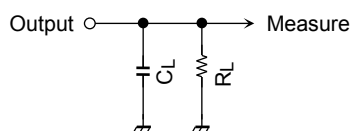


Figure 1

### AC Waveform

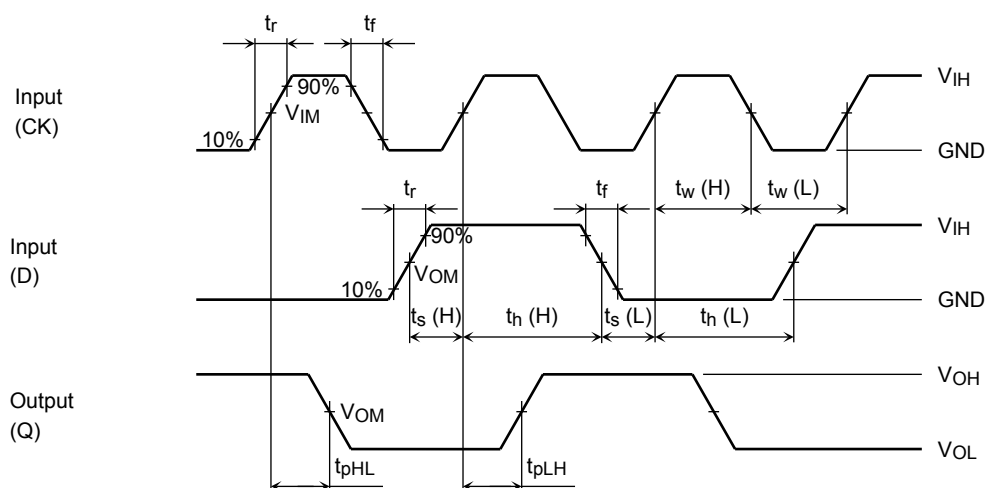


Figure 2  $t_{pLH}$ ,  $t_{pHL}$ ,  $t_w$ ,  $t_s$ ,  $t_h$

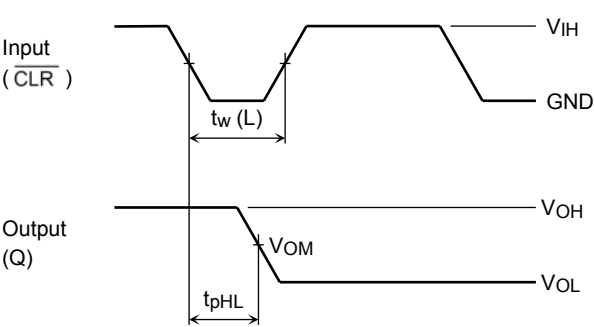


Figure 3  $t_{pHL}$

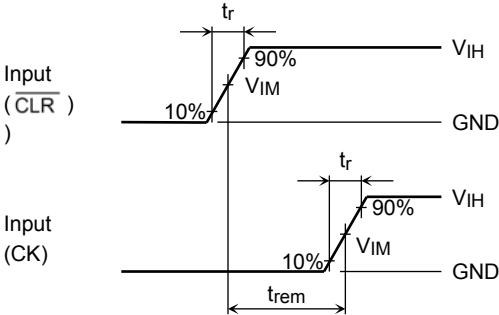


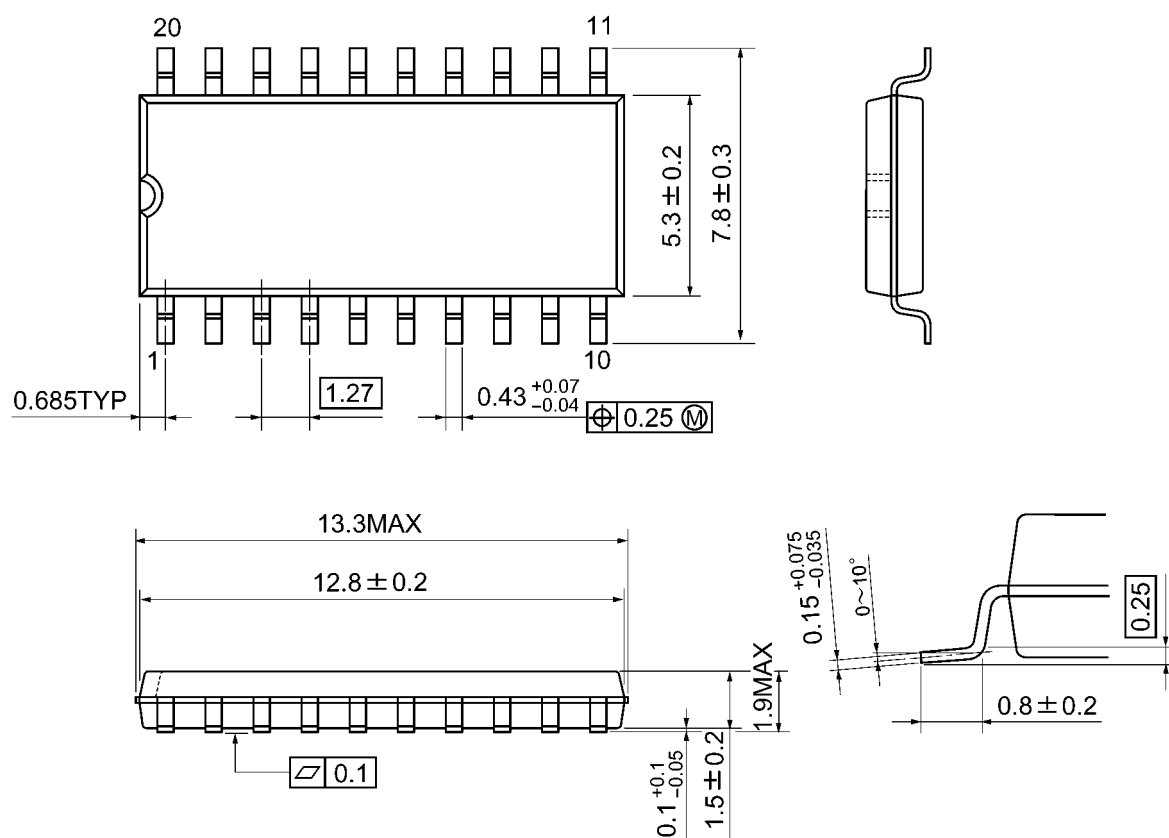
Figure 4  $t_{rem}$

	Symbol	V <sub>CC</sub>		
		3.3 ± 0.3 V 2.7 V	2.5 ± 0.2 V	1.8 ± 0.15 V
Input	V <sub>IH</sub>	2.7 V	V <sub>CC</sub>	V <sub>CC</sub>
	V <sub>IM</sub>	1.5 V	V <sub>CC</sub> /2	V <sub>CC</sub> /2
	t <sub>r</sub> , t <sub>f</sub>	2.5 ns	2.0 ns	2.0 ns
Output	V <sub>OM</sub>	1.5 V	V <sub>OH</sub> /2	V <sub>OH</sub> /2
Load	C <sub>L</sub>	50 pF	30 pF	30 pF
	R <sub>L</sub>	500 Ω	500 Ω	1 kΩ

### Package Dimensions

SOP20-P-300-1.27A

Unit: mm



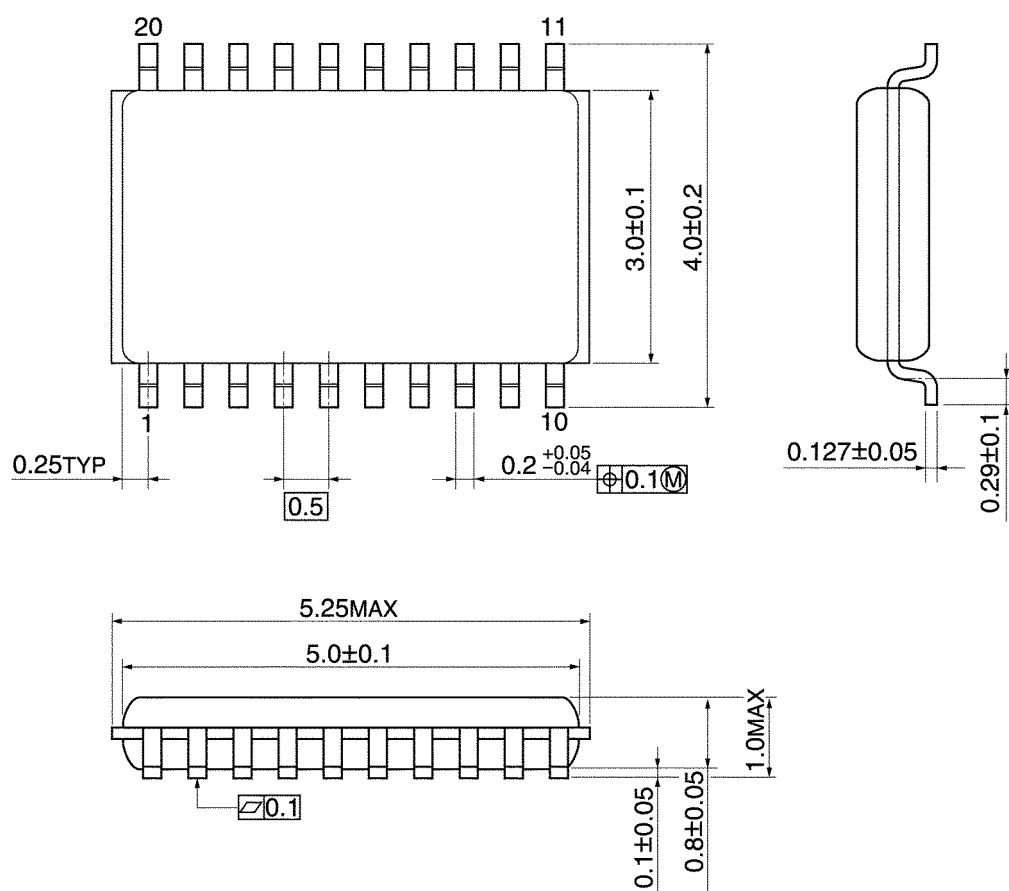
Weight: 0.22 g (typ.)



### Package Dimensions

VSSOP20-P-0030-0.50

Unit: mm



Weight: 0.03 g (typ.)

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