TC74HC221P/F

T-51-19

TC74HC221P/F DUAL MONOSTABLE MULTIVIBRATOR

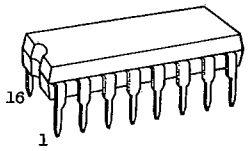
The TC74HC221 is a high speed CMOS DUAL MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaing the CMOS low power dissipation.
There are two trigger inputs. One is A INPUT (Negative-edge input), another is B INPUT (Positive-edge input). These inputs are valid for slow rising/falling signal ($t_r=t_f=1$ sec). Because of schmitt-trigger input function. The device may also be triggered by using $\overline{CLR}$ INPUT (Positive-edge input). After triggering, Output keeps MONOSTABLE STATE for the time period determined by external resistor Rx and by external capacitor Cx. "L" level $\overline{CLR}$ input breaks this STABLE STATE. Next coming new trigger in MONOSTABLE period is not effected. Limitation for Cx and Rx is as follows.

External capacitor Cx ..... no limitation
External resistor Rx ..... V_{CC}=2.0V from 5kΩ to 1MΩ
$V_{CC}\geq$3.0V from 1kΩ to 1MΩ

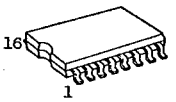
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... t_{pd}=32ns(Typ.) at V_{CC}=5V
- Low Power Dissipation .....
  Standby State I_{CC}=4μA(Max.) at Ta=25°C
  Active State I_{CC}=200μA(Typ.) at VCC=5V
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .... $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}\fallingdotseq t_{pHL}$
- Wide Output Pulse Width Range .... t_w(OUT)=150ns ∿ 60s over at V_{CC}=4.5V
- Pin and Function Compatible with LS221



DIP16(3D16A-P)



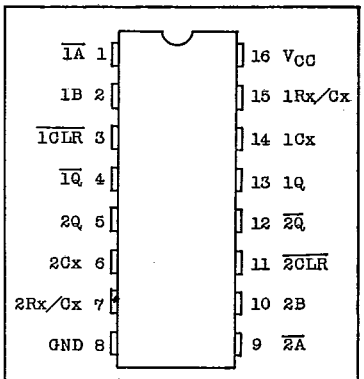
MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ∿ 7	V
DC Input Voltage	V_{IN}	-0.5 ∿ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ∿ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP) * 180 (MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40°C∿65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT



(TOP VIEW)

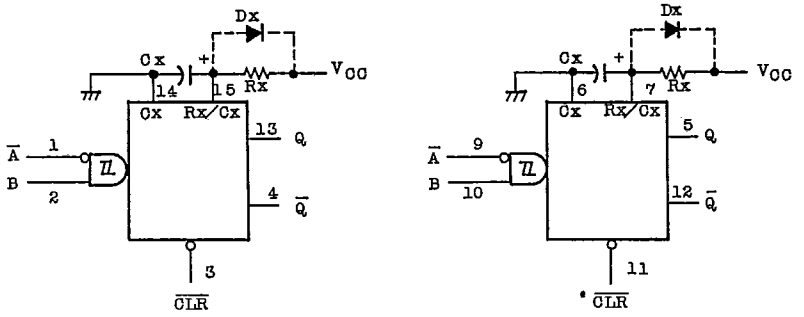
TRUTH TABLE

INPUTS			OUTPUTS		NOTE
$\overline{A}$	B	$\overline{CL}$	Q	$\overline{Q}$	
↓	H	H	⎍	⎓	OUTPUT ENABLE
X	L	H	L△	H△	INHIBIT
H	X	H	L△	H△	INHIBIT
L	↑	H	⎍	⎓	OUTPUT ENABLE
L	H	↑	⎍	⎓	OUTPUT ENABLE
X	X	L	L	H	INHIBIT

X: DON'T CARE

△: EXCEPT FOR MONOSTABLE PERIOD

BLOCK DIAGRAM



Note (1) Cx, Rx, Dx are external electric parts. Capacitor, resistor and diode.

(2) External diode Dx (CRAMPING DIODE)

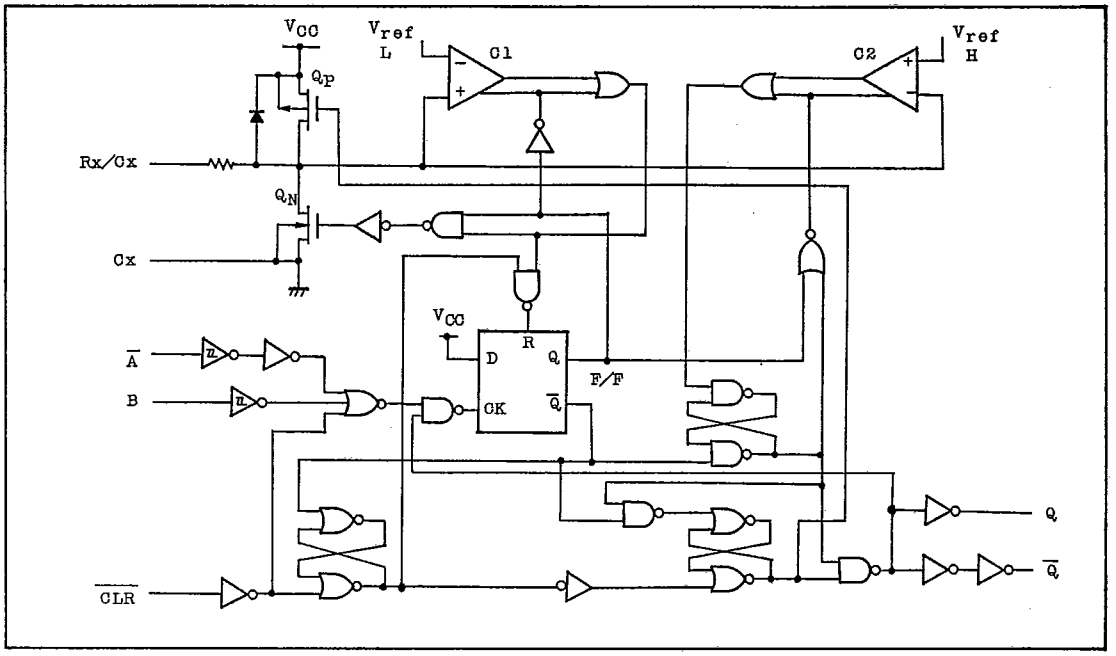
External capacitor is charged to V_{CC} level in the state of waiting, i.e. in no trigger state. Supply Voltage is turned off then Cx is discharged mainly through internal (parasitic) diode. See figure.
If Cx is sufficiently large and V_{CC} falls dowen rapidly, there will be some possibility of damaging IC by rushing current or latch-up. If capacitance of voltage supply filter is large enough and V_{CC} falls down slowly, the rushing current is automatically limited and avoid the damaging of IC.
The maximum value of forward current of parasitic diode is ±20mA. In the case of large Cx, limitation of falling down time of voltage supply is as follows

$$t_f \geqq (V_{CC} - 0.7) \cdot Cx/20mA$$

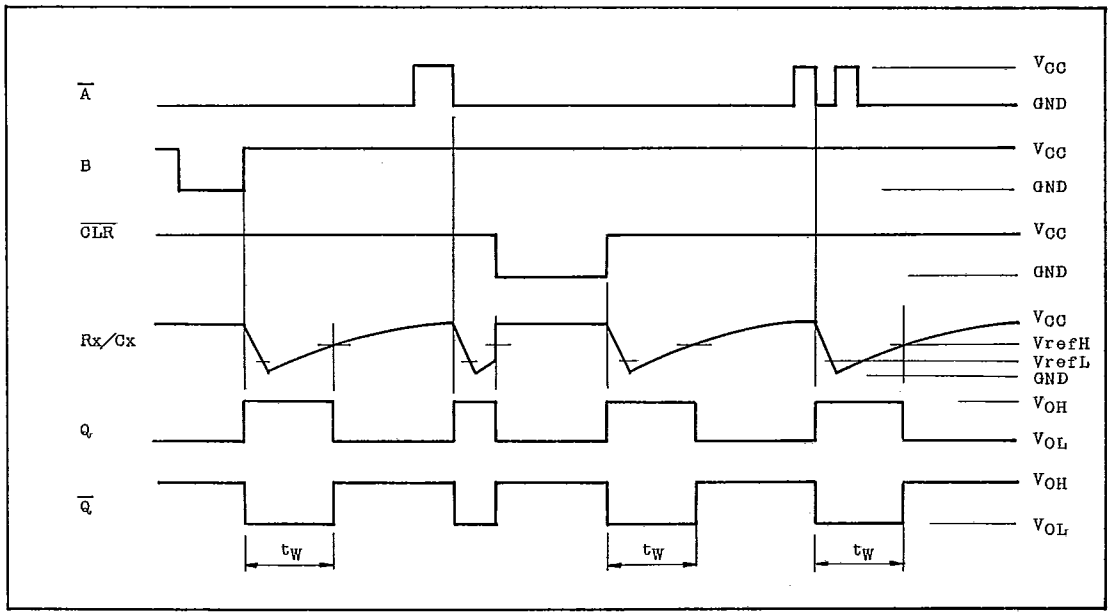
(t_f is the time from voltage supply turning off to level of voltage supply becoming 0.4 V_{CC})

In the case of "system is not satisfy the above condition", external CRAMPING DIODE is needed for protecting IC from rushing current. See figure.

SYSTEM DIAGRAM



TIMING CHART



FUNCTIONAL DESCRIPTION

(1) Stand-by state

External capacitor is fully charged to V_{CC} level in stand-by state. That means, before triggering, Qp, Qn transistors (Connected to Rx/Cx node) are in off state. Two comparator that relate to timing of pulse, and two reference voltage supplier stops their operations. The total supply current is only leakage current.

(2) Trigger operation

Trigger is effective in following three cases. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT have falling down signal. Under the condition B INPUT is "H" level and $\overline{A}$ INPUT has rising up signal. Under the condition $\overline{A}$ INPUT is "L" level and B INPUT is "H" level and $\overline{CLR}$ INPUT has rising up signal. After trigger effective, comparator of C1 and C2 start operating, and Qn transistor is turned on. Then the charge of external capacitor discharges through Qn transistor. The voltage level of Rx/Cx node becomes lower. If voltage level of Rx/Cx falls to the internal reference voltage VrefL, output of comparator C1 becomes "L". That means flip-flop is reseted and Qn transistor turns off. At that moment C1 stops but C2 continues its operating.

After turning off of Qn transistor, the voltage of Rx/Cx starts rising with the time constant of external capacitor Cx and resistor Rx.

By triggering, output Q becomes "H" level, after some delay time of internal F/F and gate. It keeps "H" level even in the voltage level of Rx/Cx changed from falling to rising. When it reaches to the internal reference voltage VrefH, output of comparator C2 becomes "L" level and Q output becomes "L" and comparator C2 stops its operations. That means, after triggering the voltage level of Rx/Cx becomes VrefH, IC keeps its MONO STABLE STATE. In the case Cx.Rx are large enough and it could be ignored the discharge time of capacitor and delay in IC, the width of output pulse $t_W(OUT)$ is as follows.

$$t_W(OUT) = 0.70 \quad Cx \; Rx$$

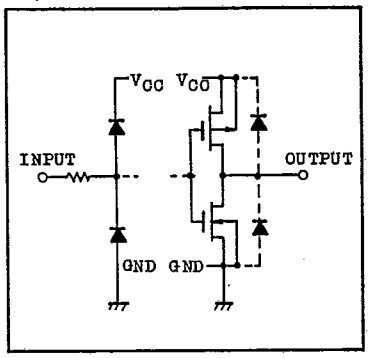
(3) Reset operation

$\overline{CLR}$ is normally "H". If $\overline{CLR}$ is "L", trigger is not effective because of Q output becomes "L" and trigger control F/F is reseted. And also transistor Qp is turns on and Cx is charged rapidly to V_{CC} level. This means if $\overline{CLR}$ input becomes "L", IC becomes waiting state both in operating and non-operating state.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ∿ 6	V
Input Voltage	V_{IN}	0 ∿ V_{CC}	V
Output Voltage	V_{OUT}	0 ∿ V_{CC}	V
Operating Temperature	T_{opr}	−40 ∿ 85	°C
Input Rise and Fall Time ($\overline{CLR}$ Only)	t_r, t_f	0 ∿ 1000 (V_{CC}=2.0V) 0 ∿ 500 (V_{CC}=4.5V) 0 ∿ 400 (V_{CC}=6.0V)	ns
External Capacitor	Cx	No Limitation	F
External Resistor (V_{CC}=2.0V) (V_{CC}≧3.0V)	Rx	5K ∿ 1M 1K ∿ 1M	Ω

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=−40∿85°C MIN.	Ta=−40∿85°C MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OH}	V_{IN}= V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	−	1.9	−	
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH}=−4mA	4.5	4.18	4.31	−	4.31	−	
			I_{OH}=−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage (Q, $\overline{Q}$ Output)	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	−	0.0	0.1	−	0.1	
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL}=4mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL}=5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
R/C Terminal Off-State Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	−	−	±0.5	−	±5.0	
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	−	−	4.0	−	40.0	
Active-State * Supply Current	I_{CC}'	V_{IN}=V_{CC} or GND R/C_{ext}=0.5V_{CC}		2.0	−	40	120	−	160	μA
				4.5	−	0.1	0.3	−	0.4	mA
				6.0	−	0.2	0.6	−	0.8	mA

*: per Circuit

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input $t_r=t_f$=6ns)

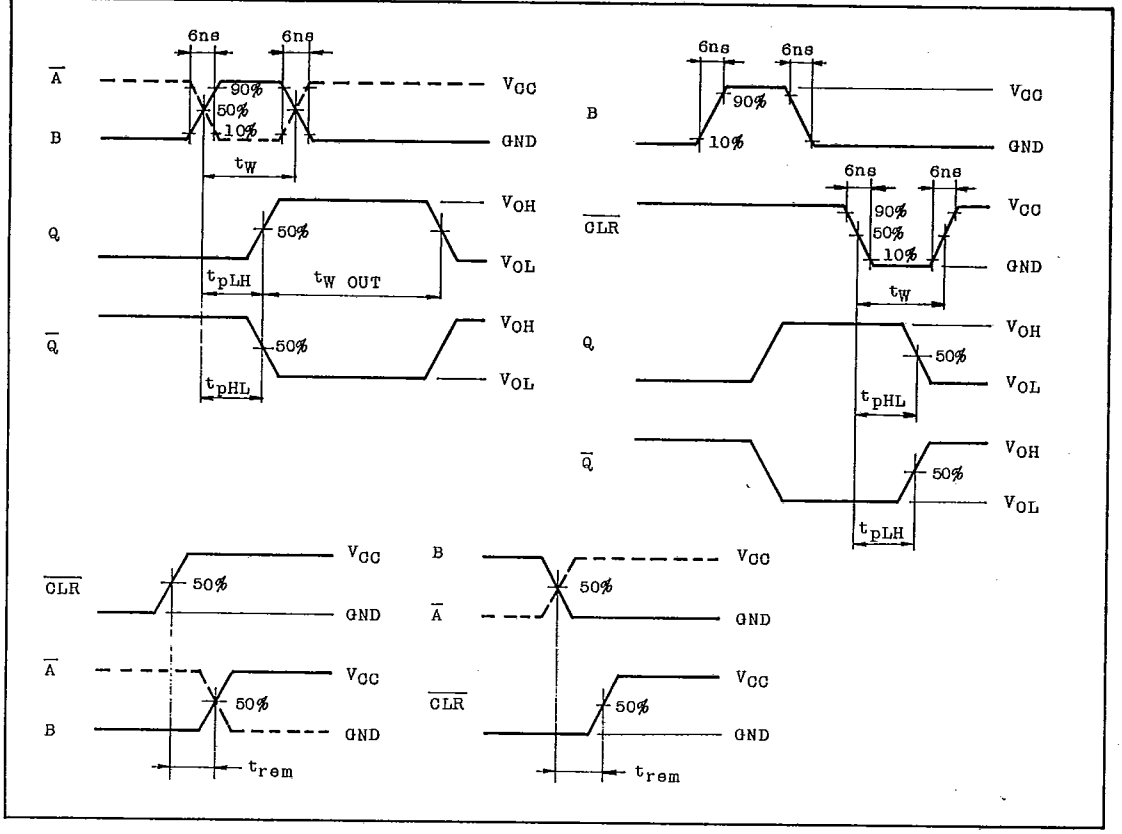
PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		2.0	-	30	75	-	95	ns
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Propagation Delay Time ($\overline{A}$,B TRIGGER-Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	144	280	-	350	
			4.5	-	36	56	-	70	
			6.0	-	31	48	-	60	
Propagation Delay Time ($\overline{CLR}$ TRIGGER-Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	164	310	-	390	
			4.5	-	41	62	-	78	
			6.0	-	35	53	-	66	
Propagation Delay Time ($\overline{CLR}$-Q,$\overline{Q}$)	t_{pLH} t_{pHL}		2.0	-	108	210	-	265	
			4.5	-	27	42	-	53	
			6.0	-	23	36	-	45	
Minimum Trigger Pulse Width	$t_{w(H)}$ $t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Minimum Clear Pulse Width	$t_{w(L)}$		2.0	-	30	75	-	95	
			4.5	-	8	15	-	19	
			6.0	-	7	13	-	16	
Output Pulse Width Error. Between Circuits In same Package	Δt_{wOUT}			-	±1	-	-	-	%
Minimum Removal Time ($\overline{A}$,B TRIGGER)	t_{rem}		2.0	-	-	0	-	0	ns
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time ($\overline{CLR}$ TRIGGER)	t_{rem}		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Output Pulse Width	t_{wOUT} (MIN)	Cx=0 Rx=5kΩ (V_{CC}=2V)	2.0	-	490	1450	-	1825	
			4.5	-	190	290	-	365	
		Rx=1kΩ (V_{CC}=4.5, 6V)	6.0	-	170	260	-	325	
Output Pulse Width	t_{wOUT}	Cx=0.01μF Rx=10kΩ	2.0	72	85	98	72	98	μs
			4.5	72	80	88	72	88	
			6.0	72	80	88	72	88	
		Cx=0.1μF Rx=10kΩ	2.0	0.67	0.75	0.83	0.67	0.83	ms
			4.5	0.67	0.73	0.79	0.67	0.79	
			6.0	0.67	0.73	0.79	0.67	0.79	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	109	-	-	-	

Note(1): C_{PD} is defined as the value of internal equivalent capacitance of IC which is calcualted from the operating current consumption without load (refer to Test circuit). Average operating current can be obtained by equation hereunder.

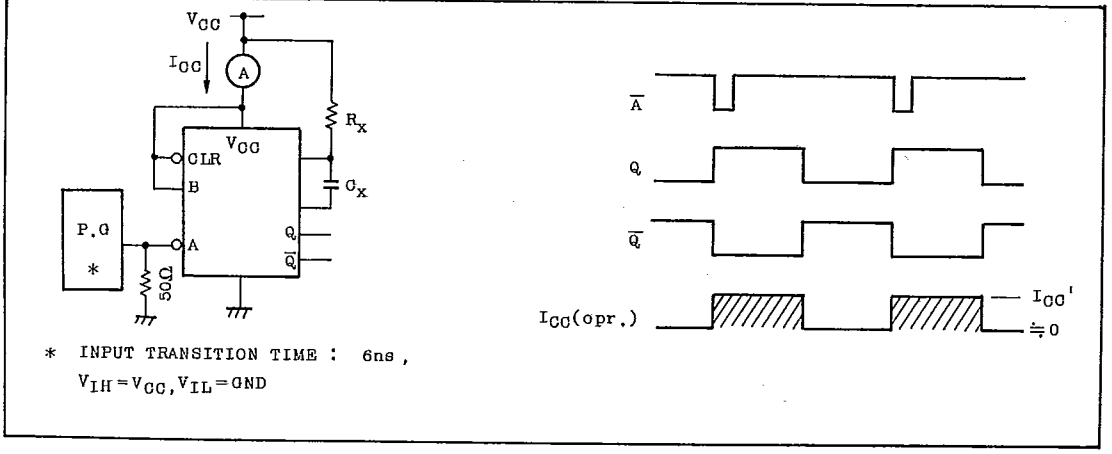
$I_{CC}(opr.)=C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}' \cdot Duty/100 + I_{CC}/2$ (per monostable)

(I_{CC}': Active Supply Current, Duty: %)

SWITCHING CHARACTERISTICS TEST WAVEFORM

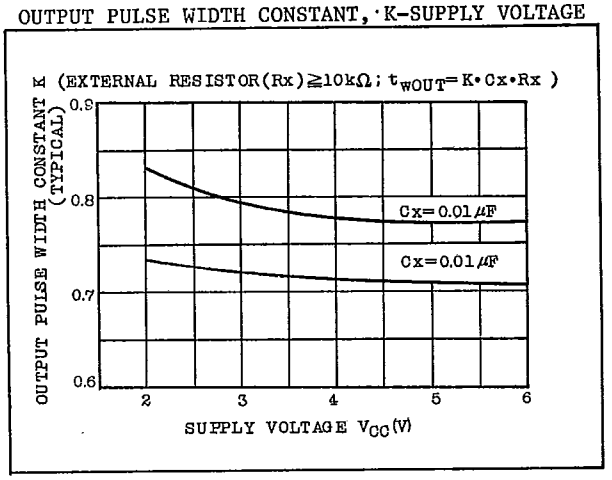


I_{CC}(opr.) TEST WAVEFROM



* INPUT TRANSITION TIME : 6ns ,
$V_{IH}=V_{CC}, V_{IL}=GND$

OUTPUT PULSE WIDTH CONSTANT, K-SUPPLY VOLTAGE



t_{wOUT} - Cx CHARACTERISTICS (TYP.)