TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

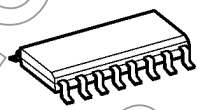
TC74HC161AFN
TC74HC163AFN

Synchronous Presettable 4-Bit Counter

TC74HC161AFN	Binary, Asynchronous Clear
TC74HC163AFN	Binary, Synchronous Clear

Note: xxxFN (JEDEC SOP) is not available in Japan.

TC74HC161AFN, TC74HC163AFN



SOL16-P-150-1.27

Weight
SOL16-P-150-1.27 : 0.13 g (typ.)

The TC74HC161A and 163A are high speed CMOS BINARY PRESETTABLE COUNTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The CK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLR}$ inputs are active on low logic level.

Presetting of their IC's is synchronous to the rising edge of CK.

The clear function of the TC74HC163A is synchronous to CK, while the TC74HC161A is cleared asynchronously.

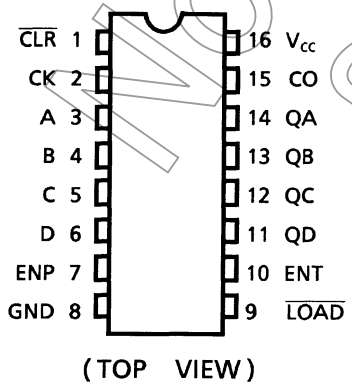
Two enable inputs (ENP and ENT) and CO are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: f_{max} = 63 MHz (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- High noise immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 4 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 6 V
- Pin and function compatible with 74LS161, 163

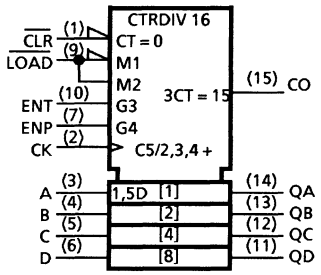
Pin Assignment



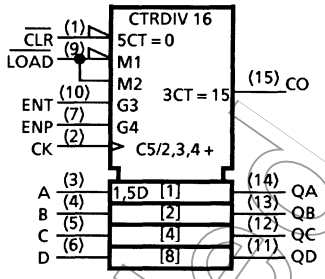
(TOP VIEW)

IEC Logic Symbol

TC74HC161A



TC74HC163A



Truth Table

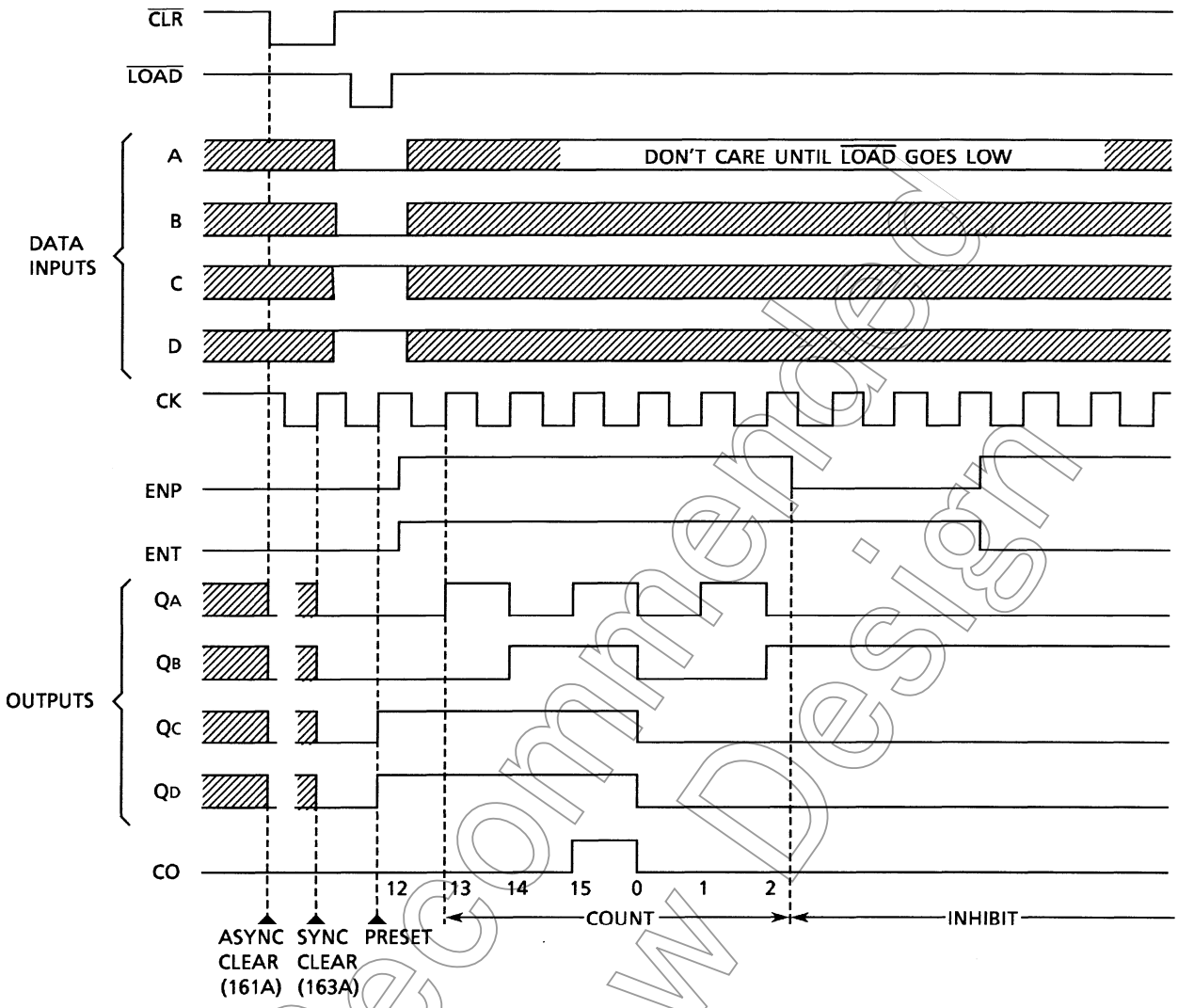
TC74HC161A					TC74HC163A					Outputs				Function
Inputs					Inputs									
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	Reset to “0”
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	Preset Data
H	H	X	L	↑	H	H	X	L	↑	No Change				No Count
H	H	L	X	↑	H	H	L	X	↑	No Change				No Count
H	H	H	H	↑	H	H	H	H	↑	Count Up				Count
H	X	X	X	↓	X	X	X	X	↓	No Change				No Count

X: Don’t care

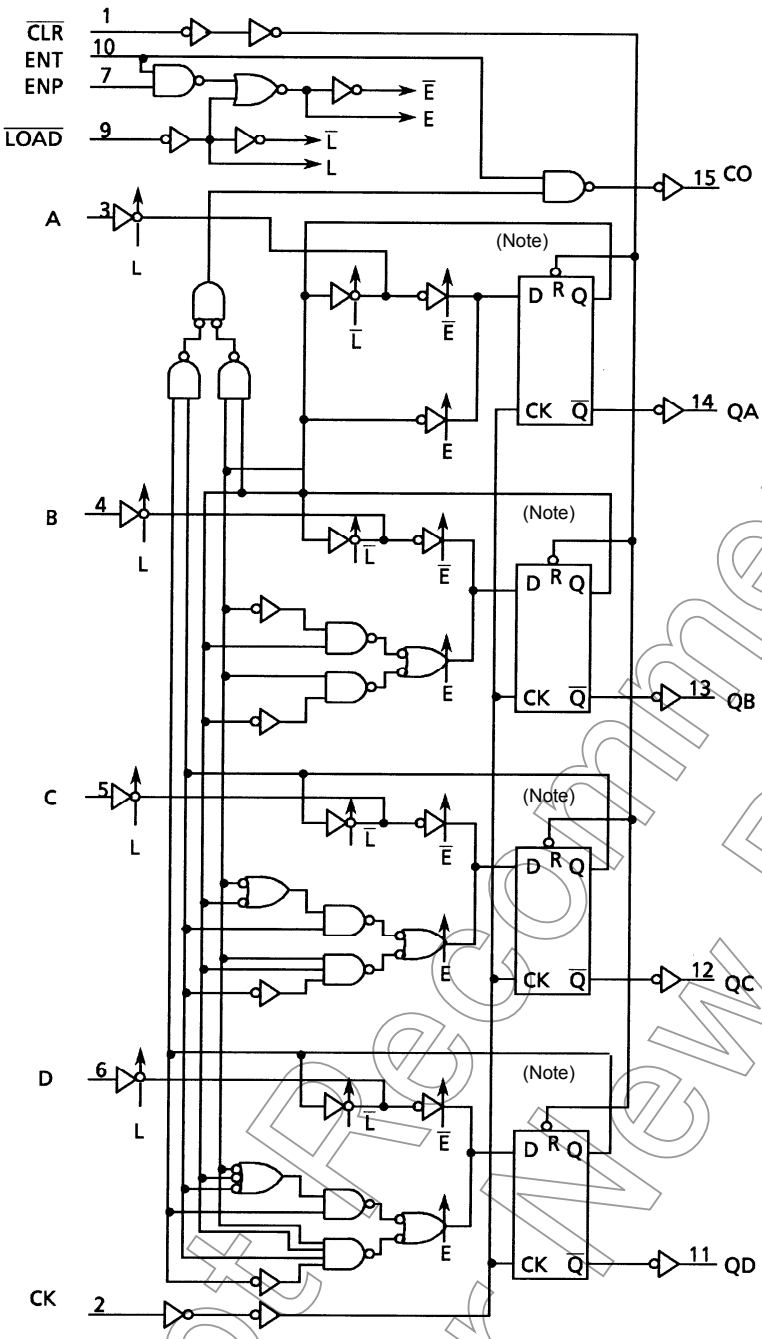
A, B, C, D: Logic level of data inputs

Carry: Carry = ENT·QA·QB·QC·QD

Timing Chart



System Diagram



Note: Truth table of internal F/F

TC74HC161A					TC74HC163A				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	L	L	H	X	↑	L	L	H
L	↑	H	L	H	L	↑	H	L	H
H	↑	H	H	L	H	↑	H	H	L
X	↓	H	No Change		L	↓	H	No Change	

X: Don't care

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7	V
DC input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2 to 6	V
Input voltage	V_{IN}	0 to V_{CC}	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	t_r, t_f	0 to 1000 (V_{CC} = 2.0 V) 0 to 500 (V_{CC} = 4.5 V) 0 to 400 (V_{CC} = 6.0 V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40 to 85°C Min	Ta = −40 to 85°C Max	Unit
High-level input voltage	V_{IH}	—		2.0	1.50	—	—	1.50	—	V
				4.5	3.15	—	—	3.15	—	
				6.0	4.20	—	—	4.20	—	
Low-level input voltage	V_{IL}	—		2.0	—	—	0.50	—	0.50	V
				4.5	—	—	1.35	—	1.35	
				6.0	—	—	1.80	—	1.80	
High-level output voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20 μA	2.0	1.9	2.0	—	1.9	—	V
				4.5	4.4	4.5	—	4.4	—	
				6.0	5.9	6.0	—	5.9	—	
			I_{OH} = −4 mA	4.5	4.18	4.31	—	4.13	—	
			I_{OH} = −5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 μA	2.0	—	0.0	0.1	—	0.1	V
				4.5	—	0.0	0.1	—	0.1	
				6.0	—	0.1	0.1	—	0.1	
			I_{OL} = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I_{OL} = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C		Ta = −40 to 85°C	Unit
			V_{CC} (V)	Typ.	Limit	Limit	
Minimum pulse width (CK)	$t_{W(H)}$ / $t_{W(L)}$	Figure 1	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum pulse width ($\overline{CLR}$) (Note 1)	$t_{W(L)}$	Figure 4	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ($\overline{LOAD}$, ENP, ENT)	t_s	Figure 2, Figure 3	2.0	—	100	125	ns
			4.5	—	20	25	
			6.0	—	17	21	
Minimum set-up time (A, B, C, D)	t_s	Figure 2	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum set-up time ($\overline{CLR}$) (Note 2)	t_s	Figure 5	2.0	—	75	95	ns
			4.5	—	15	19	
			6.0	—	13	16	
Minimum hold time	t_h	Figure 2, Figure 3, Figure 5	2.0	—	0	0	ns
			4.5	—	0	0	
			6.0	—	0	0	
Minimum removal time ($\overline{CLR}$) (Note 1)	t_{rem}	Figure 4	2.0	—	50	65	ns
			4.5	—	10	13	
			6.0	—	9	11	
Clock frequency	f	—	2.0	—	6	5	MHz
			4.5	—	31	25	
			6.0	—	36	29	

Note 1: For TC74HC161A only

Note 2: For TC74HC163A only

AC Characteristics (C_L = 15 pF, V_{CC} = 5 V, Ta = 25°C, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	t_{TLH} t_{THL}	Figure 1	—	4	8	ns
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	Figure 1	—	13	21	ns
Propagation delay time (CK-CO) [count mode]	t_{pLH} t_{pHL}	Figure 1	—	16	26	ns
Propagation delay time (CK-CO) [preset mode]	t_{pLH}	Figure 2	—	18	30	ns
	t_{pHL}		—	20	35	
Propagation delay time (ENT-CO)	t_{pLH} t_{pHL}	Figure 6	—	10	17	ns
Propagation delay time ($\overline{CLR}$ -Q) (Note)	t_{pHL}	Figure 4	—	17	26	ns
Propagation delay time ($\overline{CLR}$ -CO) (Note)	t_{pHL}	Figure 4	—	20	35	ns
Maximum clock frequency	f_{max}	—	36	63	—	MHz

Note: For TC74HC161A only

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	2.0	—	25	75	—	95	ns
			4.5	—	7	15	—	19	
			6.0	—	6	13	—	16	
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	Figure 1	2.0	—	48	125	—	155	ns
			4.5	—	16	25	—	31	
			6.0	—	14	21	—	26	
Propagation delay time (CK-CO) [count mode]	t_{pLH} t_{pHL}	Figure 1	2.0	—	57	150	—	190	ns
			4.5	—	19	30	—	38	
			6.0	—	16	26	—	33	
Propagation delay time (CK-CO) [preset mode]	t_{pLH}	Figure 2	2.0	—	66	175	—	220	ns
			4.5	—	22	35	—	44	
			6.0	—	19	30	—	37	
	t_{pHL}		2.0	—	72	200	—	250	
			4.5	—	24	40	—	50	
			6.0	—	20	34	—	43	
Propagation delay time (ENT-CO)	t_{pLH} t_{pHL}	Figure 6	2.0	—	39	100	—	125	ns
			4.5	—	13	20	—	25	
			6.0	—	11	17	—	21	
Propagation delay time ($\overline{CLR}$ -Q) (Note 2)	t_{pHL}	Figure 4	2.0	—	60	150	—	190	ns
			4.5	—	20	30	—	38	
			6.0	—	17	26	—	33	
Propagation delay time ($\overline{CLR}$ -CO) (Note 2)	t_{pHL}	Figure 4	2.0	—	72	200	—	250	ns
			4.5	—	24	40	—	50	
			6.0	—	20	34	—	43	
Maximum clock frequency	f_{max}	—	2.0	6	18	—	5	—	MHz
			4.5	31	53	—	25	—	
			6.0	36	62	—	29	—	
Input capacitance	C_{IN}	—		—	5	10	—	10	pF
Power dissipation capacitance	C_{PD} (Note 1)	—		—	34	—	—	—	pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}\ (opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of C_{PD}, and ΔI_{CC} which is obtained from the following formula:

In case of TC74HC161A/163A:

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16}\right)$$

C_{QA}~C_{QD} and C_{CO} are the capacitances at QA~QD and CO, respectively.

f_{CK} is the input frequency of the CK.

Note 2: For TC74HC161A only

Switching Characteristics Test Waveform

Count Mode

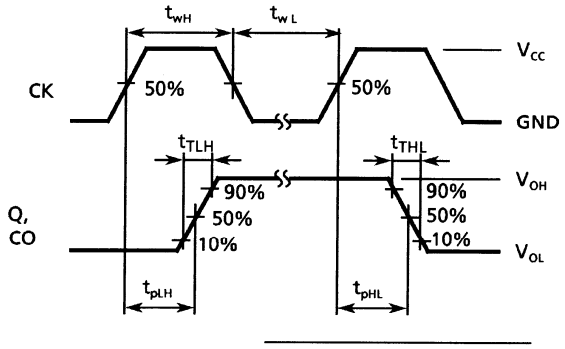


Figure 1

Preset Mode

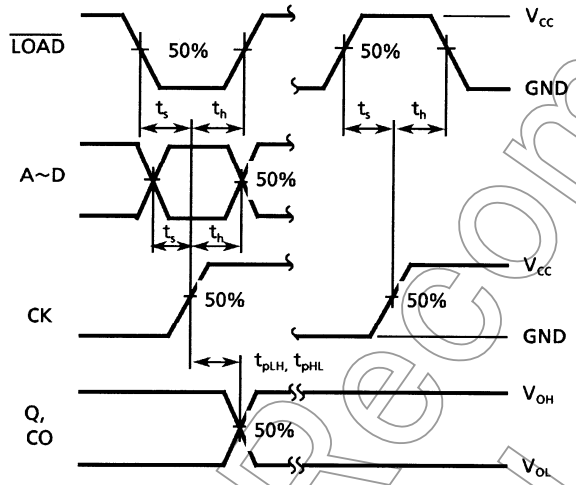


Figure 2

Count Enable Mode

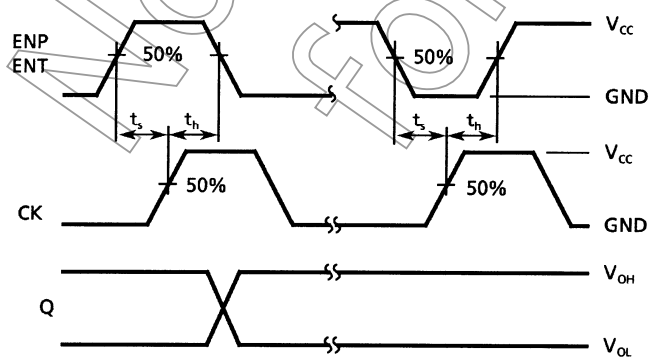


Figure 3

Clear Mode (TC74HC161A)

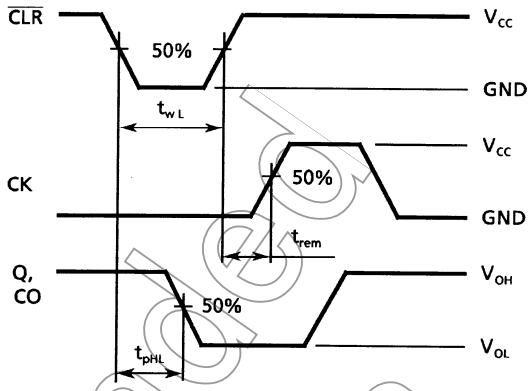


Figure 4

Clear Mode (TC74HC163A)

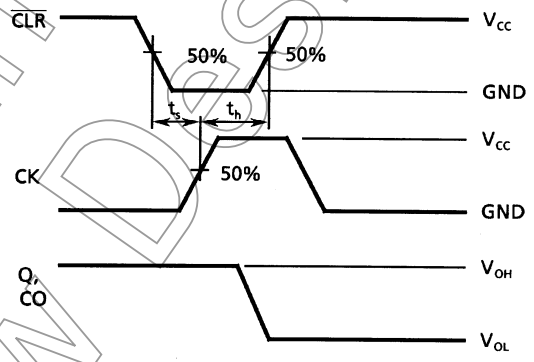


Figure 5

Cascade Mode (fix maximum count)

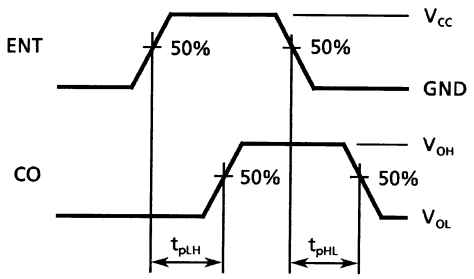
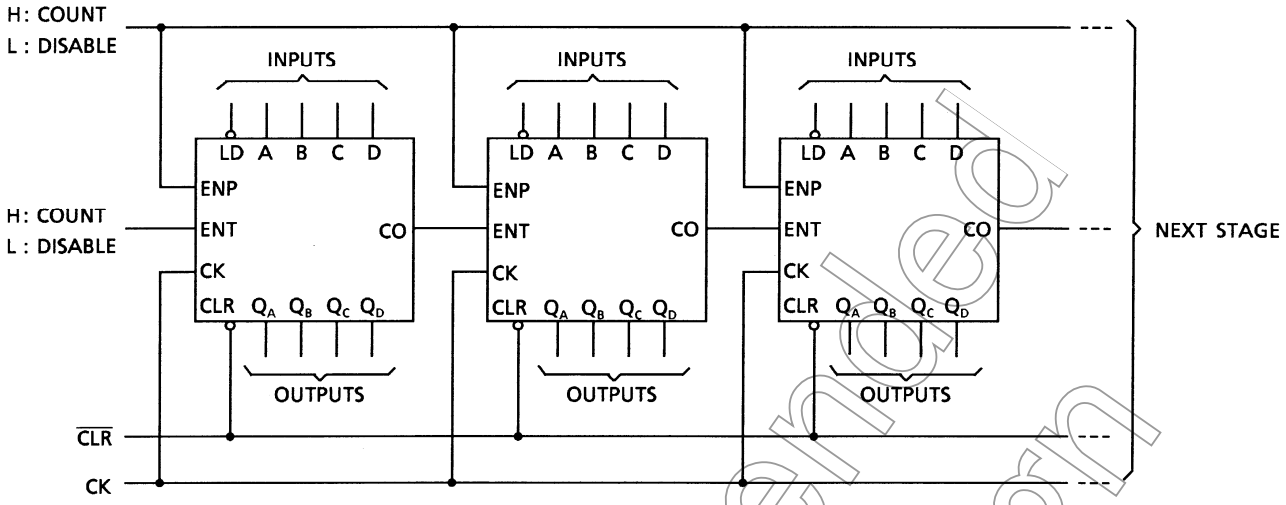


Figure 6

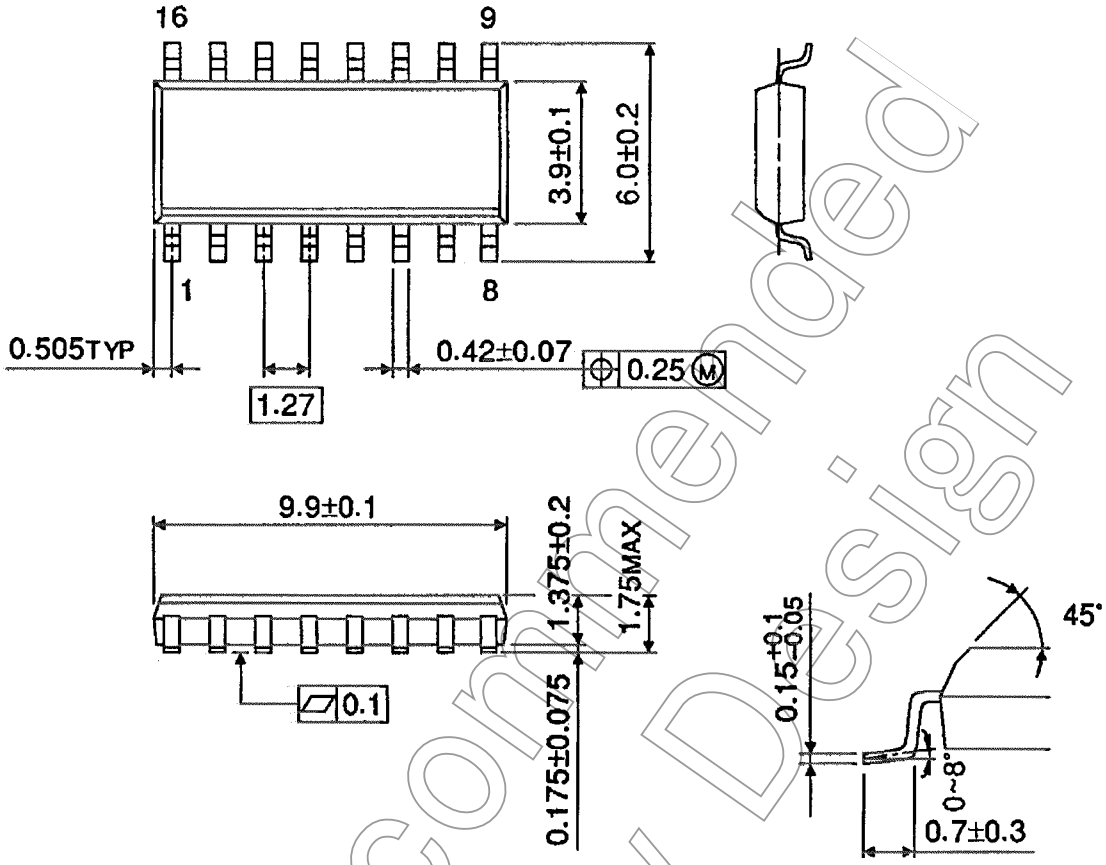
Typical Application

Parallel Carry N-Bit Counter



Package Dimensions (Note)

SOL16-P-150-1.27 Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

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