TC74AC374P, TC74AC534F

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC374P, TC74AC374F, TC74AC374FT TC74AC534P, TC74AC534F

Octal D-Type Flip-Flop with 3-state Output

TC74AC374P/F/FT Non-Inverting

TC74AC534P/F Inverting

The TC74AC374 and TC74AC534 are advanced high speed CMOS OCTAL FLIP-FLOPS fabricated with silicon gate and double-layer metal wiring C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input (\overline{OE}) .

When the \overline{OE} input is high, the eight outputs are in a high impedance state.

The TC74AC374 has non-inverting outputs, and TC74AC534 has inverting outputs.

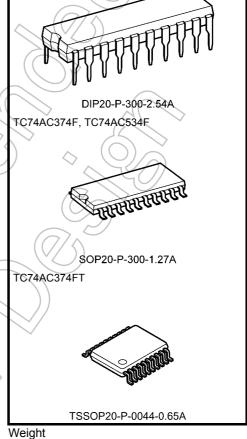
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $f_{max} = 200 \text{ MHz}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 8 \mu A \text{ (max)}$ at $T_a = 25 \text{°C}$
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Symmetrical output impedance: |IOH| = IOL = 24 mA (min) Capability of driving 50Ω

transmission lines.

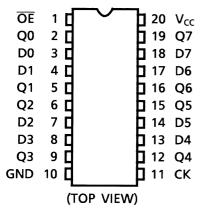
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V
- Pin and function compatible with 74F374/534



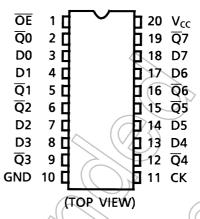
DIP20-P-300-2.54A : 1.30 g (typ.) SOP20-P-300-1.27A : 0.22 g (typ.) TSSOP20-P-0044-0.65A : 0.08 g (typ.)

Pin Assignment

TC74AC374

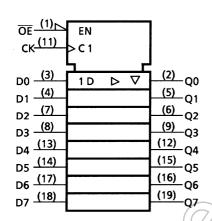


TC74AC534

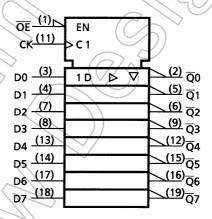


IEC Logic Symbol

TC74AC374



TC74AC534



Truth Table

	Inputs		Outputs					
ŌE	CK	D	Q (374)	Q (534)				
Н	Х	X	Z	Z				
L	\neg	X	Qn	\overline{Q}_n				
L		(L	L	Ξ(
L			H	(4)				

X: Don't care

Z: High impedance

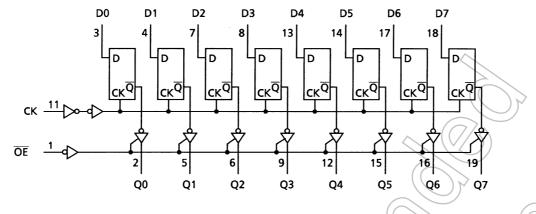
 $Q_n(\overline{Q}_n)$: No change

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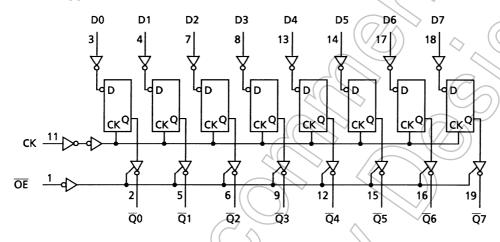


System Diagram

TC74AC374



TC74AC534



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Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to V _{CC} + 0.5	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	lok	±50	mA
DC output current	lout	±50	mA
DC V _{CC} /ground current	Icc	±200)) mA
Power dissipation	PD	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C, a derating factor of -10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	VCC	2:0 to 5.5	V
Input voltage	$//\sqrt{\hat{v}_{jN}}$	0 to V _{CC}	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature	Topr	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 ($V_{CC} = 3.3 \pm 0.3 \text{ V}$) 0 to 20 ($V_{CC} = 5 \pm 0.5 \text{ V}$)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.



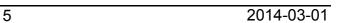
Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = –40 to 85°C		Unit	
Characteristics	Cymbol			V _{CC} (V)	Min	Тур.	Max	Min	Max	Omit
				2.0	1.50	_	1	1.50	_	
High-level input voltage	V_{IH}		_	3.0	2.10	_	(=)	2.10	_	V
S .				5.5	3.85			3.85	_	
				2.0	>	40	0.50	_	0.50	
Low-level input voltage	V_{IL}		_	3.0	-	\ \ \\	0.90	_	0.90	V
				5.5	-(1	1.65	_	1.65	
				2.0	1.9	2.0	_	1.9	_	
			$I_{OH} = -50 \ \mu A$	3.0	2.9	3.0	_	2.9	_	
High-level output	V _{OH}	V _{IN} = V _{IH} or V _{IL}		4.5	4.4	4.5		4.4	\searrow	V
voltage			$I_{OH} = -4 \text{ mA}$	3.0	2.58	_	-6	2.48	> —	V
			I _{OH} = -24 mA	4.5	3.94	_\	(3.80) —	
			$I_{OH} = -75 \text{ mA}$ (Note)	5.5	_		1	3.85		
		V _{IN} = V _{IH} or V _{IL}		2.0	_	0.0	0.1	>_	0.1	V
			$I_{OL} = 50 \mu A$	3.0	_	0.0	0.1	_	0.1	
Low-level output	V _{OL}			4.5	_	0.0	0.1	_	0.1	
voltage	V OL		$I_{OL} = 12 \text{ mA}$	3.0	((2)	0.36	_	0.44	V
			$I_{OL} = 24 \text{ mA}$	4.5	_		0.36	_	0.44	
			$I_{OL} = 75 \text{ mA}$ (Note)	5.5)	_	_	1.65	
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5		_	±0.5	_	±5.0	μА
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	\ \ \	_	±0.1	_	±1.0	μА
Quiescent supply current	lee	$V_{IN} = V_{C}$	C or GND	5.5		_	8.0	_	80.0	μА

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.





Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	Ta = 25°C	Ta = -40 to 85°C	Unit	
			V _{CC} (V)	Limit	Limit	
Minimum pulse width	t _{W (H)}		3.3 ± 0.3	7.0	7.0	20
(CK)	t _{W (L)}	_	5.0 ± 0.5	5.0	5.0	ns
Minimum set-up time	t _S		3.3 ± 0.3	9.0	9.0	20
		_	5.0 ± 0.5	5.0	5.0	ns
Minimum hold time	t _h		3.3 ± 0.3	0.0	0.0	20
		_	5.0 ± 0.5	0.0	0.0	ns

AC Characteristics ($C_L = 50 \text{ pF}, R_L = 500 \Omega$, input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Test Condition		Ta = 25°C			Ta = -40 to 85°C	
	-,		V _{CC} (V)	Min	Тур.	Max	Min	Max	
Propagation delay time	t _{pLH}	_	3.3 ± 0.3	7 _}	8.5	15.8	1.0	18.0	ns
(CK-Q, \overline{Q})	t _{pHL}		5.0 ± 0.5		6.1	8.7	(4.0)	10.0	110
Output enable time	t _{pZL}		3.3 ± 0.3	_	7.5	14.0	1.0	16.0	ns
Output enable time	t _{pZH}	_	5.0 ± 0.5	_	6.1	8.7	1.0	10.0	115
Output disable time	t _{pLZ}		3.3 ± 0.3	_	5.5	12.3	1.0	14.0	ns
Output disable time	t _{pHZ}		5.0 ± 0.5		4.7	7.0	1.0	8.0	115
Maximum clock	f _{max}		3.3 ± 0.3/	55	120		55		MHz
frequency	ımax		5.0 ± 0.5	100	160		100		IVII IZ
Input capacitance	C _{IN}	(\bigcirc)		-	5	10	_	10	pF
Output capacitance	C _{OUT}		\wedge	_	10		_		pF
Power dissipation capacitance	C _{PD} (Note)	<u> </u>		<u> </u>	37		_		pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption

Average operating current can be obtained by the equation:

$$I_{CC}$$
 (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per F/F)

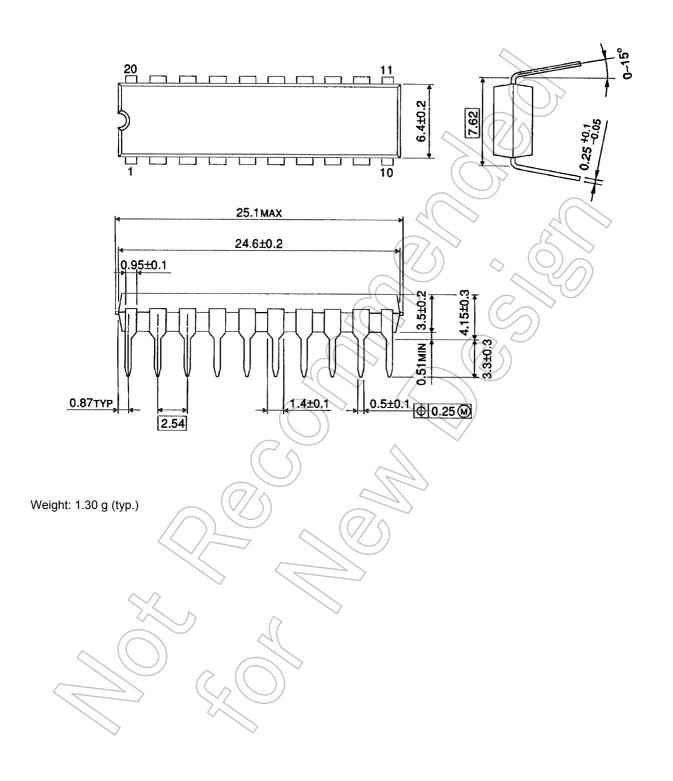
And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation:

C_{PD} (total) = 25 + 12 · n



Package Dimensions

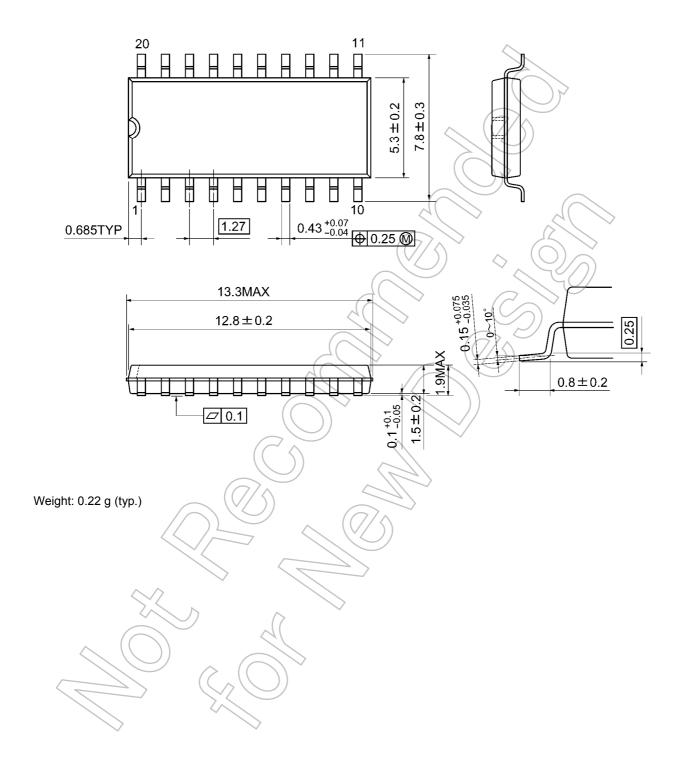
DIP20-P-300-2.54A Unit: mm





Package Dimensions

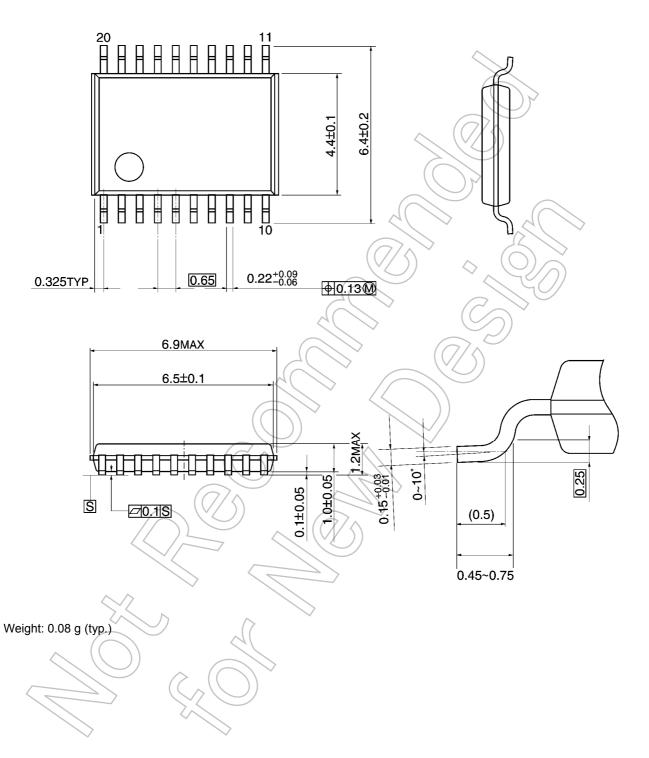
SOP20-P-300-1.27A Unit: mm





Package Dimensions

TSSOP20-P-0044-0.65A Unit: mm



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