TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC4024BP, TC4024BF

## TC4024B 7 Stage Ripple-Carry Binary Counter/Dividers

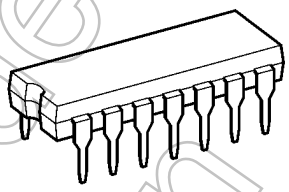
TC4024B is 7 stage ripple carry type binary counter having asynchronous clear function.

The counter advances its counting state by falling edge of $\overline{\text{CLOCK}}$ input.

When RESET input is placed at "H", all the internal flip-flop are reset making all the outputs Q1 through Q7 to be "L" regardless of $\overline{\text{CLOCK}}$ input.

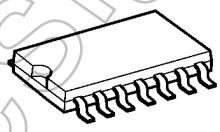
This is suitable for frequency divider circuits and control circuits.

TC4024BP



DIP14-P-300-2.54

TC4024BF



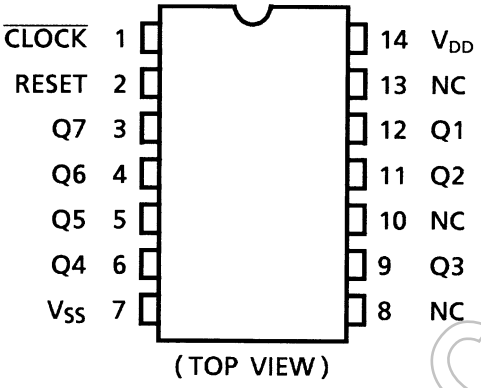
SOP14-P-300-1.27A

Weight

DIP14-P-300-2.54 : 0.96 g (typ.)

SOP14-P-300-1.27A : 0.18 g (typ.)

### Pin Assignment




### Truth Table

| $\overline{\text{CLOCK}}$ Δ | RESET | Output State |
|---|---|---|
| * | H | All Outputs = "L" |
| ↑ | L | No Change |
| ↓ | L | Advance to Next State |

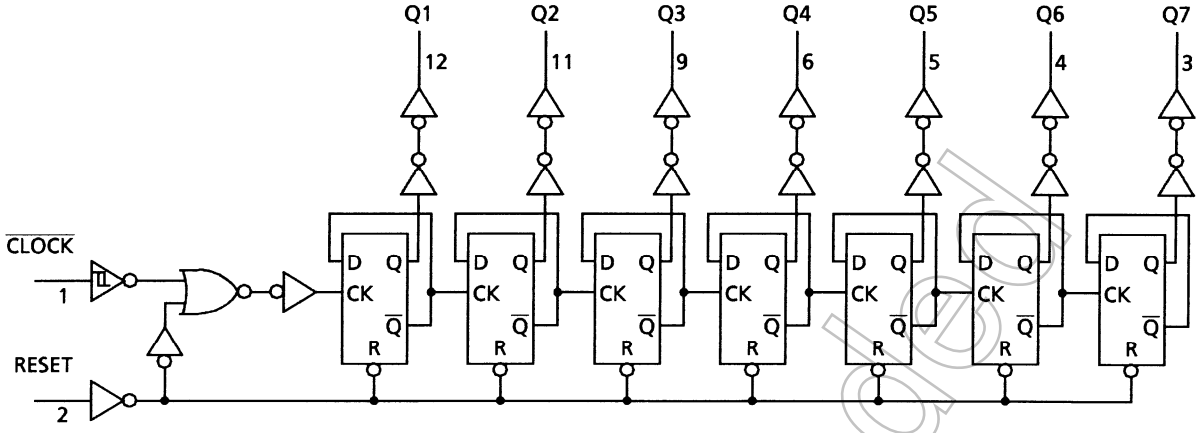
Δ: Level change

*: Don't care



Start of commercial production
1978-07

## Logic Diagram




## Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| DC supply voltage | $V_{DD}$ | $V_{SS}$ − 0.5 to $V_{SS}$ + 20 | V |
| Input voltage | $V_{IN}$ | $V_{SS}$ − 0.5 to $V_{DD}$ + 0.5 | V |
| Output voltage | $V_{OUT}$ | $V_{SS}$ − 0.5 to $V_{DD}$ + 0.5 | V |
| DC input current | $I_{IN}$ | ±10 | mA |
| Power dissipation | $P_D$ | 300 (DIP)/180 (SOP) | mW |
| Operating temperature range | $T_{opr}$ | −40 to 85 | °C |
| Storage temperature range | $T_{stg}$ | −65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges ($V_{SS}$ = 0 V) (Note)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| DC supply voltage | $V_{DD}$ | — | 3 | — | 18 | V |
| Input voltage | $V_{IN}$ | — | 0 | — | $V_{DD}$ | V |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either $V_{DD}$ or $V_{SS}$.

## Static Electrical Characteristics ($V_{SS}$ = 0 V)

| Characteristics | Sym-bol | Test Condition | | –40°C | | 25°C | | | 85°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{DD}$ (V) | Min | Max | Min | Typ. | Max | Min | Max | |
| High-level output voltage | $V_{OH}$ | $\|I_{OUT}\| < 1$ μA<br>$V_{IN} = V_{SS}, V_{DD}$ | 5 | 4.95 | — | 4.95 | 5.00 | — | 4.95 | — | V |
| | | | 10 | 9.95 | — | 9.95 | 10.00 | — | 9.95 | — | |
| | | | 15 | 14.95 | — | 14.95 | 15.00 | — | 14.95 | — | |
| Low-level output voltage | $V_{OL}$ | $\|I_{OUT}\| < 1$ μA<br>$V_{IN} = V_{SS}, V_{DD}$ | 5 | — | 0.05 | — | 0.00 | 0.05 | — | 0.05 | V |
| | | | 10 | — | 0.05 | — | 0.00 | 0.05 | — | 0.05 | |
| | | | 15 | — | 0.05 | — | 0.00 | 0.05 | — | 0.05 | |
| Output high current | $I_{OH}$ | $V_{OH}$ = 4.6 V | 5 | –0.61 | — | –0.51 | –1.0 | — | –0.42 | — | mA |
| | | $V_{OH}$ = 2.5 V | 5 | –2.50 | — | –2.10 | –4.0 | — | –1.70 | — | |
| | | $V_{OH}$ = 9.5 V | 10 | –1.50 | — | –1.30 | –2.2 | — | –1.10 | — | |
| | | $V_{OH}$ = 13.5 V | 15 | –4.00 | — | –3.40 | –9.0 | — | –2.80 | — | |
| | | $V_{IN} = V_{SS}, V_{DD}$ | | | | | | | | | |
| Output low current | $I_{OL}$ | $V_{OL}$ = 0.4 V | 5 | 0.61 | — | 0.51 | 1.2 | — | 0.42 | — | mA |
| | | $V_{OL}$ = 0.5 V | 10 | 1.50 | — | 1.30 | 3.2 | — | 1.10 | — | |
| | | $V_{OL}$ = 1.5 V | 15 | 4.00 | — | 3.40 | 12.0 | — | 2.80 | — | |
| | | $V_{IN} = V_{SS}, V_{DD}$ | | | | | | | | | |
| Input high voltage | $V_{IH}$ | $V_{OUT}$ = 0.5 V, 4.5 V | 5 | 3.5 | — | 3.5 | 2.75 | — | 3.5 | — | V |
| | | $V_{OUT}$ = 1.0 V, 9.0 V | 10 | 7.0 | — | 7.0 | 5.50 | — | 7.0 | — | |
| | | $V_{OUT}$ = 1.5 V, 13.5 V | 15 | 11.0 | — | 11.0 | 8.25 | — | 11.0 | — | |
| | | $\|I_{OUT}\| < 1$ μA | | | | | | | | | |
| Input low voltage | $V_{IL}$ | $V_{OUT}$ = 0.5 V, 4.5 V | 5 | — | 1.5 | — | 2.25 | 1.5 | — | 1.5 | V |
| | | $V_{OUT}$ = 1.0 V, 9.0 V | 10 | — | 3.0 | — | 4.50 | 3.0 | — | 3.0 | |
| | | $V_{OUT}$ = 1.5 V, 13.5 V | 15 | — | 4.0 | — | 6.75 | 4.0 | — | 4.0 | |
| | | $\|I_{OUT}\| < 1$ μA | | | | | | | | | |
| Input current "H" level | $I_{IH}$ | $V_{IH}$ = 18 V | 18 | — | 0.1 | — | $10^{-5}$ | 0.1 | — | 1.0 | μA |
| Input current "L" level | $I_{IL}$ | $V_{IL}$ = 0 V | 18 | — | –0.1 | — | $-10^{-5}$ | –0.1 | — | –1.0 | |
| Quiescent supply current | $I_{DD}$ | $V_{IN} = V_{SS}, V_{DD}$ (Note) | 5 | — | 5 | — | 0.005 | 5 | — | 150 | μA |
| | | | 10 | — | 10 | — | 0.010 | 10 | — | 300 | |
| | | | 15 | — | 20 | — | 0.015 | 20 | — | 600 | |

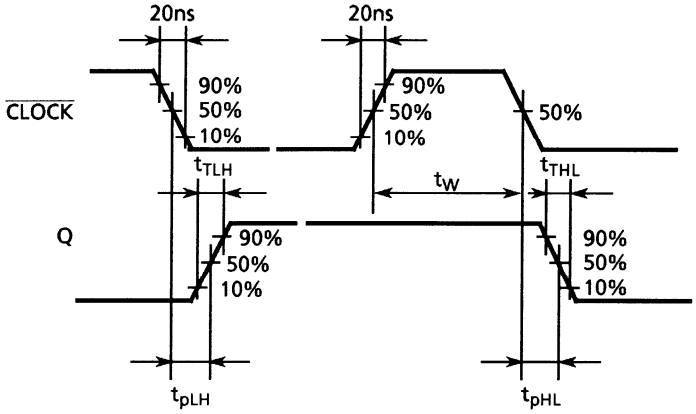
Note: All valid input combinations.

## Dynamic Electrical Characteristics (Ta = 25°C, $V_{SS}$ = 0 V, $C_L$ = 50 pF)

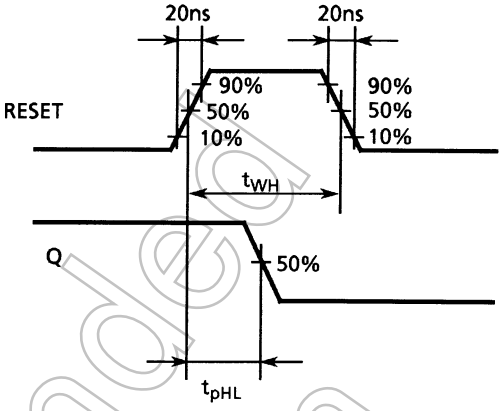
| Characteristics | Symbol | Test Condition | $V_{DD}$ (V) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Output transition time (low to high) | $t_{TLH}$ | — | 5 | — | 70 | 200 | ns |
| | | | 10 | — | 35 | 100 | |
| | | | 15 | | 30 | 80 | |
| Output transition time (high to low) | $t_{THL}$ | — | 5 | — | 70 | 200 | ns |
| | | | 10 | — | 35 | 100 | |
| | | | 15 | — | 30 | 80 | |
| Propagation delay time ($\overline{CLOCK}$ -Q1) | $t_{pLH}$ | — | 5 | — | 140 | 360 | ns |
| | | | 10 | — | 70 | 160 | |
| | | | 15 | — | 50 | 130 | |
| Propagation delay time ($\overline{CLOCK}$ -Q1) | $t_{pHL}$ | — | 5 | — | 140 | 360 | ns |
| | | | 10 | — | 70 | 160 | |
| | | | 15 | — | 50 | 130 | |
| Propagation delay time ($\overline{CLOCK}$ -Q7) | $t_{pLH}$ | — | 5 | — | 400 | 1200 | ns |
| | | | 10 | — | 160 | 520 | |
| | | | 15 | — | 115 | 430 | |
| Propagation delay time ($\overline{CLOCK}$ -Q7) | $t_{pHL}$ | — | 5 | — | 400 | 1200 | ns |
| | | | 10 | — | 160 | 520 | |
| | | | 15 | — | 115 | 430 | |
| Propagation delay time (RESET-Q) | $t_{pHL}$ | — | 5 | — | 140 | 280 | ns |
| | | | 10 | — | 70 | 120 | |
| | | | 15 | — | 50 | 100 | |
| Max clock frequency | $f_{CL}$ | — | 5 | 3.5 | 14 | — | MHz |
| | | | 10 | 8.0 | 30 | — | |
| | | | 15 | 12.0 | 40 | — | |
| Max clock input rise time<br>Max clock input fall time | $t_{rCL}$<br>$t_{fCL}$ | — | 5<br>10<br>15 | No limit | | | μs |
| Max clock pulse width | $t_W$ | — | 5 | — | 40 | 140 | ns |
| | | | 10 | — | 20 | 60 | |
| | | | 15 | — | 15 | 40 | |
| Max pulse width (RESET) | $t_{WH}$ | — | 5 | — | 40 | 200 | ns |
| | | | 10 | — | 20 | 80 | |
| | | | 15 | — | 15 | 60 | |
| Minimum removal time | $t_{rem}$ | — | 5 | — | 0 | 350 | ns |
| | | | 10 | — | 0 | 150 | |
| | | | 15 | — | 0 | 100 | |
| Input capacitance | $C_{IN}$ | — | | — | 5 | 7.5 | pF |

## Waveforms for Measurement of Dynamic Characteristics

### Waveform 1

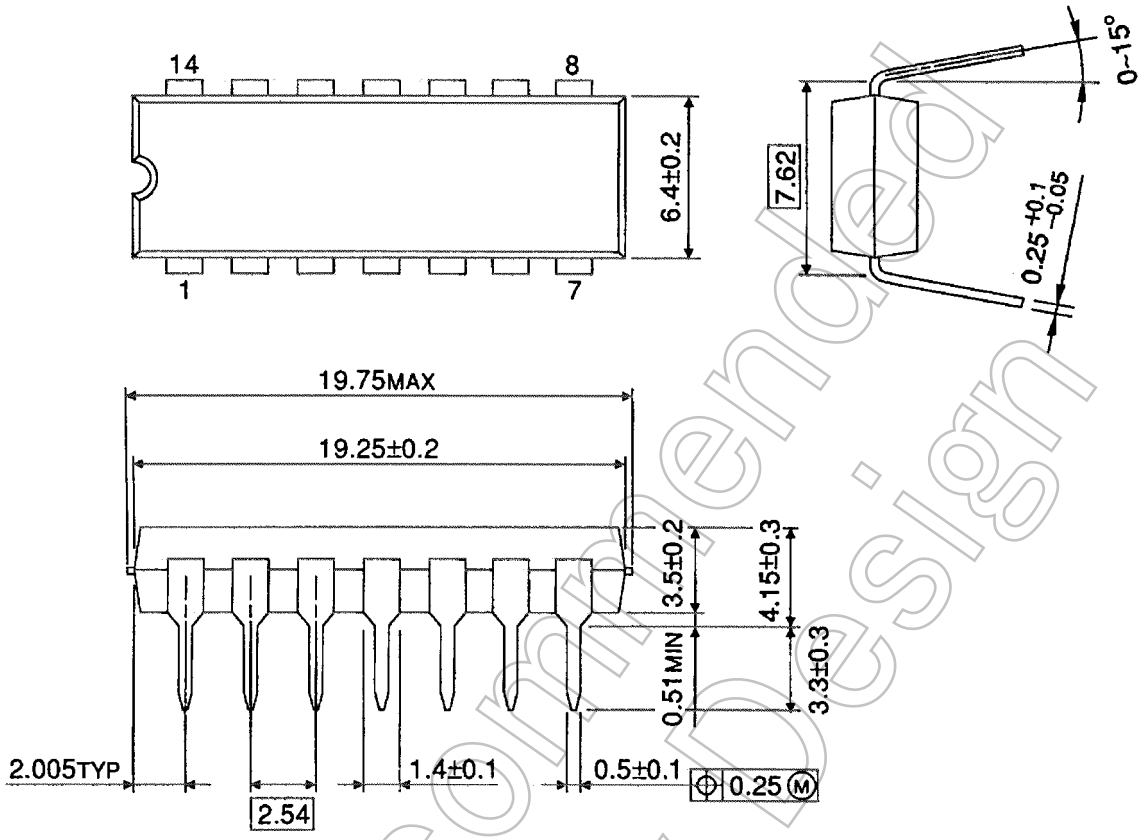



### Waveform 2



## Package Dimensions

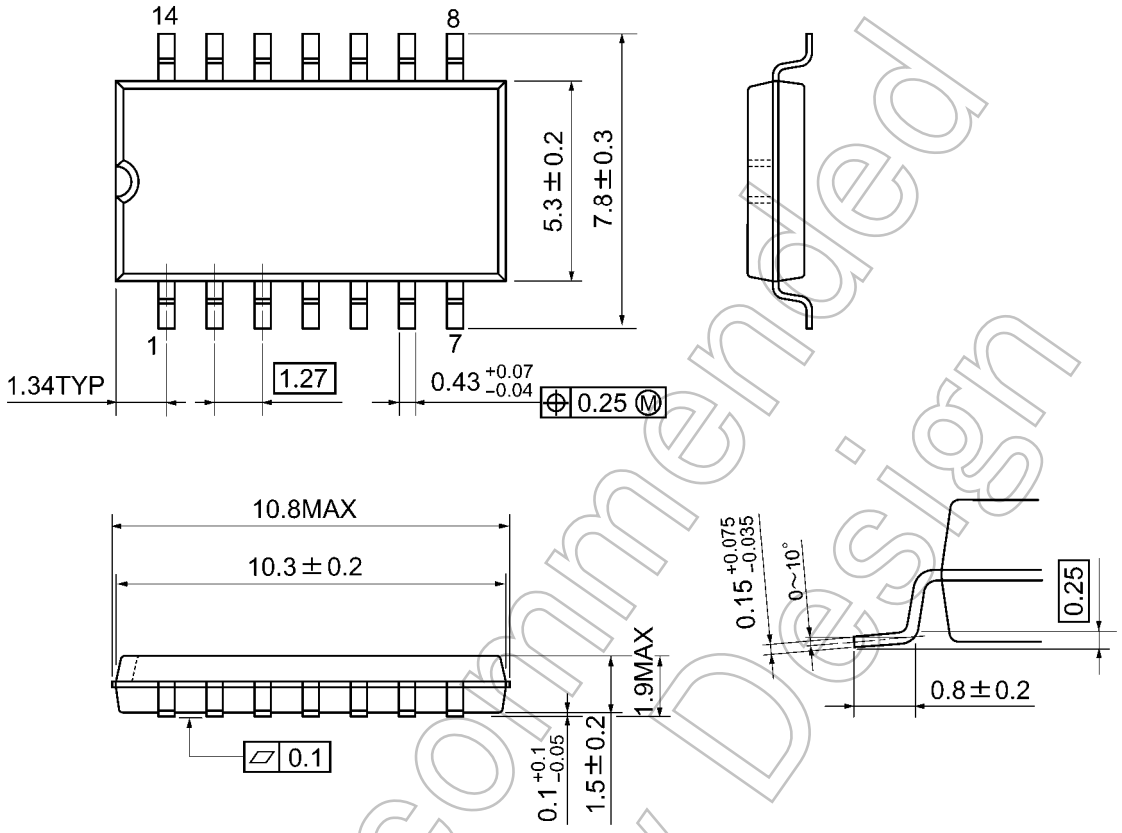
DIP14-P-300-2.54 Unit : mm




Weight: 0.96 g (typ.)

## Package Dimensions

SOP14-P-300-1.27A Unit: mm




Weight: 0.18 g (typ.)

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