XIO2001 PCI Express to PCI Bus Translation Bridge Silicon Errata

This document identifies the errata discovered in the XIO2001.

1 Using Serial Interrupts may result in multiple MSI messages being sent.

Table 1.

Description	If a serial interrupt stream is provided for the XIO2001 to convert into a message signal interrupt (MSI) then in some high bus traffic situations, the XIO2001 may send out duplicate MSI messages. The error is largely timing dependant and occurs when a MSI occurs and large posted transaction is sent through the XIO2001. If the MSI REQ/ACK handshake is delayed due to a pending posted transaction, the XIO2001 will resend the MSI. If large posted transactions continue to pass through the XIO2001, this may happen multiple times.
Impact	Interrupt Service Routines for the asserted interrupts may be incorrectly called multiple times. Results of false interrupt calls are driver and system dependent and may have no impact or may result in system instability or serious errors resulting in system halts.
Workaround	The error will not occur if large posted transactions are not passed through the XIO2001. It has been verified that limiting posted transactions to no larger than 200 bytes will prevent this issue from occurring. Larger transactions will run the risk of a spurious MSI.

2 Using Serial Interrupts in Level Mode may result in a situation where after 1 or more interrupts, no further interrupts are sent.

Table 2.

Description	If a serial interrupt stream is provided for the XIO2001 to convert into a message signal interrupt (MSI) and the interrupt mode is set to level mode, if the message to the XIO2001 to rearm the interrupt comes too quickly, the re-arm message may be lost resulting in a loss of future interrupt events
Impact	If the re-arm message is missed by the XIO2001 then it will not be enabled to send further interrupt messages for that IRQ. This will result in a loss of all future processing from that device that is dependant on the interrupt and may result in system instability
Workaround	The use of edge triggered serial IRQs will not result in this issue occurring. And it is recommended that edge triggered serial IRQs be used when possible. When it is necessary to use a level triggered serial IRQ then IRQ13, IRQ14, and IRQ15 should be used as the use of these interrupts does not result in duplicate MSI messages. If the standard 33/66 MHz clocks provided by the XIO2001 are used then IRQ12 also can be used, however if other clock frequencies are used, IRQ12 should not be used as it may result in the same issue.

3 CLKREQ# does not function properly in all PCI Power managed states.

Description:

Table 3 shows the state of REFCLK/PCLK. Where REFCLK is the pci-express reference clock and PCLK is the PCI bus clock. Bit 0 in the TL Control and Diagnostic Register 0 at PCI offset C0h is the FORCE_CLKREQ bit. When this bit is set, the bridge will force CLKREQ# output to always be asserted. Bit 8 in the Link Control Register at PCI offset 80h is the CPM_EN bit. This bit is used to enable the bridge to use CLKREQ# for clock power management. Bit 11 in the General Control Register at PCI offset D4h is the BPCC_E bit. This bit controls whether the secondary bus PCI clocks are stopped when the bridge is placed in the D3 state

Table 3.

FORCE_CLKREQ	CPM_EN	BPCC_E	Bridge D State			
			D0	D1	D2	D3
0	0	0	ON/ON	ON/ON	ON/ON	ON/ON
0	0	1	ON/ON	ON/ON	ON/ON	ON/OFF
0	1	0	ON/ON	OFF/FR	OFF/FR	OFF/FR
0	1	1	ON/ON	OFF/FR	OFF/FR	ON/OFF
1	X	0	ON/ON	ON/ON	ON/ON	ON/ON
1	X	1	ON/ON	ON/ON	ON/ON	ON/OFF

Where:

ON = PCI clock is running

OFF = PCI clock is driven low

FR = PCI clock is free running (PLL not locked) clock may stop or run at a frequency less than specified.

The correct operation should look like the Table 4

Table 4.

FORCE_CLKREQ	CPM_EN	BPCC_E	Bridge D State			
			D0	D1	D2	D3
0	0	0	ON/ON	ON/ON	ON/ON	ON/ON
0	0	1	ON/ON	ON/ON	ON/OFF	ON/OFF
0	1	0	ON/ON	ON/ON	ON/ON	ON/ON
0	1	1	ON/ON	ON/ON	OFF/OFF	OFF/OFF
1	X	0	ON/ON	ON/ON	ON/ON	ON/ON
1	X	1	ON/ON	ON/ON	ON/OFF	ON/OFF

Furthermore, if the CLKRUN_EN signal is pulled high, CLKREQ# is incorrectly asserted at all times. However, this does not prevent proper operation of CLKRUN on the PCI bus.

IMPACT:

Implementations that support CLKREQ should reference Table 4 to ensure the PCI device can operate normally.

Workaround:

Set the FORCE_CLKREQ bit to disable CLKREQ support on the pci-express bus.

4 TLP transfer may halt when ASPM L0s is enabled on the chipset and the XIO2001.

Table 5.

Description	The problem has been observed when the XIO2001 is initiating an upstream memory write and a recovery occurs before the chipset sends an acknowledgement in response to the memory write TLP. After the recovery completes, the XIO2001 fails to send anymore TLP or DLLP packets. In order for the problem to occur, ASPM L0s must be enabled on both the chipset and on the XIO2001. It is believed that the recovery occurs because of a bit error detected by the XIO2001.
Impact	The problem can result in system hang since the XIO2001 is no longer to capable of sending any TLP or DLLP packets upstream.
Workaround	Disabling ASPM L0s on either or both the chipset and XIO2001 will prevent the problem from occurring.

5 Internal pull-down resistor on EXT_ARB_EN and CLKRUN_EN does not work.

Table 6.

Description	EXT_ARB_EN and CLKRUN_EN terminals have I/O cells with built-in resistor. However, these resistors were not enabled in the design, leaving them effectively not connected. The datasheet dated May 2012 specifies that these two terminals have internal pull-down which is not the case.
Impact	Leaving these terminals unconnected may cause the voltage level to be detected as either high or low when GRST# de-asserts causing unknown status for these terminal functions.
Workaround	Designs need to ensure that an external resistor is provided on the board to pull the signal either high or low as desired. A 47-kΩ resistor is sufficient.

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