SM320VC33GNMM150
SMJ320VC33HFGM150 / 5962-0053901QYA
SM320VC33GNMM150EP, SM320VC33PGEA120EP
SGYV095C December 2002

VERY LOW POWER, 150 MFLOPS (Million Floating Point Operations Per Second - peak), 32-BIT FLOATING POINT DSP (DIGITAL SIGNAL PROCESSOR)

HIGHLIGHTS

The 320VC33's internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 150 MFLOPS, 75 MIPS (Million Instructions Per Second) and 825 MOPS (Million Operations Per Second) at 75 MHz across the military temperature range (-55°C to 125°C). The 320VC33 optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach supports high performance DSP applications. In addition, for designers needing QML product in a ceramic quad flatpack, the SMJ320VC33 is also available in the 164-lead non-conductive tie bar quad flatpack (the HFG package).

An enhanced plastic processing option is available which provides the benefit of an enhanced qualification pedigree. For more information, go to http://www.ti.com/sc/ep

The 320VC33 can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. The processor also possesses a general-purpose register file, a program cache, two Auxiliary Register Arithmetic Units (ARAUs), internal dual-access memories, one DMA channel supporting concurrent I/O and a short machine-cycle time. High performance and ease of use result.

KEY FEATURES/BENEFITS

High Performance, Very Low Power 320VC33 Digital Signal Processor (DSP):

- 13-ns Instruction Cycle Time
- Up to 150 MFLOPS, 75 MIPS, 825 MOPS @ 75 MHz
- 34K × 32-Bit (1.1-Mbit) On-Chip Words of Dual Access SRAM Configured in 2 × 16K plus 2 x 1K Blocks to Improve Internal Performance
- x5 PLL Clock Generator
- Very Low Power: < 200 mW @ 150 MFLOPS (est.)
- 32-Bit High-Performance CPU
- 16-/ 32-Bit Integer and 32-/ 40-Bit Floating-Point Operations
- Four Internally Decoded Page Strobes to Simplify Interface to I/O and Memory Devices
- 32-Bit Instruction Word, 24-Bit Addresses, EDGEMODE Selectable External Interrupts
- Boot-Program Loader
- On-Chip Memory-Mapped Peripherals:
  - One Serial Port
  - Two 32-Bit Timers
  - Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation
- Fabricated Using the 0.18-micron (Leff — effective gate length) TImeline™ Technology by Texas Instruments
- Eight Extended-Precision Registers
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Two Low-Power Modes
- Two- and Three-Operand Instructions
- Parallel Arithmetic/ Logic Unit (ALU) and Multiplier Execution in a Single Cycle
- Block-Repeat Capability
- Zero-Overhead Loops With Single-Cycle Branches

KEY FEATURES/BENEFITS (continued)

- Conditional Calls and Returns
- Interlocked Instructions for Multiprocessing Support
- Bus-Control Registers Configure Strobe-Control Wait-State Generation
- 1.8-V (Core) and 3.3-V (I/O) Supply Voltages
- On-Chip JTAG Scan-Based Emulation Logic

PROCESS/PERFORMANCE OPTIONS

Device	Package	Speed (MFLOPS)	DSCC SMD	Processing	Order as
SM320VC33GNMM150 ***Available Now***	144-ball, molded-top, non-hermetic, C-BGA	150	N/A	-55°C to +125°C Military Temp, Commercial Processing	SM320VC33GNMM150
SM320VC33GNMM150EP ***Available Now***	144-ball, molded top, non-hermetic, C-BGA	150	N/A	-55°C to +125°C Military Temp, Enhanced Plastic	SM320VC33GNMM150EP
SMJ320VC33HFGM150 ***Available Now***	164-lead, hermetic, NCTB CQFP	150	5962-0053901QYA	-55°C to +125°C Military Temp, Full Military QML Processing	SMJ320VC33GNLM150 or 5962-0053901QYA
SM320VC33PGEA120EP ***Available Now***	144-pin, non-hermetic, LQFP	120	N/A	-40°C to +100°C Enhanced Plastic	SM320VC33PGEA120EP
SM320VC33PGEA150EP ***Potential Product***	144-pin, non-hermetic, LQFP	150	N/A	-40°C to +100°C Enhanced Plastic	Contact PIC for availability

DIE SIZE

The die size of the VC33: 217 x 198 mils.
Bond pad size: 102.5 microns
Bond pad pitch: 70 microns

TECHNOLOGY

4-Level Metal 0.18-micron effective (TImeline™) CMOS Process Technology
3.3-volt I/Os, 1.8-volt Core
ESD Level = Class II (2 kV to 3,999 kV)

POWER DISSIPATION

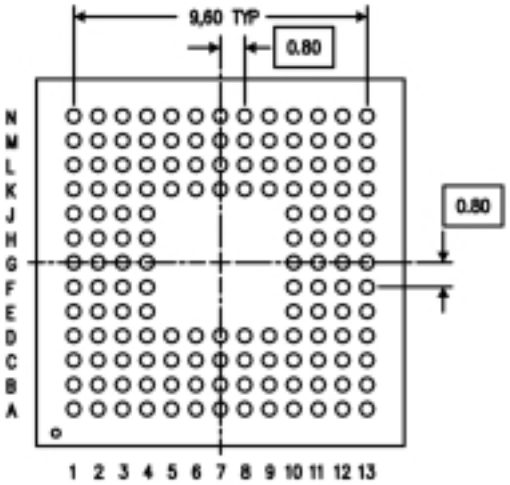
The VC33 dissipates less than 200 mW at 75 MHz (est.).

PACKAGE THERMAL CHARACTERISTICS and WEIGHT

GNM / 144-ball, molded-top BGA: Rθja = 27.2° C/W, Rθjc* = 17.4°C/W per JEDEC Std. 51
GNM Package weight including die = 0.481 grams
HFG / 164-lead, CQFP; Rθja = 35°C/W, Rθjc** = 2°C/W
HFG Package weight including die - 12.60 grams

* Measured to the top of the package
** Thermal resistance assuming an infinite path for heat dissipation.

VC33 FINE-PITCH, BALL GRID ARRAY PACKAGE INFORMATION

Package	Details
144-ceramic ball grid array (BGA) package (bottom view, in millimeters) 	12 x 12 mm package outline. Reduced parasitics for improved performance Ultra thin package (2.4 mm for the GNM and 2.7 mm for the GNL packages) supports military trend for higher integration and minimizing board space 0.8 mm pitch on 63% Sn, 37% Pb solderballs Two package options (hermetic metal lid and non-hermetic, molded top) available to meet a variety of customer requirements: • GNL = Metal lid, ceramic base, hermetic* • GNM = Molded top, ceramic base, non-hermetic

NOMENCLATURE

SM — SMJ = MIL-PRF-38535 (QML); SM = Commercial Processing

320 — DSP Family

VC33 — Device

GNM — Package:
GNM = Molded lid, Ceramic, 144-Ball Grid Array/ Non-hermetic
HFG = Ceramic 164-lead NCTB QFP/Hermetic
PGE = Low Profile Quad Flatpack/Non-Hermetic

M — M = Mil-temp (-55°C – 125°C)

150 — Speed: 150 = 150 MFLOPs

EP — Enhanced Plastic

SUPPORT

You can access data sheets via TI's home page on the internet (http://www.ti.com) or reference the literature number SGUS033 (available 4Q00) when contacting the Product Information Center (PIC).

For additional information on this and other military DSP products, contact the PIC or visit our military semiconductors home page at: http://www.ti.com/sc/military.

Development tool information is on the web at: http://dspvillage.ti.com/docs/tools/dsp/index.htm

Product Information Center

North America
Telephone # - 972-644-5580 (English)
Fax # - 972-480-7800
PIC – http://www.ti.com/sc/docs/pic/home.htm
PIC E-mail - sc-infomaster@ti.com
Military Products – http://www.ti.com/sc/docs/products/military/overview.htm
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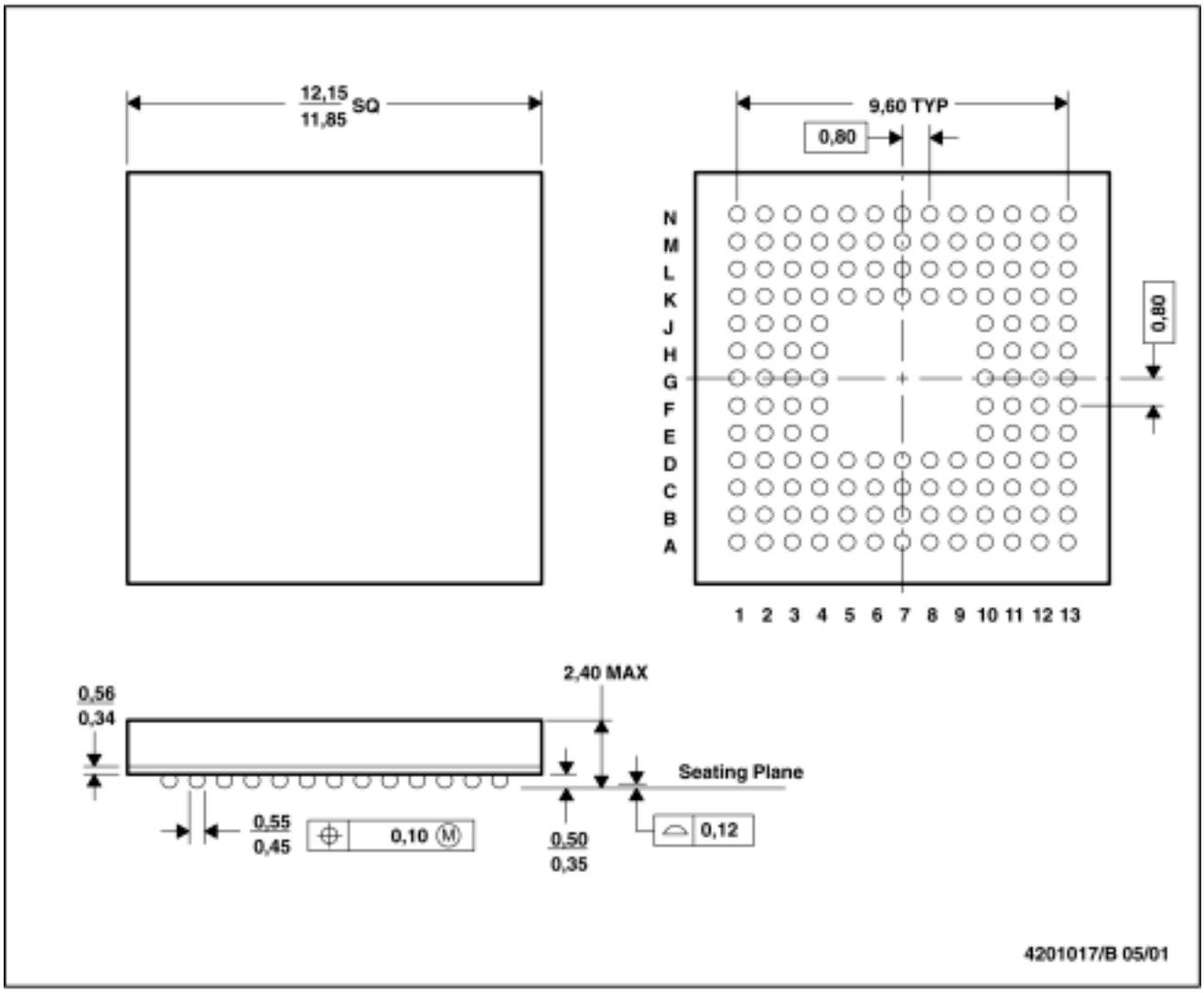
TEXAS INSTRUMENTS

The molded top, CBGA (GNM) package is used for production of the non-hermetic VC33 DSP.

GNM (S-CBGA-N144) **CERAMIC BALL GRID ARRAY**

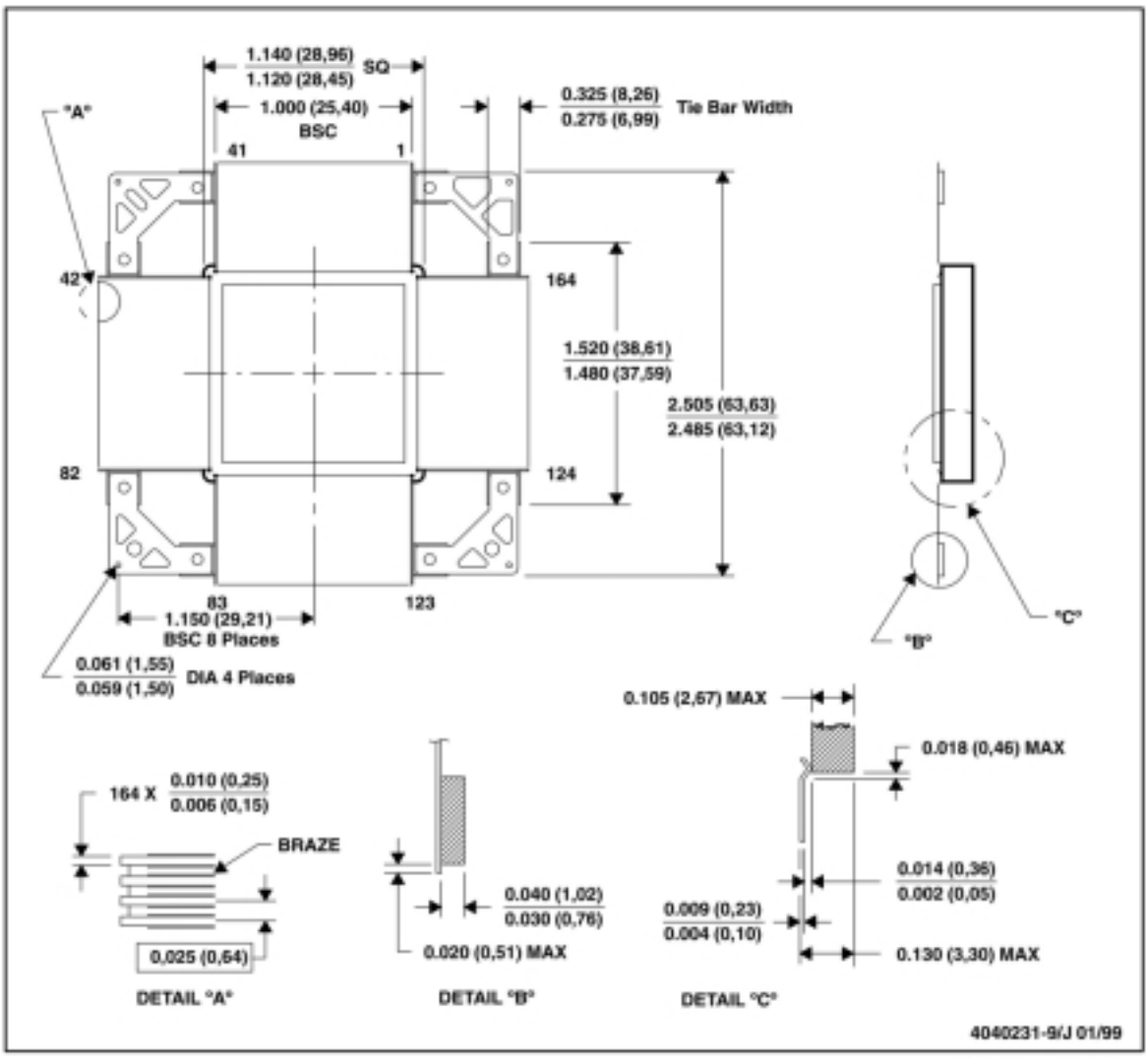


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is not a controlled drawing.

NON-HERMETIC VERSION

The non-conductive tie bar (NCTB), ceramic quad flatpack (HFG) package is a package for designers desiring a non-ball grid array package option.

HFG (S±CQFP±F164) **CERAMIC QUAD FLATPACK WITH NCTB**

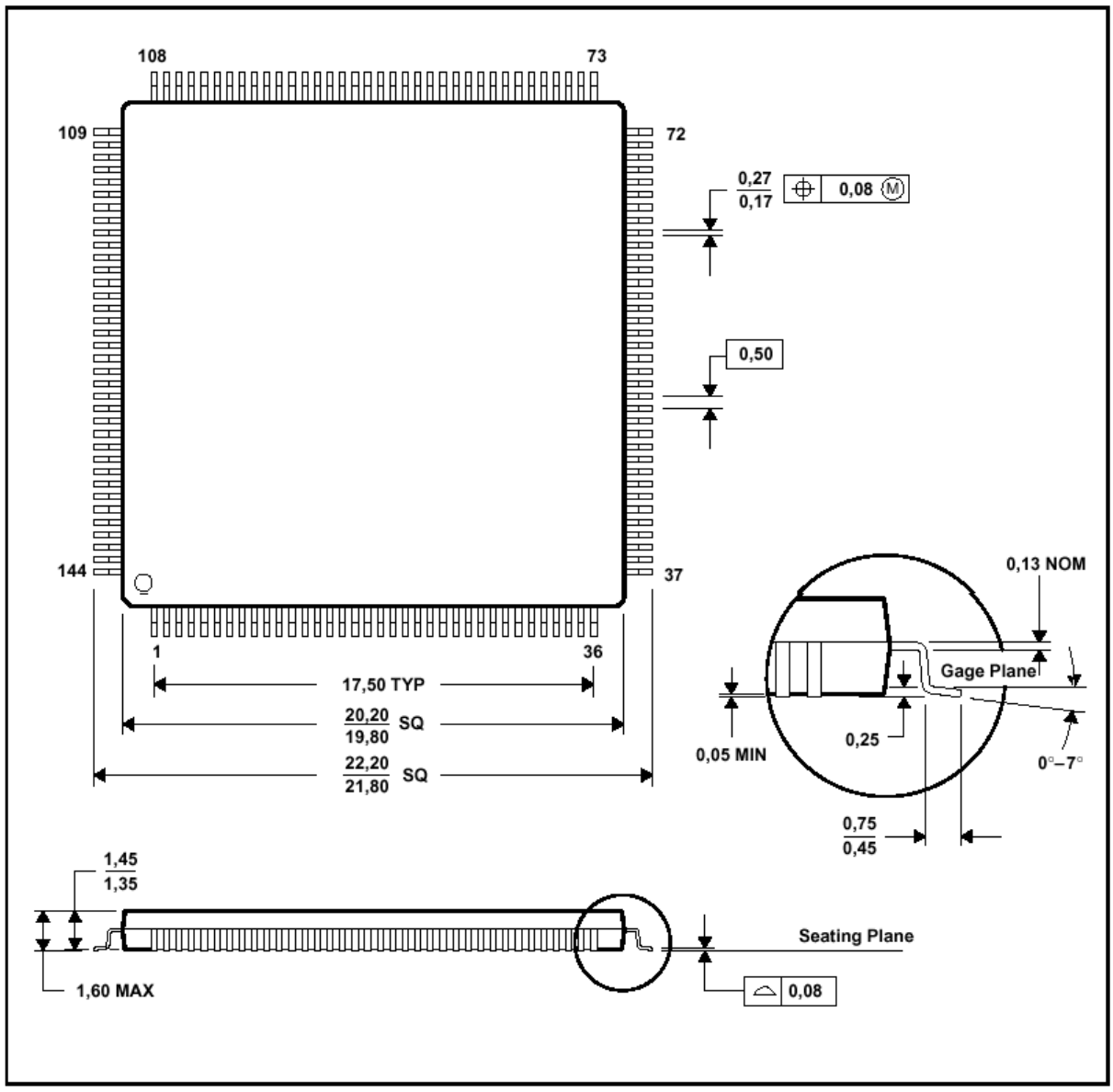


MCQF012 ± JUNE 1999

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier
D. This package is hermetically sealed with a metal lid.
E. The leads are gold-plated and can be solder-dipped.
F. Leads not shown for clarity purposes
G. Falls within JEDEC MO-113AA (REV D)

The 144-pin low profile quad flatpack (LQFP) (PGE suffix) is available for designers who do not need a hermetic package. This package is for the SM320VC33PGEAXXXEP only. (XXX = 120 or 150 MHz)

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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