

Regulating Pulse Width Modulator

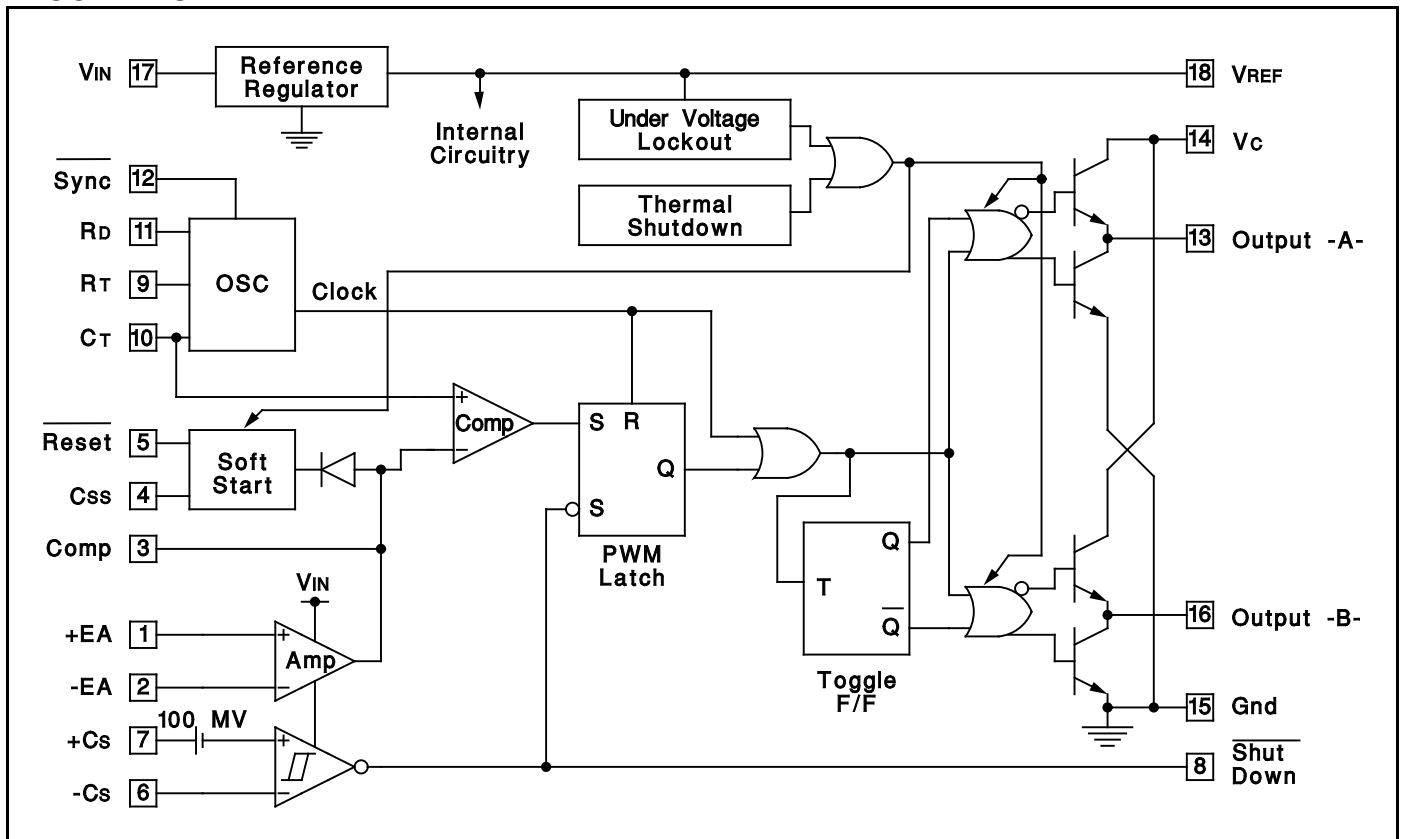
FEATURES

- 8 To 35V Operation
- 5V Reference Trimmed To $\pm 1\%$
- 1Hz To 400kHz Oscillator Range
- Dual 100mA Source/Sink Outputs
- Digital Current Limiting
- Double Pulse Suppression
- Programmable Deadtime
- Under-Voltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- TTL/CMOS Compatible Logic Ports
- Symmetry Correction Capability
- Guaranteed 6 Unit Synchronization

DESCRIPTION

The UC1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and setting logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The UC1526 is characterized for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$. The UC2526 is characterized for operation from -25°C to $+85^{\circ}\text{C}$, and the UC3526 is characterized for operation from 0° to $+70^{\circ}\text{C}$.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

| | |
|--|-----------------|
| Input Voltage (+VIN) | +40V |
| Collector Supply Voltage (+Vc) | +40V |
| Logic Inputs | -0.3V to +5.5V |
| Analog Inputs | -0.3V to +VIN |
| Source/Sink Load Current (each output) | 200mA |
| Reference Load Current | 50mA |
| Logic Sink Current | 15mA |
| Power Dissipation at TA = +25°C (Note 2) | 1000mW |
| Power Dissipation at Tc = +25°C (Note 2) | 3000mW |
| Operating Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10 seconds) | +300°C |

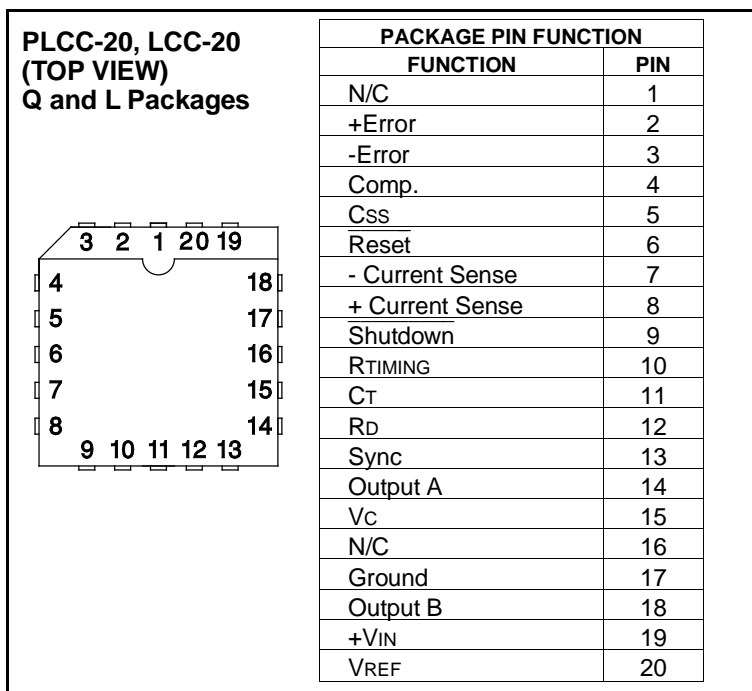
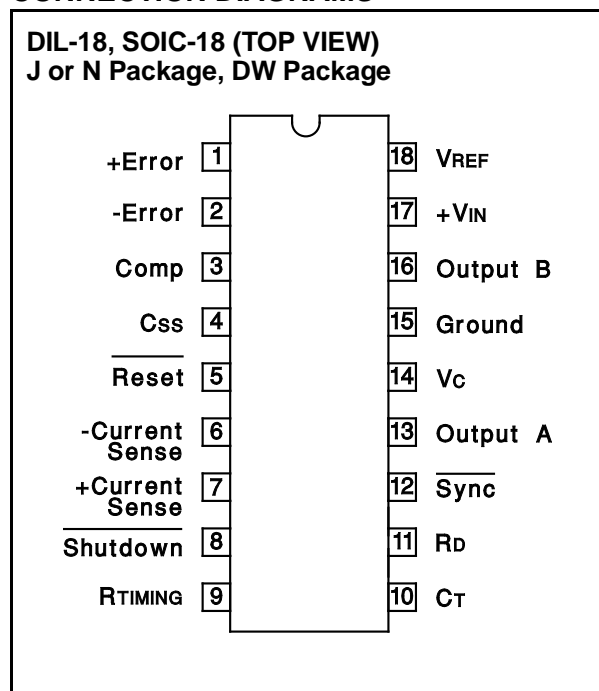
Note 1: Values beyond which damage may occur.
 Note 2: Consult packaging section of databook for thermal limitations and considerations of package.

RECOMMENDED OPERATING CONDITIONS (Note 3)

| | |
|--|-----------------|
| Input Voltage | +8V to +35V |
| Collector Supply Voltage | +4.5V to +35V |
| Sink/Source Load Current (each output) | 0 to 100mA |
| Reference Load Current | 0 to 20mA |
| Oscillator Frequency Range | 1Hz to 400kHz |
| Oscillator Timing Resistor | 2kΩ to 150kΩ |
| Oscillator Timing Capacitor | 1nF to 20μF |
| Available Deadtime Range at 40kHz | 3% to 50% |
| Operating Ambient Temperature Range | |
| UC1526 | -55°C to +125°C |
| UC2526 | -25°C to +85°C |
| UC3526 | -0°C to +70°C |

Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS



ELECTRICAL CHARACTERISTICS: +VIN = 15V, and over operating ambient temperature, unless otherwise specified, TA = Tj.

| PARAMETER | TEST CONDITIONS | UC1526 / UC2526 | | | UC3526 | | | UNITS |
|-----------------------------------|---------------------------------------|-----------------|------|------|--------|------|------|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Reference Section (Note 4) | | | | | | | | |
| Output Voltage | TJ = + 25°C | 4.95 | 5.00 | 5.05 | 4.90 | 5.00 | 5.10 | V |
| Line Regulation | +VIN = 8 to 35V | | 10 | 20 | | 10 | 30 | mV |
| Load Regulation | IL = 0 to 20mA | | 10 | 30 | | 10 | 50 | mV |
| Temperature Stability | Over Operating TJ | | 15 | 50 | | 15 | 50 | mV |
| Total Output Voltage Range | Over Recommended Operating Conditions | 4.90 | 5.00 | 5.10 | 4.85 | 5.00 | 5.15 | V |
| Short Circuit Current | VREF = 0V | 25 | 50 | 100 | 25 | 50 | 100 | mA |
| Under -Voltage Lockout | | | | | | | | |
| RESET Output Voltage | VREF = 3.8V | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| | VREF = 4.8V | 2.4 | 4.8 | | 2.4 | 4.8 | | V |

Note 4: IL = 0mA.

ELECTRICAL CHARACTERISTICS: +VIN = 15V, and over operating ambient temperature, unless otherwise specified, TA = TJ.

| PARAMETER | TEST CONDITIONS | UC1526 / UC2526 | | | UC3526 | | | UNITS |
|--|--------------------------------------|-----------------|------|-------|--------|------|-------|-------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Oscillator Section (Note 5) | | | | | | | | |
| Initial Accuracy | TJ = + 25°C | | ±3 | ±8 | | ±3 | ±8 | % |
| Voltage Stability | +VIN = 8 to 35V | | 0.5 | 1 | | 0.5 | 1 | % |
| Temperature Stability | Over Operating TJ | | 7 | 10 | | 3 | 5 | % |
| Minimum Frequency | RT = 150kΩ, CT = 20μF | | | 1 | | | 1 | Hz |
| Maximum Frequency | RT = 2kΩ, CT = 1.0nF | 400 | | | 400 | | | kHz |
| Sawtooth Peak Voltage | +VIN = 35V | | 3.0 | 3.5 | | 3.0 | 3.5 | V |
| Sawtooth Valley Voltage | +VIN = 8V | 0.5 | 1.0 | | 0.5 | 1.0 | | V |
| Error Amplifier Section (Note 6) | | | | | | | | |
| Input Offset Voltage | Rs ≤ 2kΩ | | 2 | 5 | | 2 | 10 | mV |
| Input Bias Current | | | -350 | -1000 | | -350 | -2000 | nA |
| Input Offset Current | | | 35 | 100 | | 35 | 200 | nA |
| DC Open Loop Gain | RL ≥ 10MΩ | 64 | 72 | | 60 | 72 | | dB |
| HIGH Output Voltage | VPIN1-VPIN2 ≥ 150mV, ISOURCE = 100μA | 3.6 | 4.2 | | 3.6 | 4.2 | | V |
| LOW Output Voltage | VPIN2-VPIN1 ≥ 150mV, ISINK = 100μA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| Common Mode Rejection | Rs ≤ 12kΩ | 70 | 94 | | 70 | 94 | | dB |
| Supply Voltage Rejection | +VIN = 12 to 18V | 66 | 80 | | 66 | 80 | | dB |
| PWM Comparator (Note 5) | | | | | | | | |
| Minimum Duty Cycle | VCOMPENSATION = +0.4V | | | 0 | | | 0 | % |
| Maximum Duty Cycle | VCOMPENSATION = +3.6V | 45 | 49 | | 45 | 49 | | % |
| Digital Ports (SYNC, SHUTDOWN, and RESET) | | | | | | | | |
| HIGH Output Voltage | ISOURCE = 40μA | 2.4 | 4.0 | | 2.4 | 4.0 | | V |
| LOW Output Voltage | ISINK = 3.6mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| HIGH Input Current | VIH = +2.4V | | -125 | -200 | | -125 | -200 | μA |
| LOW Input Current | VIL = +0.4V | | -225 | -360 | | -225 | -360 | μA |
| Current Limit Comparator (Note 7) | | | | | | | | |
| Sense Voltage | Rs ≤ 50Ω | 90 | 100 | 110 | 80 | 100 | 120 | mV |
| Input Bias Current | | | -3 | -10 | | -3 | -10 | μA |
| Soft-Start Section | | | | | | | | |
| Error Clamp Voltage | RESET = +0.4V | | 0.1 | 0.4 | | 0.1 | 0.4 | V |
| Cs Charging Current | RESET = +2.4V | 50 | 100 | 150 | 50 | 100 | 150 | μA |
| Output Drivers (Each Output) (Note 8) | | | | | | | | |
| HIGH Output Voltage | ISOURCE = 20mA | 12.5 | 13.5 | | 12.5 | 13.5 | | V |
| | ISOURCE = 100mA | 12 | 13 | | 12 | 13 | | V |
| LOW Output Voltage | ISINK = 20mA | | 0.2 | 0.3 | | 0.2 | 0.3 | V |
| | ISINK = 100mA | | 1.2 | 2.0 | | 1.2 | 2.0 | V |
| Collector Leakage | VC = 40V | | 50 | 150 | | 50 | 150 | μA |
| Rise Time | CL = 1000pF | | 0.3 | 0.6 | | 0.3 | 0.6 | μs |
| Fall Time | CL = 1000pF | | 0.1 | 0.2 | | 0.1 | 0.2 | μs |
| Power Consumption (Note 9) | | | | | | | | |
| Standby Current | SHUTDOWN = +0.4V | | 18 | 30 | | 18 | 30 | mA |

Note 4: IL = 0mA.

Note 5: FOSC = 40kHz (RT = 4.12kΩ ± 1%, CT = 0.1μF ± 1%, RD = 0Ω)

Note 6: VCM = 0 to +5.2V

Note 8: VC = +15V

Note 9: +VIN = +35V, RT = 4.12kΩ

APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

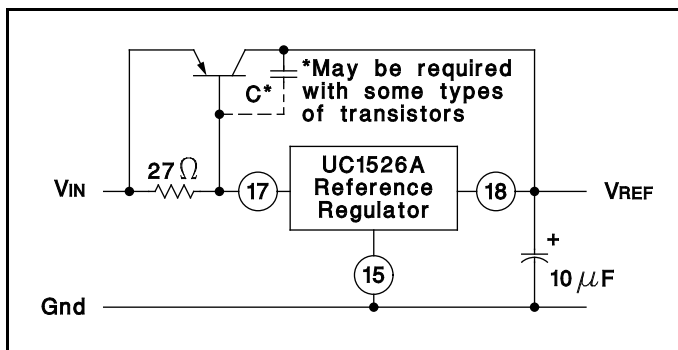


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526 and the power devices it controls from inadequate supply voltage. If +VIN is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$ or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When +VIN to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526 can operate from a +5V supply by connecting the VREF pin to the +VIN pin and maintaining the supply between +4.8 and +5.2V.

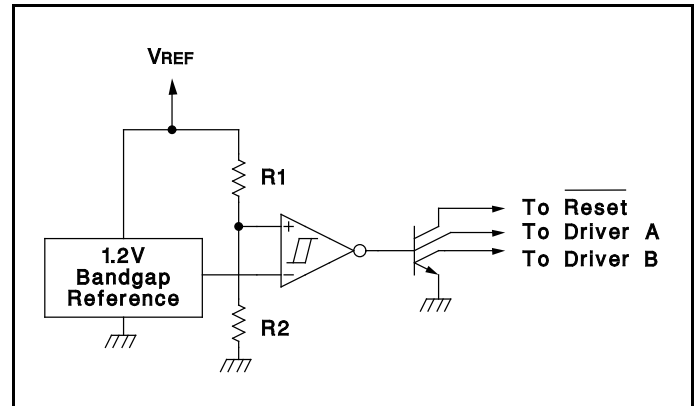


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q3. Q1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q1 turns off, allowing the internal 100mA current source to charge Cs. Q2 clamps the error amplifier output to $1V_{BE}$ above the voltage on Cs. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

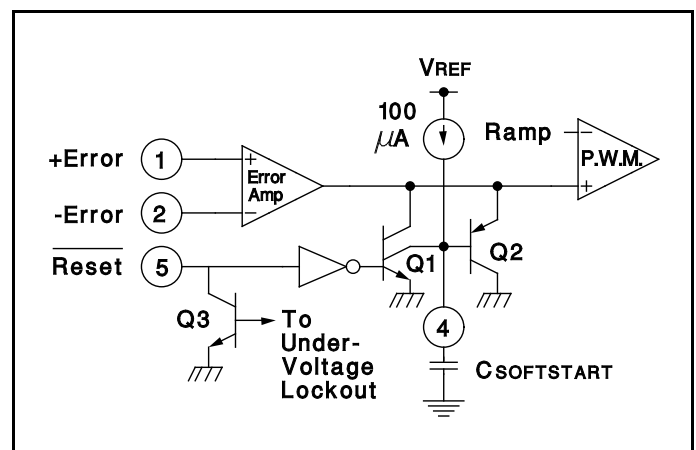


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526 are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector

APPLICATIONS INFORMATION (cont.)

TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

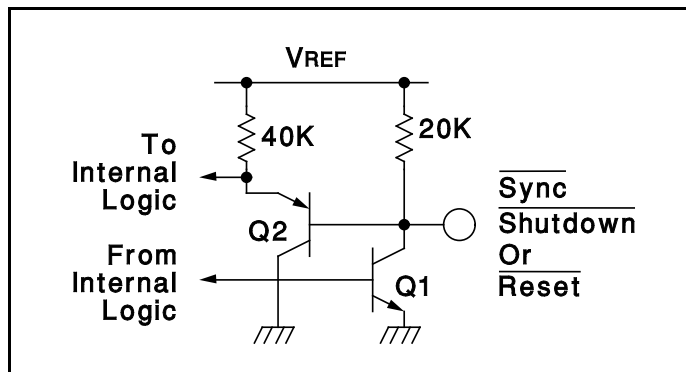


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: R_T , C_T and R_D . Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With $R_D = 0$ (pin 11 shorted to ground) select values for R_T and C_T from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the +Vc terminal is the same as the oscillator frequency.
2. If more dead time is required, select a large value of R_D . At 40kHz dead time increases by 400ns/ Ω .
3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The UC1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5 μ s wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave R_T terminals are left open or connected to V_{REF} . Slave R_D terminals may be either left open or grounded.

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2M Ω . Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

Output Drivers

The totem-pole output drivers of the UC1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the +Vc, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the +Vc terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents.

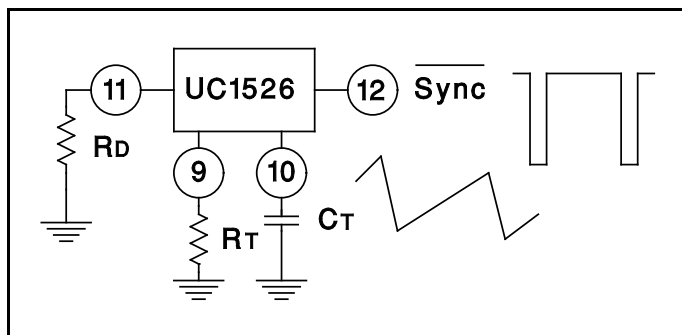


Figure 5. Oscillator Connections and Waveforms

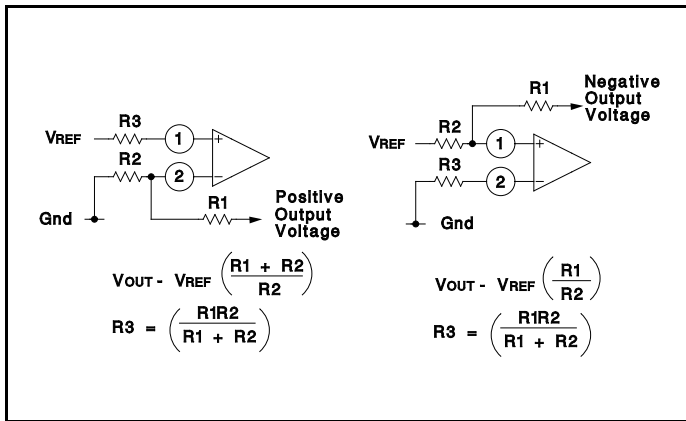


Figure 6. Error Amplifier Connections

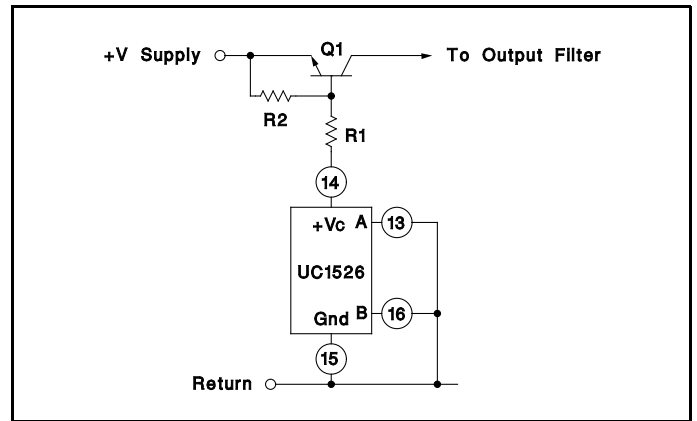


Figure 8. Single-Ended Configuration

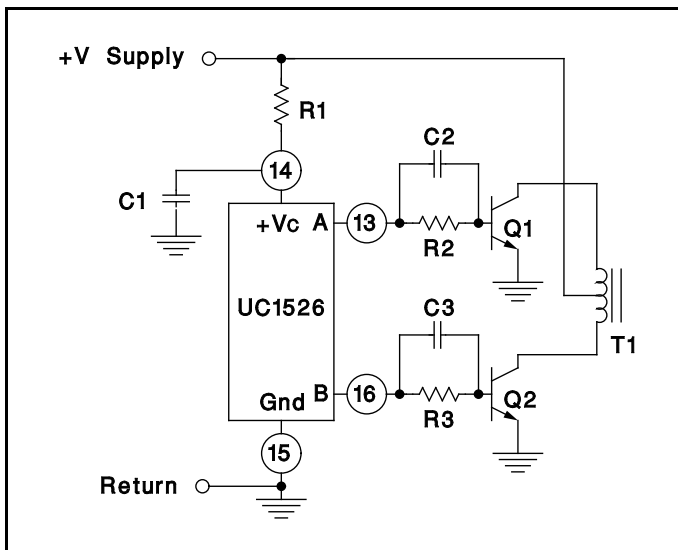


Figure 7. Push-Pull Configuration

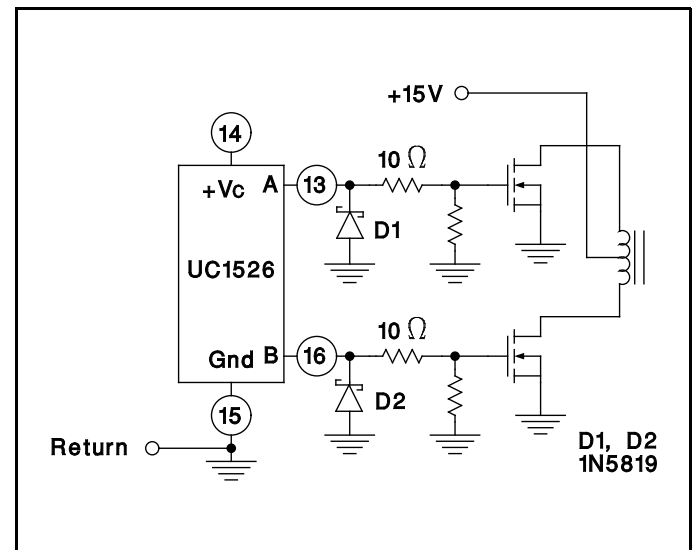
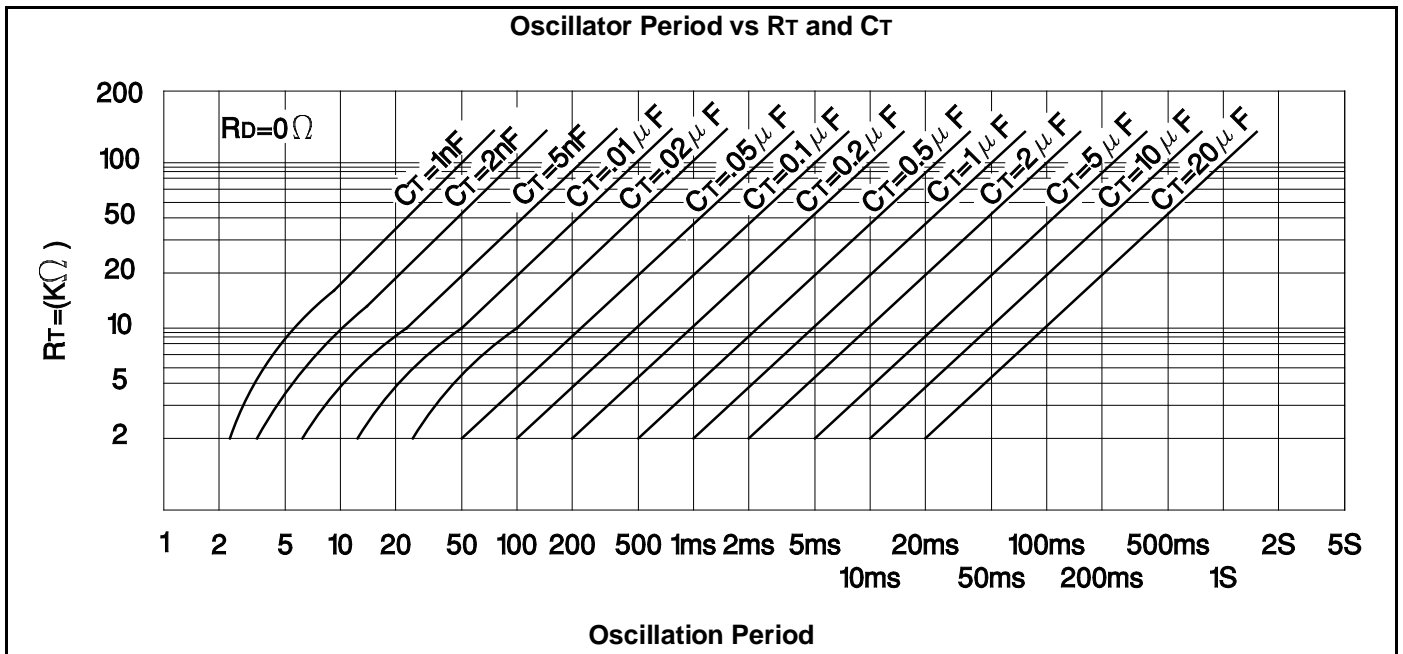
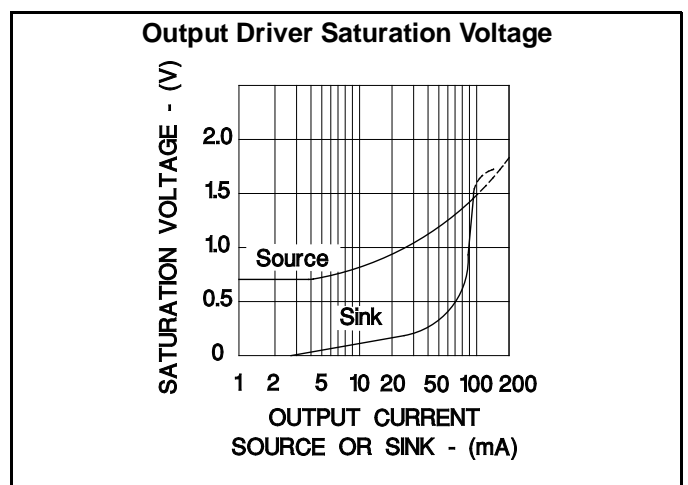
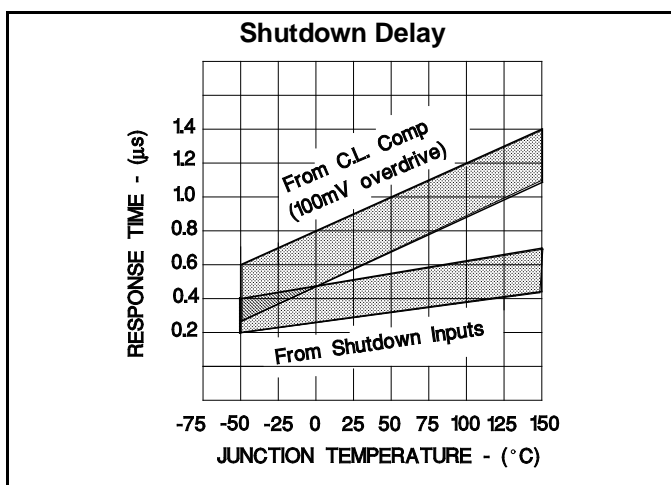
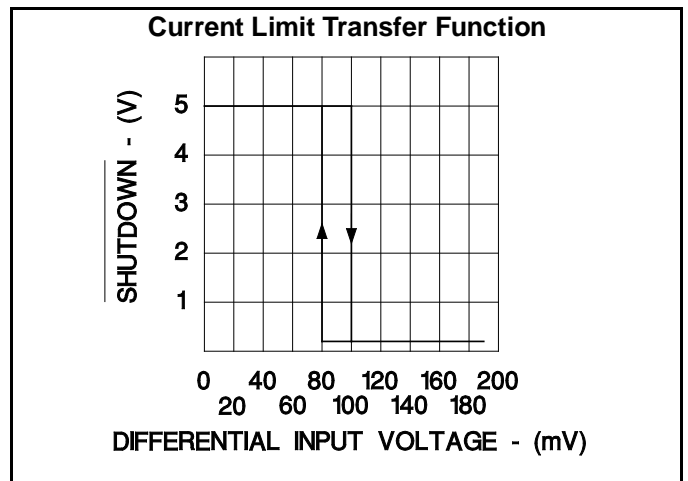
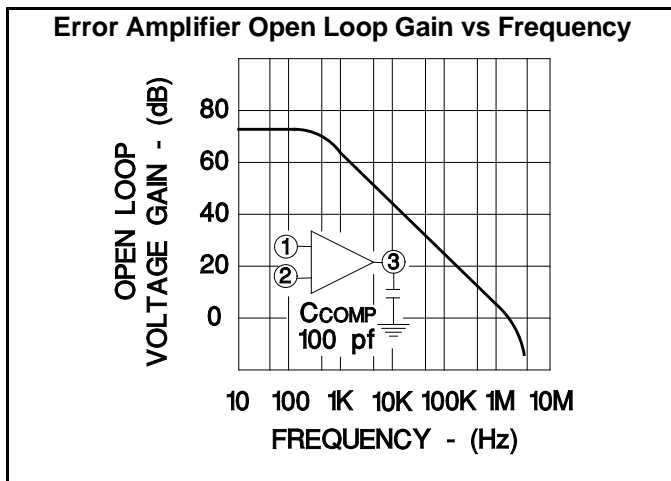
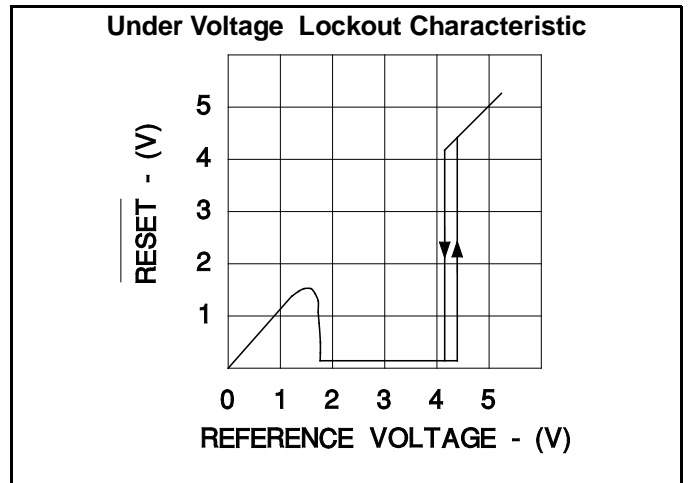
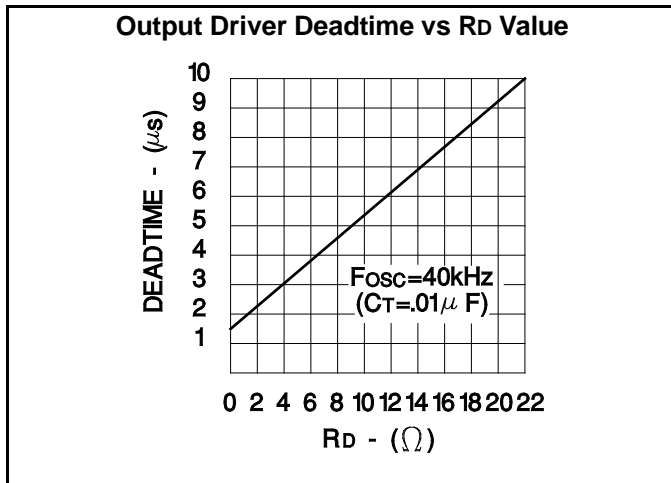


Figure 9. Driving N-channel Power Mosfets

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---------------------------|-------------------------|
| 8551501VA | ACTIVE | CDIP | J | 18 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8551501VA UC1526J/883B | Samples |
| UC1526J | ACTIVE | CDIP | J | 18 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | UC1526J | Samples |
| UC1526J883B | ACTIVE | CDIP | J | 18 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8551501VA UC1526J/883B | Samples |
| UC2526AJ | ACTIVE | CDIP | J | 18 | 1 | TBD | A42 | N / A for Pkg Type | -25 to 85 | UC2526AJ | Samples |
| UC2526N | ACTIVE | PDIP | N | 18 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -25 to 85 | UC2526N | Samples |
| UC2526NG4 | ACTIVE | PDIP | N | 18 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | -25 to 85 | UC2526N | Samples |
| UC3526AJ | ACTIVE | CDIP | J | 18 | 1 | TBD | A42 | N / A for Pkg Type | 0 to 70 | UC3526AJ | Samples |
| UC3526DW | ACTIVE | SOIC | DW | 18 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3526DW | Samples |
| UC3526DWG4 | ACTIVE | SOIC | DW | 18 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3526DW | Samples |
| UC3526DWTR | ACTIVE | SOIC | DW | 18 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3526DW | Samples |
| UC3526N | ACTIVE | PDIP | N | 18 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3526N | Samples |
| UC3526NG4 | ACTIVE | PDIP | N | 18 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | UC3526N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC1526, UC2526, UC2526AM, UC3526, UC3526AM :

- Catalog: [UC3526](#), [UC2526A](#), [UC3526M](#), [UC3526A](#)
- Military: [UC2526M](#), [UC1526](#), [UC1526A](#)

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- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

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