High-Performance Synchronous Buck EVM Using the TPS51220

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1 Description

The TPS51220 is a dual, peak-current mode, synchronous step-down controller with three low-dropout (LDO) regulators. It is optimized for 5-V /3.3-V notebook system power supplies. A 99% duty cycle operation enables designers to complete Li-ion battery applications from 2-cells to 4-cells cost effectively. The TPS51220 supports high-efficiency, fast transient response and 99% duty cycle operation. DCR current sensing provides lossless current sensing and free MOSFET selection; resistor sensing supports accurate current-sensing operation. It supports supply input voltages ranging from 4.5 V to 30 V and output voltages from 1 V to 12 V. High-current, 5 V at 100 mA, 3.3 V at 10 mA, onboard linear regulators have glitch-free switchover function to SMPS, and the 2-V reference has a 100-µA capability.

A peak current-sensing current mode and fixed-frequency control scheme support the full range of current mode operation including simplified loop compensation, ceramic output capacitors, as well as a seamless transition to reduced frequency operation at light-load condition.

This evaluation module demonstrates the performance of the high-current/ high-efficiency TPS51220 buck converter

2 Electrical Performance

SPECIFICATIONS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range (VIN)		8	12	20	V
CH1	Output voltage			5		V
	Operating frequency	VIN = 12 V, Iout1 = 6 A		280		kHz
	Output current	VIN = 8 V to 20 V	6			A
	Over current limit	VIN = 12 V		9		A
	Output ripple voltage	VIN = 12 V, Iout1 = 6 A		15		mVp-p
CH2	Output voltage			3.3		V
	Operating frequency	VIN = 12 V, Iout2 = 6 A		280		kHz
	Output current	VIN = 8 V to 20 V	6			A
	Over current limit	VIN = 12 V		9		A
	Output ripple voltage	VIN = 12 V, Iout2 = 6 A		15		mVp-p

3 Schematic

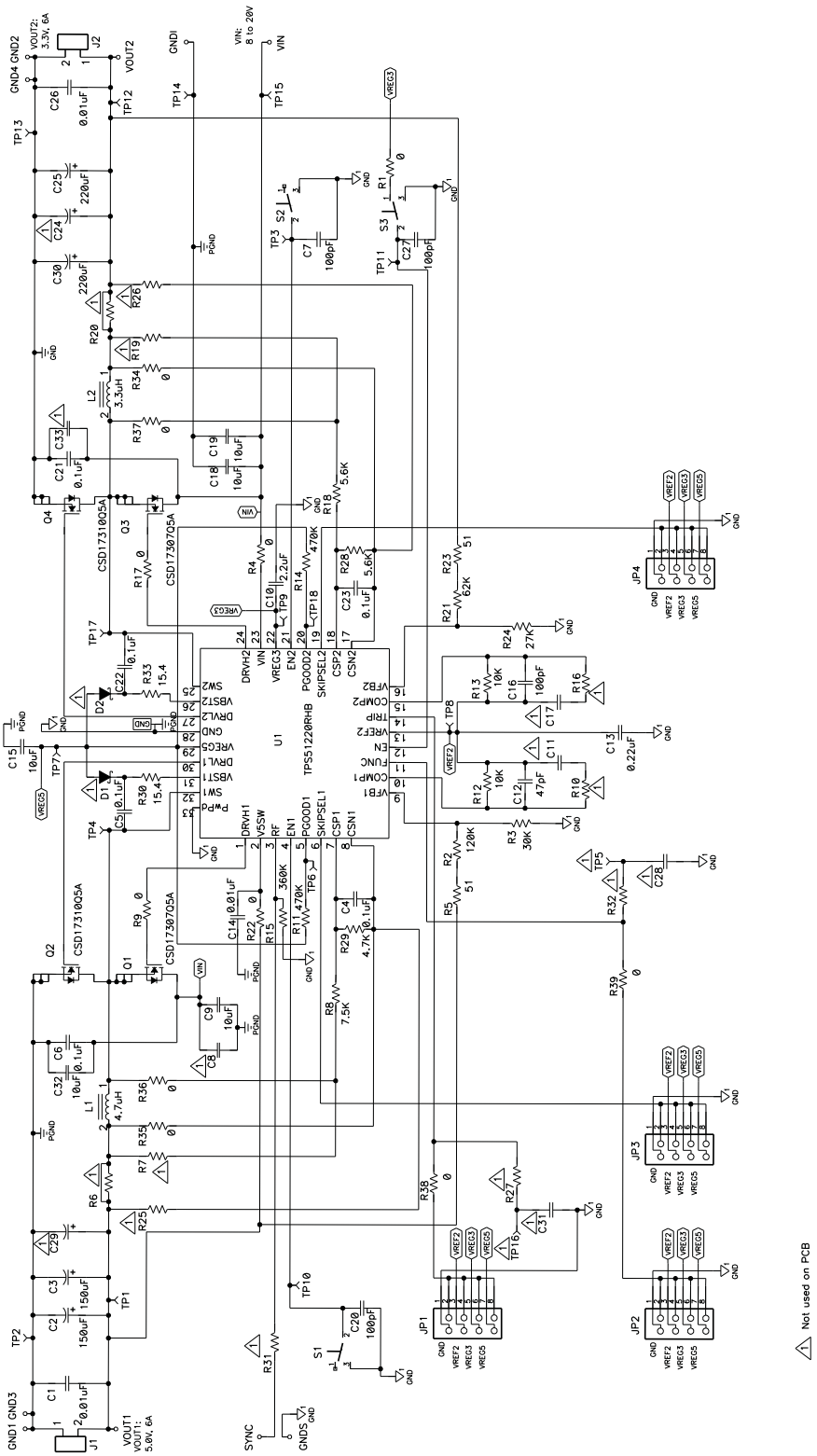

Figure 1. HPA302 EVM Schematic Diagram (DCR-Sensing)

4 Test Setup and Procedure

4.1 Test Setup

Connect test equipment and HPA302-EVM board as shown in Figure 2.

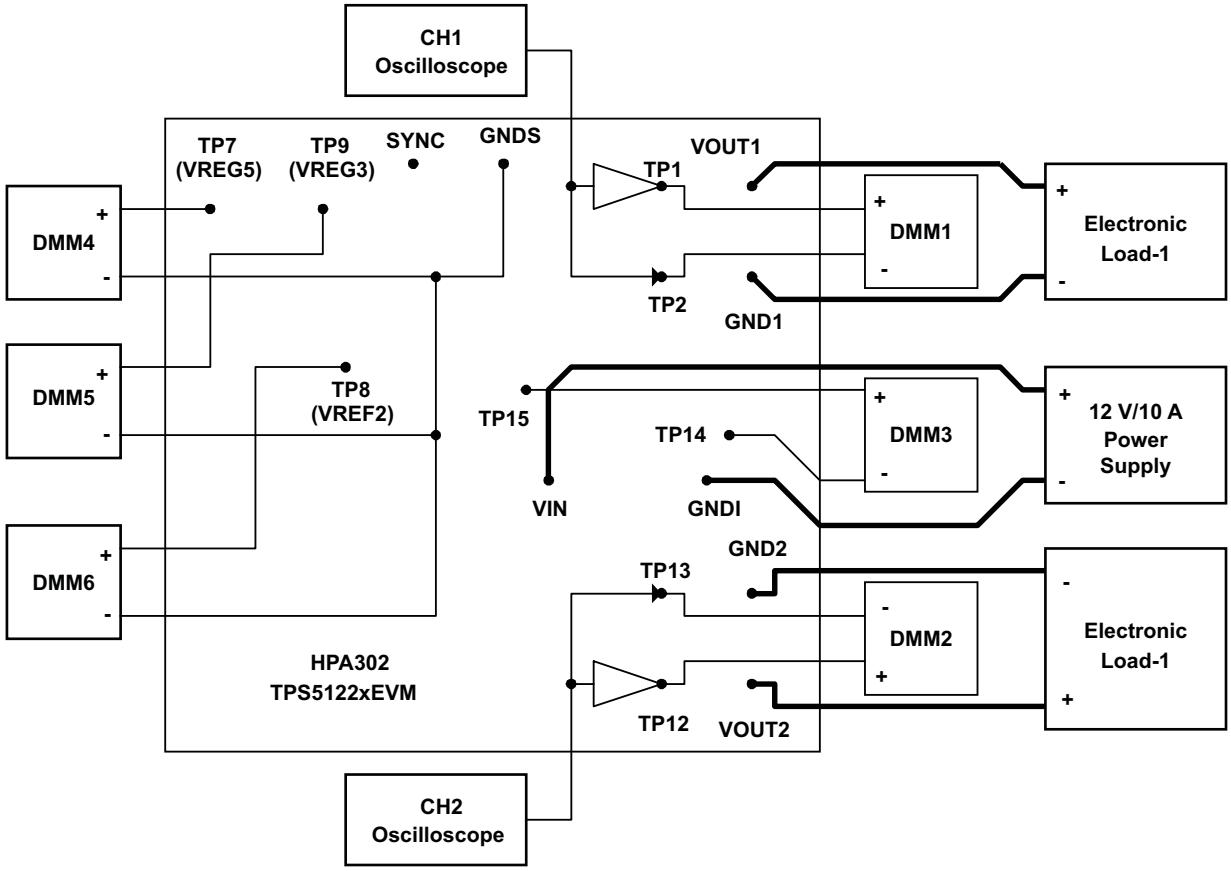

Figure 2. Equipment Setup for TPS51220EVM Board

4.2 Test Procedure

1. Ensure that the switches S1 (EN1), S2 (EN2), and S3 (EN) are in OFF position.
2. Ensure that the shunt jumpers for JP1 (TRIP) is set 7-pin to 8-pin (VREG5; Vocl = 60 mV, Discharge-enabled), JP2 (FUNC) is set 1-pin to 2-pin (GND; UVP/OVP-enabled), and JP3, JP4 are set 3-pin to 4-pin (VREF2; Auto-skip).
3. Apply appropriate VIN voltage to VIN and GNDI terminals. Check that VREG3 (3.3V-LDO) starts up.
4. Turn S3 (EN) to ON. Check that VREG5 (5V-LDO) and VREF2 (2V-Ref) start up.
5. When S1 (EN1) is turned to ON, CH1-output starts up.
6. When S2 (EN2) is turned to ON, CH2-output starts up.

5 Configuration

Users can configure this EVM per the following configurations.

5.1 Switching Frequency Selection

The switching frequency can be set by the RF-resistor (R15) or applying external clock into RF pin on the EVM.

Default setting is 280-kHz using RF resistor.

Table 1. Switching Frequency Selection

	Connection
Internal	Add RF-resistor from RF to GND and be R31 open $f_{sw} = \frac{1 \times 10^8}{RF[\Omega]}$ [kHz]
External	Apply external clock signal to SYNC (5 Vpp and 50% duty) , remove R15 in addition, and add 0-Ω to R31.

5.2 Skip Mode and Control Scheme Selection

The skip mode can be set by the SKIPSEL1,2 pins using JP3 and JP4 on the EVM.

Default setting is Auto-skip.

Table 2. Skip Mode Selection

Jumper (JP3, JP4) set to	SKIPSEL1,2	Skip
Top (1-2 pin shorted)	GND	CCM
Second (3-4 pin shorted)	**VREF2**	**Auto-skip**
Third (5-6 pin shorted)	VREG3	OOA (<400-kHz)
Bottom (7-8 pin shorted)	VREG5	OOA (>400-kHz)

5.3 Current-Sensing Selection

The current-sensing scheme can be set by the external current sensing devices, using some resistors on the EVM.

Default setting is Inductor DCR sensing

Table 3. Current-Sensing Scheme Selection (CH1)

	R8	R29	R35	R36	R6	R7	R25
Inductor DCR	**Put on (1)**	**Put on (1) (if necessary)**	**Put on (1)**	**Put on (1)**	**Open**	**Open**	**Open**
External Resistor	Put on(1)	Put on(1) (if necessary)	Put on(1)	Open	Put on (1) Cut trace	Open	Open

(1) "Put on" means add appropriate resistor.

Table 4. Current Sensing Scheme Selection (CH2)

	R18	R28	R33	R37	R20	R19	R26
Inductor DCR	**Put on (1)**	**Put on (1) (if necessary)**	**Put on (1)**	**Put on (1)**	**Open**	**Open**	**Open**
External Resistor	Put on(1)	Put on(1) (if necessary)	Put on(1)	Open	Put on (1) Cut trace	Open	Open

(1) "Put on" means add appropriate resistor.

For external resistor sensing, cut the trace as follows.

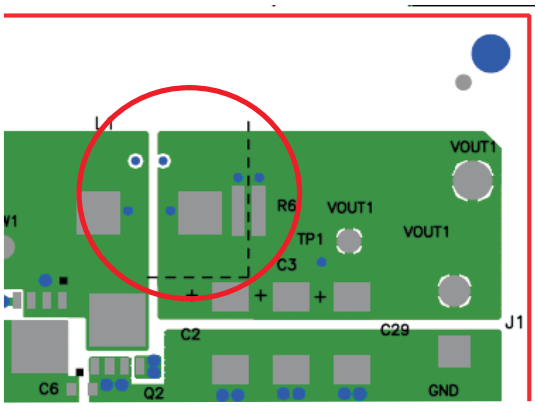

Figure 3. (CH1) Cut Trace Underneath R6

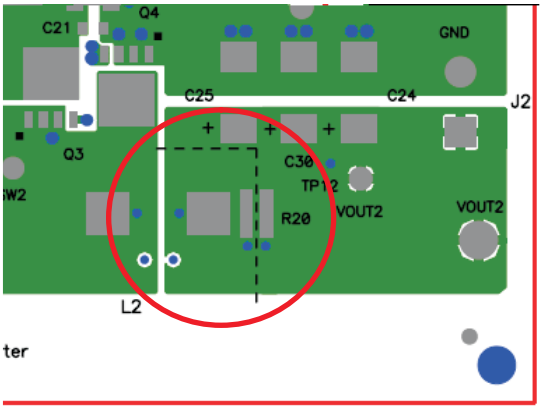

Figure 4. (CH2) Cut Trace Underneath R20

5.4 Overcurrent Limit and Discharge Selection

The overcurrent limit threshold and discharge function can be set by the TRIP pin using JP1 on the EVM.

Default setting is 60 mV and discharge enabled.

Table 5. TRIP/ Discharge Mode Selection

Jumper (JP2) set to	TRIP	VOCL	Discharge
Top (1-2 pin shorted)	GND	31 mV	Enabled
Second (3-4 pin shorted)	VREF2	31 mV	Disabled
Third (5-6 pin shorted)	VREG3	60 mV	Disabled
Bottom (7-8 pin shorted)	**VREG5**	**60 mV**	**Enabled**

5.5 Control Mode and Protection Selection

The control mode and protection function can be set by the FUNC pin using JP2 on the EVM.

Default setting is current mode and UVP/OVP-enabled.

Table 6. Control Mode/OVP Selection

Jumper (JP2) set to	FUNC	Mode	OVP
Top (1-2 pin shorted)	**GND**	**Current**	**Enabled**
Second (3-4 pin shorted)	VREF2	D-CAP	Disabled
Third (5-6 pin shorted)	VREG3	D-CAP	Enabled
Bottom (7-8 pin shorted)	VREG5	Current	Disabled

5.6 Soft-Start Setting Selection

Output voltage soft-start time can be set by the ENx pin using some capacitors on the EVM.

Default setting is integrated soft start.

Table 7. Soft-Start Setting Selection[(1)]

	CH1 (C20)	**CH2 (C7)**
Integrated soft start	**Open** (adding small bypass-capacitor; 100 pF)	Open (adding small bypass-capacitor; 100 pF)
External soft start	Put on	Put on

(1) When external soft start is selected, add appropriate capacitor on C20 and/or C7.)

5.7 Output Voltage Adjustment

Output voltage is programmable by changing R2, R3, and R5 for CH1 and R21, R23, and R24 for CH2.

Default setting is 5 V for CH1 and 3.3 V for CH2.

$$V_{out}(CH1) = \frac{(R5 + R2 + R3)}{R3} \times V_{ref} (= 1\ V) \quad (1)$$

When V_{out}(CH1) is set above 5 V, V5SW input resistor (R22) must be open.

$$V_{out}(CH2) = \frac{(R21 + R23 + R24)}{R24} \times V_{ref} \ (= 1\ V) \quad (2)$$

6 Bill of Materials

Table 8. Bill of Materials

Reference	Qty	Description	Size	Mfr	Part Number
C1, C14, C26	3	Capacitor, Ceramic, 10 nF, 50V, X7R, 20%	0603	Std	Std
C2, C3	2	Capacitor, SPCAP, 150 µF, 6.3-V, 15-mΩ, 20%	7343	Panasonic	EEFCX0J151R
C4, C5, C6, C21, C22, C23	6	Capacitor, Ceramic, 0.1 µF, 50V, X7R, 20%	0603	TDK	C1608X7R1H104K
C7, C16, C20, C27	4	Capacitor, Ceramic, 100 pF, 50V, CH, 5%	0603	TDK	C1608CH1H101J
C8, C33	0	Capacitor, Ceramic, 10 µF, 25V, X7R, 20%	1210	–	–
C9, C18, C19, C32	4	Capacitor, Ceramic, 10 µF, 25V, X7R , 20%	1210	Murata	GRM32DR71E106KA
C10	1	Capacitor, Ceramic, 2.2 F, 6.3V, X7R (or X5R), 10%	0603	Murata TDK	GRM188R70J225KA C1608X5R0J225K
C11	0	Capacitor, Ceramic	0603	–	–
C12	1	Capacitor, Ceramic, 47pF, 50V, CH, 5%	0603	TDK	C1608CH1H470J
C13	1	Capacitor, Ceramic, 0.22 F, 50V, X7R, 10%	0630	TDK	C1608X7R1E224K
C15	1	Capacitor, Ceramic, 10 F, 10V, X7R (or X5R), 10%	0805	Murata TDK	GRM21BR71A106K C2012X5R0J106K
C17	0	Capacitor, Ceramic	0603	–	–
C24, C29	0	Capacitor	7343	–	–
C25, C30	2	Capacitor, SPCAP, 220 F, 4-V, 15-mΩ, 20%	7343	Panasonic	EEFCX0G221R
C28	0	Capacitor, Ceramic	0603	–	–
C31	0	Capacitor, Ceramic	0603	–	–
D1, D2	0	Diode	0.1 × 0.049 inch	–	–
L1	1	Inductor, 4.7µH, 10.2A, 12.9-mΩ	0.4 × 0.4 inch	TOKO	FDV1040-4R7M
L2	1	Inductor, 3.3µH, 10.7A, 10.5-mΩ	0.4 × 0.4 inch	TOKO	FDV1040-3R3M
Q1, Q3	2	MOSFET, N-ch, 30-V, 14-A, 9.7-mΩ	SO8	TI	CSD17307Q5A
Q2, Q4	2	MOSFET, N-ch, 30-V, 21-A, 4.5-mΩ	SO8	TI	CSD17310Q5A
R1, R4, R9, R17, R22, R34, R35,R36, R37	9	Resistor, Chip, 0Ω, 1/10W, 1%	0603	Std	Std
R2	1	Resistor, Chip, 120kΩ, 1/10W, 1%	0603	Std	Std
R3	1	Resistor, Chip, 30kΩ, 1/10W, 1%	0603	Std	Std
R5, R23	2	Resistor, Chip 49.9 or 51Ω, 1/10W, 1%	0603	Std	Std
R6	0	Resistor, Chip, mΩ, 1 W, 1%	3712	Std	Std
R7, R25	0	Resistor, Chip	0603	Std	Std
R8	1	Resistor, Chip, 7.5kΩ, 1/10W, 1%	0603	Std	Std
R10	0	Resistor, Chip	0603	Std	Std
R11, R14	2	Resistor, Chip, 470kΩ, 1/10W, 1%	0603	Std	Std
R12, R13	2	Resistor, Chip, 10kΩ, 1/10W, 1%	0603	Std	Std
R15	1	Resistor, Chip, 360kΩ, 1/10W, 1%	0603	Std	Std

Table 8. Bill of Materials (continued)

Reference	Qty	Description	Size	Mfr	Part Number
R16	0	Resistor, Chip	0603	Std	Std
R18, R28	2	Resistor, Chip, 5.6kΩ, 1/10W, 1%	0603	Std	Std
R19, R26	0	Resistor, Chip	0603	Std	Std
R20	0	Resistor, Chip, mΩ, 1 W, 1%	3712	Std	Std
R21	1	Resistor, Chip, 62kΩ, 1/10W, 1%	0603	Std	Std
R24	1	Resistor, Chip, 27kΩ, 1/10W, 1%	0603	Std	Std
R27	0	Resistor, Chip	0603	Std	Std
R32	0	Resistor, Chip	0603	Std	Std
R29	1	Resistor, Chip, 4.7kΩ, 1/10W, 1%	0603	Std	Std
R30, R33	2	Resistor, Chip, 15.4Ω, 1/10W, 1%	0603	Std	Std
R31	0	Resistor, Chip	0603	Std	Std
R38	1	Resistor, Chip, 0Ω, 1/10W, 1%	0603	Std	Std
R39	1	Resistor, Chip, 0Ω, 1/10W, 1%	0603	Std	Std
S1, S2, S3	3	Switch, ON-ON Mini Toggle	0.28 × 0.18"	Nikkai	G12AP
J1, J2	2	Terminal Block, 2-pin, 15A, 5,1mm	0.40 × 0.35inch	OST	ED1609
JP1, JP2, JP3, JP4	4	Header, 2×4-pin, 100mil spacing (36-pin strip)	0.20 × 0.40inch	Sullins	PTC36DAAN
—	4	Shunt, 100-mil, Black	0.100	Std	Std
TP1, TP2	2	Pin, Probe monitor (VOUT1)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
TP3, TP10, TP11	3	Pin, Probe monitor (EN, ENx)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
TP4, TP17	2	Pin, Probe monitor (SW-node)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
TP5	0	Pin, Probe monitor (IMON)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
TP6, TP18	2	Pin, Probe monitor (PGOOD)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
TP7, TP8, TP9	3	Pin, Probe monitor (LDO)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
TP12, TP13	2	Pin, Probe monitor (VOUT2)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
TP14, TP15	2	Pin, Probe monitor (VIN)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
TP16	0	Pin, Probe monitor (IMON)	0.12(D) × 0.4 inch	Keystone or MAC8	5002 LC-2-S
U1	1	IC, Dual Peak Current Mode, Sync. Step-down Controller	QFN32	TI	TPS51220RHB
VIN, GNDI	2	Pin, Wiring Terminal (VIN)	0.12(D) × 0.4 inch	Mill Max or MAC8	3183-2-00-15-00-00-080 or WT-3-1
VOUT1, GND1, GND3	3	Pin, Wiring Terminal (VOUT1)	0.12(D) × 0.4 inch	Mill Max or MAC8	3183-2-00-15-00-00-080 or WT-3-1
VOUT2, GND2, GND4	3	Pin, Wiring Terminal (VOUT2)	0.12(D) × 0.4 inch	Mill Max or MAC8	3183-2-00-15-00-00-080 or WT-3-1
SYNC, GNDS	2	Pin, Wiring Terminal (SYNC)	0.12(D) × 0.4 inch	Mill Max or MAC8	3183-2-00-15-00-00-080 or WT-3-1

7 EVM Assembly Drawing and PCB Layout

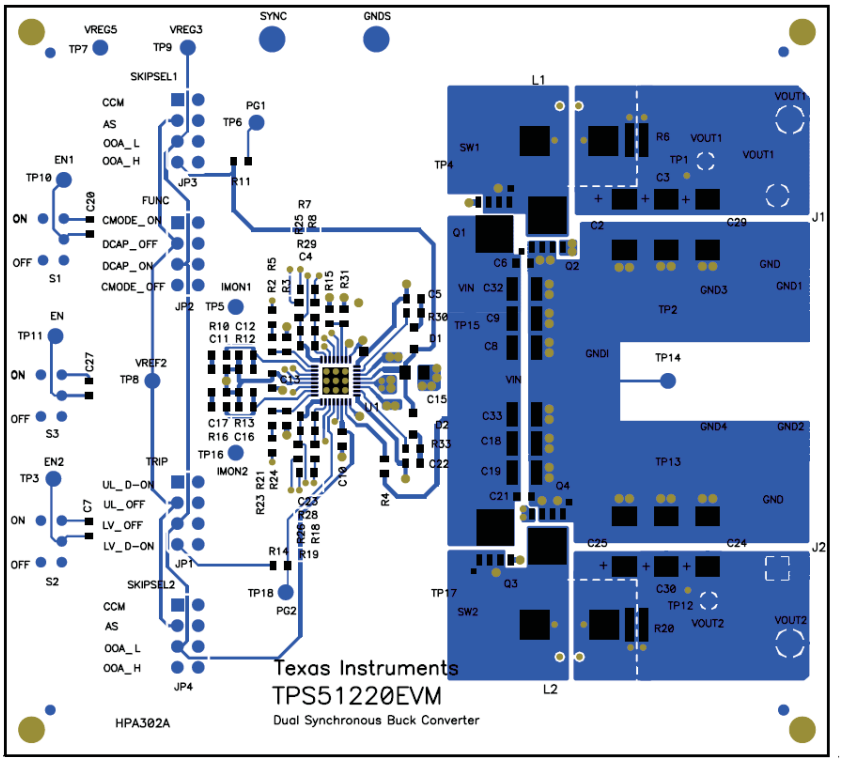

Figure 5. Top Layer/ Assembly

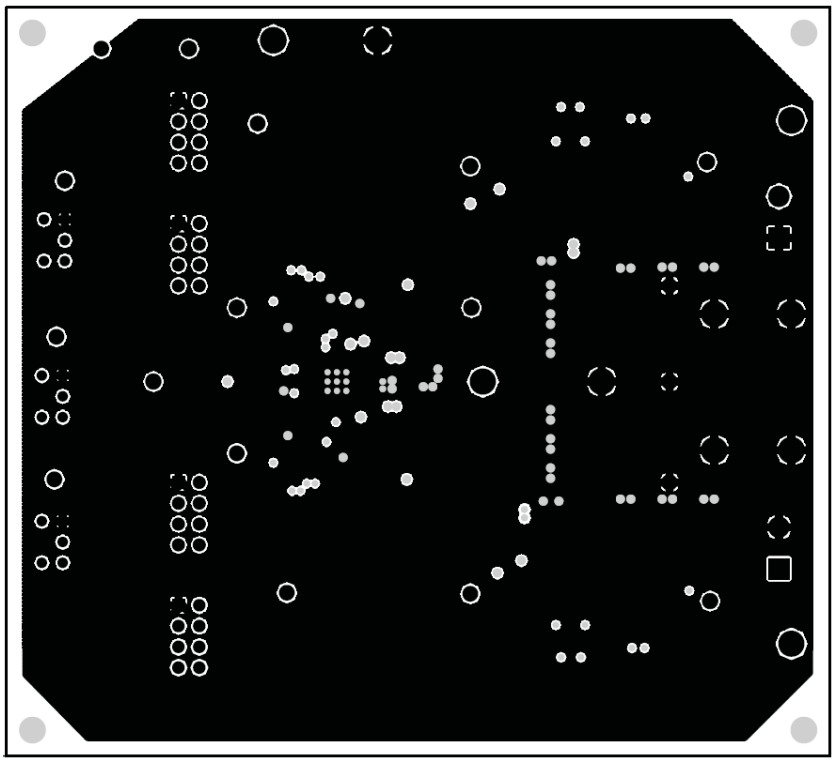

Figure 6. Inner Layer 1

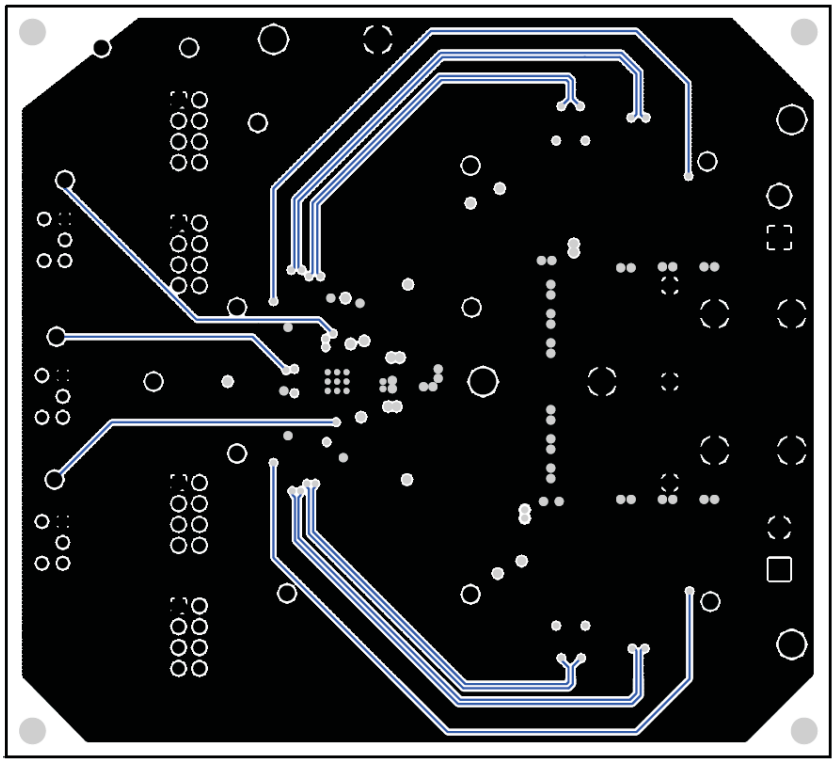

Figure 7. Inner Layer 2

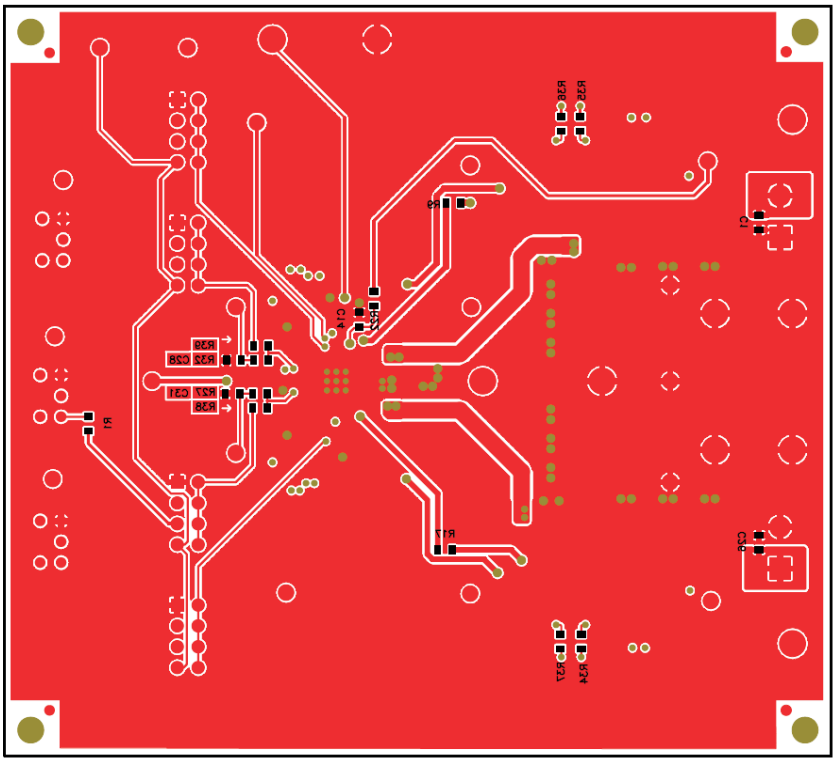

Figure 8. Bottom Layer/ Assembly

8 Reference

1. *TPS51220; Fixed Frequency, 99% Duty Cycle Peak Current Mode Notebook System Power Controller* data sheet (SLVS785)
2. *TPS51221, Fixed Frequency, 99% Duty Cycle Peak Current Mode Notebook System Power Controller* data sheet (SLVS786)

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It is important to operate this EVM within the input voltage range of 4.5 V to 25 V and the output voltage range of 1 V to 12 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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