

- Low  $r_{DS(on)}$  . . . 5  $\Omega$  Typical
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Low Power Consumption

## description

The TPIC6B273 is a monolithic, high-voltage, medium-current, power logic octal D-type latch with DMOS-transistor outputs designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

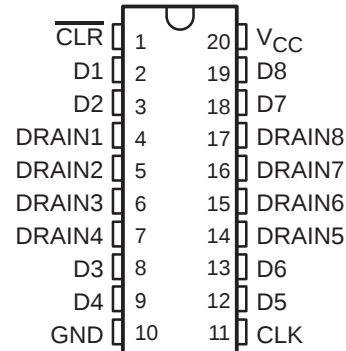
The TPIC6B273 contains eight positive-edge-triggered D-type flip-flops with a direct clear input. Each flip-flop features an open-drain power DMOS-transistor output.

When clear ( $\overline{CLR}$ ) is high, information at the D inputs meeting the setup time requirements is transferred to the DRAIN outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input (CLK) is at either the high or low level, the D input signal has no effect at the output. An asynchronous  $\overline{CLR}$  is provided to turn all eight DMOS-transistor outputs off. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

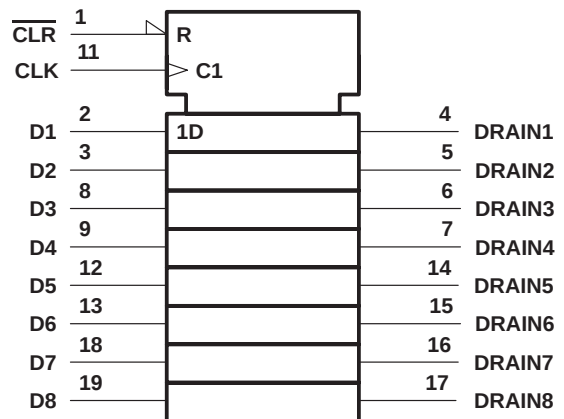
Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at  $T_C = 25^\circ\text{C}$ . The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B273 is characterized for operation over the operating case temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**DW OR N PACKAGE  
(TOP VIEW)**



## logic symbol†



† This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12.

**FUNCTION TABLE  
(each channel)**

| INPUTS           |            |   | OUTPUT<br>DRAIN |
|------------------|------------|---|-----------------|
| $\overline{CLR}$ | CLK        | D |                 |
| L                | X          | X | H               |
| H                | $\uparrow$ | H | L               |
| H                | $\uparrow$ | L | H               |
| H                | L          | X | Latched         |

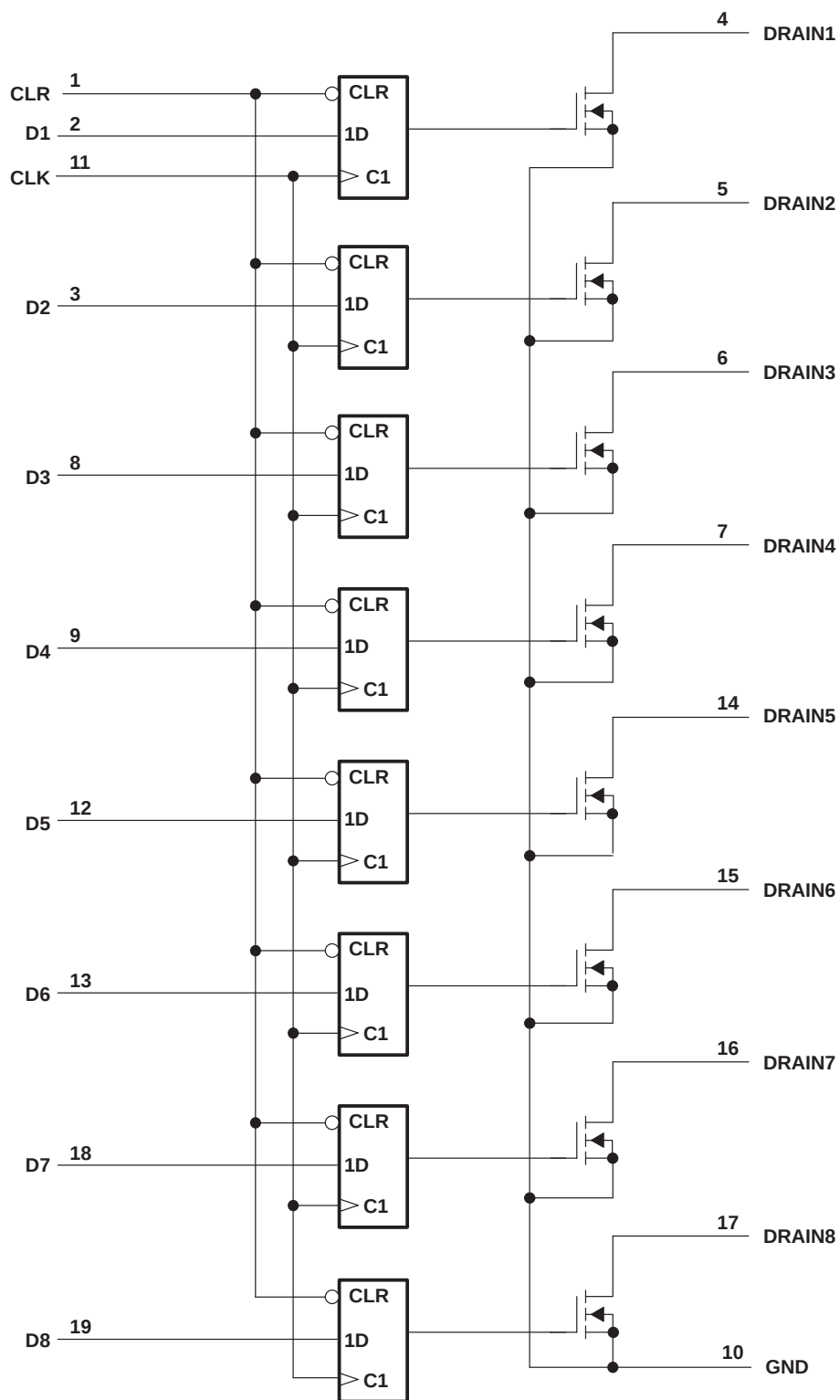
H = high level, L = low level, X = irrelevant

# TPIC6B273

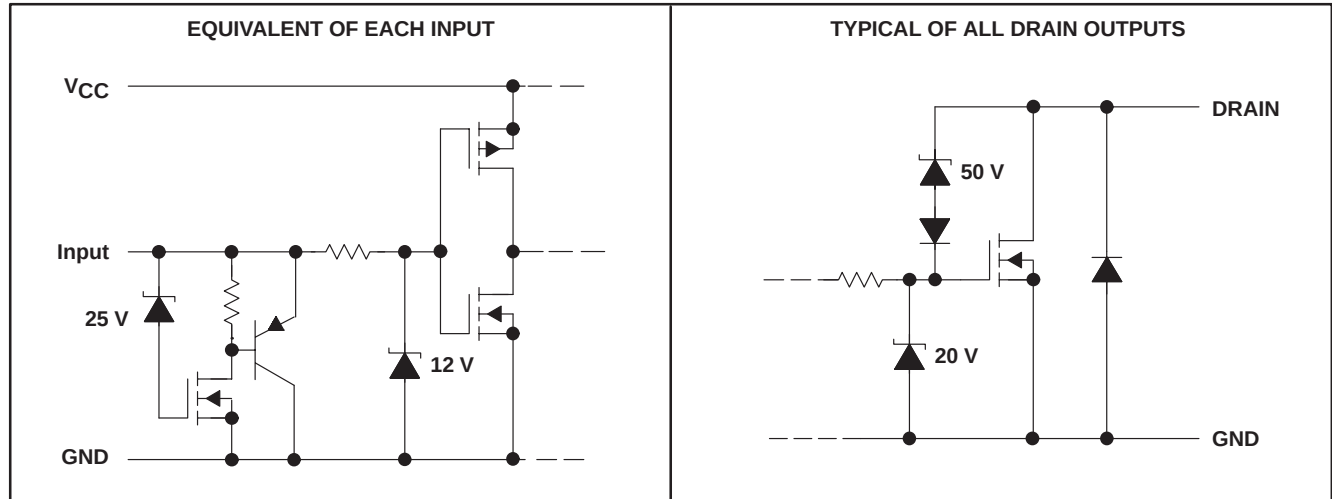
## POWER LOGIC OCTAL D-TYPE LATCH

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### logic diagram (positive logic)



## schematic of inputs and outputs



## absolute maximum ratings over recommended operating case temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                                  |                              |
|--------------------------------------------------------------------------------------------------|------------------------------|
| Logic supply voltage, $V_{CC}$ (see Note 1)                                                      | 7 V                          |
| Logic input voltage range, $V_I$                                                                 | –0.3 V to 7 V                |
| Power DMOS drain-to-source voltage, $V_{DS}$ (see Note 2)                                        | 50 V                         |
| Continuous source-to-drain diode anode current                                                   | 500 mA                       |
| Pulsed source-to-drain diode anode current (see Note 3)                                          | 1 A                          |
| Pulsed drain current, each output, all outputs on, $I_D$ , $T_C = 25^\circ\text{C}$ (see Note 3) | 500 mA                       |
| Continuous drain current, each output, all outputs on, $I_D$ , $T_C = 25^\circ\text{C}$          | 150 mA                       |
| Peak drain current single output, $I_{DM}$ , $T_C = 25^\circ\text{C}$ (see Note 3)               | 500 mA                       |
| Single-pulse avalanche energy, $E_{AS}$ (see Figure 4)                                           | 30 mJ                        |
| Avalanche current, $I_{AS}$ (see Note 4)                                                         | 500 mA                       |
| Continuous total dissipation                                                                     | See Dissipation Rating Table |
| Operating virtual junction temperature range, $T_J$                                              | –40°C to 150°C               |
| Operating case temperature range, $T_C$                                                          | –40°C to 125°C               |
| Storage temperature range                                                                        | –65°C to 150°C               |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds                                     | 260°C                        |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values are with respect to GND.
  2. Each power DMOS source is internally connected to GND.
  3. Pulse duration  $\leq 100 \mu\text{s}$  and duty cycle  $\leq 2\%$ .
  4. DRAIN supply voltage = 15 V, starting junction temperature ( $T_{JS}$ ) = 25°C,  $L = 200 \text{ mH}$ ,  $I_{AS} = 0.5 \text{ A}$  (see Figure 4).

**DISSIPATION RATING TABLE**

| PACKAGE | $T_C \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_C = 25^\circ\text{C}$ | $T_C = 125^\circ\text{C}$<br>POWER RATING |
|---------|---------------------------------------------|---------------------------------------------------|-------------------------------------------|
| DW      | 1389 mW                                     | 11.1 mW/°C                                        | 278 mW                                    |
| N       | 1050 mW                                     | 10.5 mW/°C                                        | 263 mW                                    |

# TPIC6B273

## POWER LOGIC OCTAL D-TYPE LATCH

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### recommended operating conditions

|                                                                                                   | MIN           | MAX           | UNIT             |
|---------------------------------------------------------------------------------------------------|---------------|---------------|------------------|
| Logic supply voltage, $V_{CC}$                                                                    | 4.5           | 5.5           | V                |
| High-level input voltage, $V_{IH}$                                                                | 0.85 $V_{CC}$ |               | V                |
| Low-level input voltage, $V_{IL}$                                                                 |               | 0.15 $V_{CC}$ | V                |
| Pulsed drain output current, $T_C = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$ (see Notes 3 and 5) | –500          | 500           | mA               |
| Setup time, D high before $\text{CLK}\uparrow$ , $t_{SU}$ (see Figure 2)                          | 20            |               | ns               |
| Hold time, D high after $\text{CLK}\uparrow$ , $t_H$ (see Figure 2)                               | 20            |               | ns               |
| Pulse duration, $t_W$ (see Figure 2)                                                              | 40            |               | ns               |
| Operating case temperature, $T_C$                                                                 | –40           | 125           | $^\circ\text{C}$ |

### electrical characteristics, $V_{CC} = 5\text{ V}$ , $T_C = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER                                               | TEST CONDITIONS                                                                              | MIN                                   | TYP  | MAX | UNIT          |
|---------------------------------------------------------|----------------------------------------------------------------------------------------------|---------------------------------------|------|-----|---------------|
| $V_{(BR)DSX}$ Drain-to-source breakdown voltage         | $I_D = 1\text{ mA}$                                                                          | 50                                    |      |     | V             |
| $V_{SD}$ Source-to-drain diode forward voltage          | $I_F = 100\text{ mA}$                                                                        |                                       | 0.85 | 1   | V             |
| $I_{IH}$ High-level input current                       | $V_{CC} = 5.5\text{ V}$ , $V_I = V_{CC}$                                                     |                                       |      | 1   | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current                        | $V_{CC} = 5.5\text{ V}$ , $V_I = 0$                                                          |                                       |      | –1  | $\mu\text{A}$ |
| $I_{CC}$ Logic supply current                           | $V_{CC} = 5.5\text{ V}$ All outputs off                                                      |                                       | 20   | 100 | $\mu\text{A}$ |
|                                                         | All outputs on                                                                               |                                       | 150  | 300 |               |
| $I_N$ Nominal current                                   | $V_{DS(on)} = 0.5\text{ V}$ , $I_N = I_D$ , $T_C = 85^\circ\text{C}$ , See Notes 5, 6, and 7 |                                       | 90   |     | mA            |
| $I_{DSX}$ Off-state drain current                       | $V_{DS} = 40\text{ V}$ , $V_{CC} = 5.5\text{ V}$                                             |                                       | 0.1  | 5   | $\mu\text{A}$ |
|                                                         | $V_{DS} = 40\text{ V}$ , $V_{CC} = 5.5\text{ V}$ , $T_C = 125^\circ\text{C}$                 |                                       | 0.15 | 8   |               |
| $r_{DS(on)}$ Static drain-to-source on-state resistance | $I_D = 100\text{ mA}$ , $V_{CC} = 4.5\text{ V}$                                              | See Notes 5 and 6 and Figures 6 and 7 | 4.2  | 5.7 | $\Omega$      |
|                                                         | $I_D = 100\text{ mA}$ , $V_{CC} = 4.5\text{ V}$ , $T_C = 125^\circ\text{C}$                  |                                       | 6.8  | 9.5 |               |
|                                                         | $I_D = 350\text{ mA}$ , $V_{CC} = 4.5\text{ V}$                                              |                                       | 5.5  | 8   |               |

### switching characteristics, $V_{CC} = 5\text{ V}$ , $T_C = 25^\circ\text{C}$

| PARAMETER                                                           | TEST CONDITIONS                                                                            | MIN | TYP | MAX | UNIT |
|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low-to-high-level output from CLK | $C_L = 30\text{ pF}$ , $I_D = 100\text{ mA}$ , See Figures 1, 2, and 8                     |     | 150 |     | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low-level output from CLK |                                                                                            |     | 90  |     | ns   |
| $t_r$ Rise time, drain output                                       |                                                                                            |     | 200 |     | ns   |
| $t_f$ Fall time, drain output                                       |                                                                                            |     | 200 |     | ns   |
| $t_a$ Reverse-recovery-current rise time                            | $I_F = 100\text{ mA}$ , $di/dt = 20\text{ A}/\mu\text{s}$ , See Notes 5 and 6 and Figure 3 |     | 100 |     | ns   |
| $t_{rr}$ Reverse-recovery time                                      |                                                                                            |     | 300 |     |      |

- NOTES: 3. Pulse duration  $\leq 100\text{ }\mu\text{s}$  and duty cycle  $\leq 2\%$ .  
5. Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.  
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.  
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of  $0.5\text{ V}$  at  $T_C = 85^\circ\text{C}$ .

## thermal resistance

| PARAMETER       |                                         | TEST CONDITIONS | MIN | MAX | UNIT                        |
|-----------------|-----------------------------------------|-----------------|-----|-----|-----------------------------|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient | DW package      |     | 90  | $^{\circ}\text{C}/\text{W}$ |
|                 |                                         | N package       |     | 95  |                             |

## PARAMETER MEASUREMENT INFORMATION

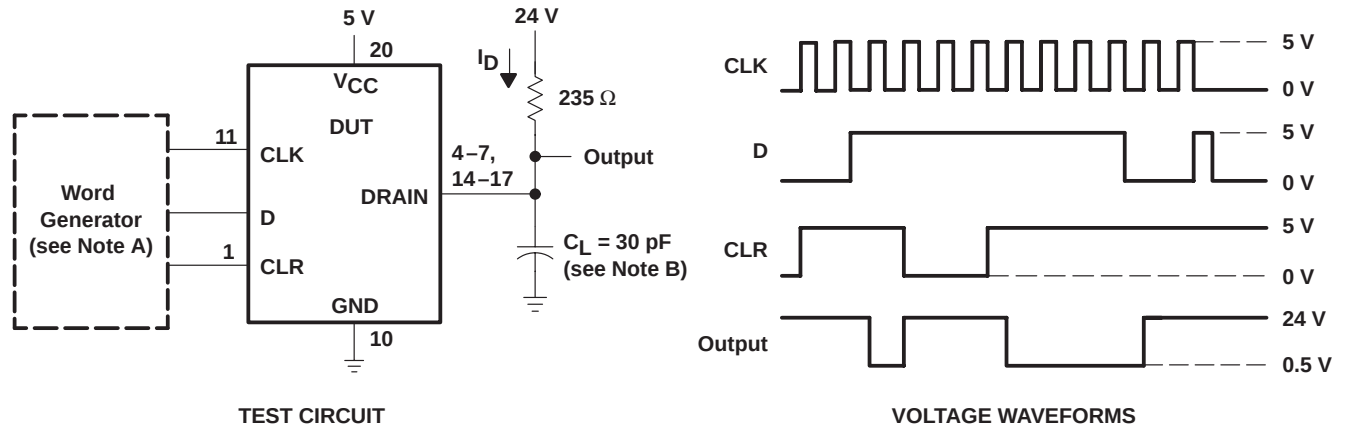


Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

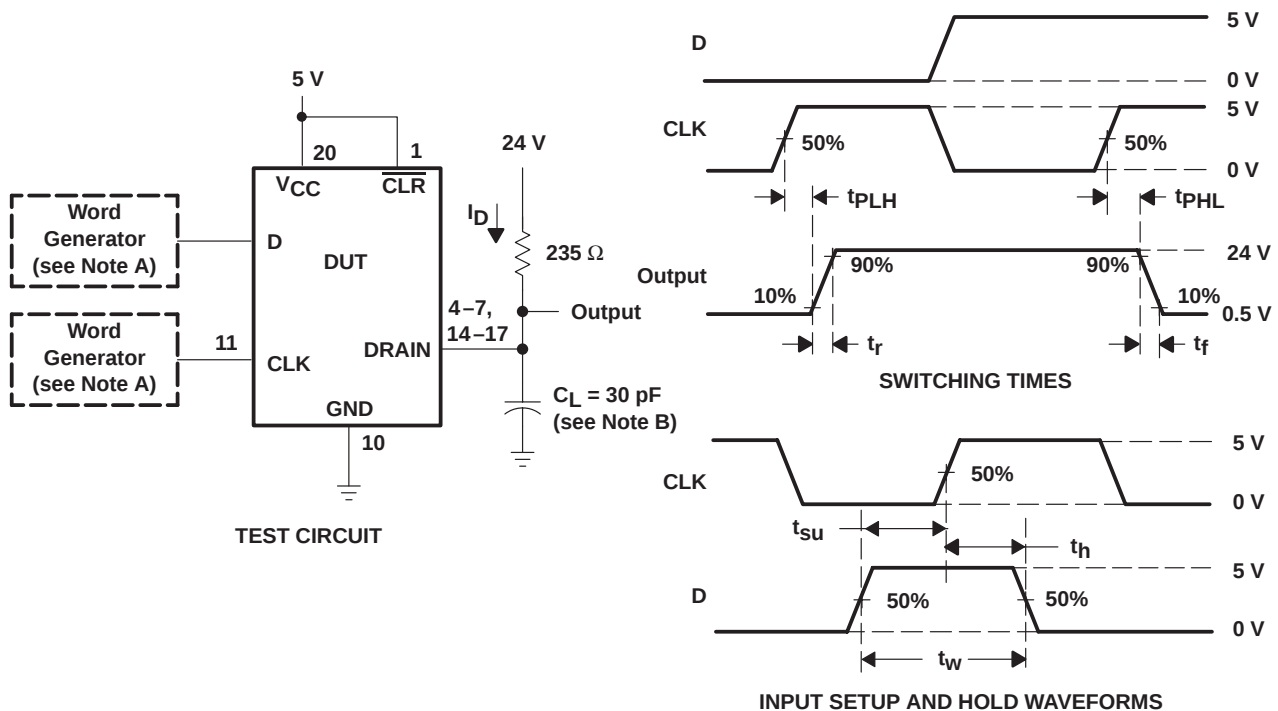


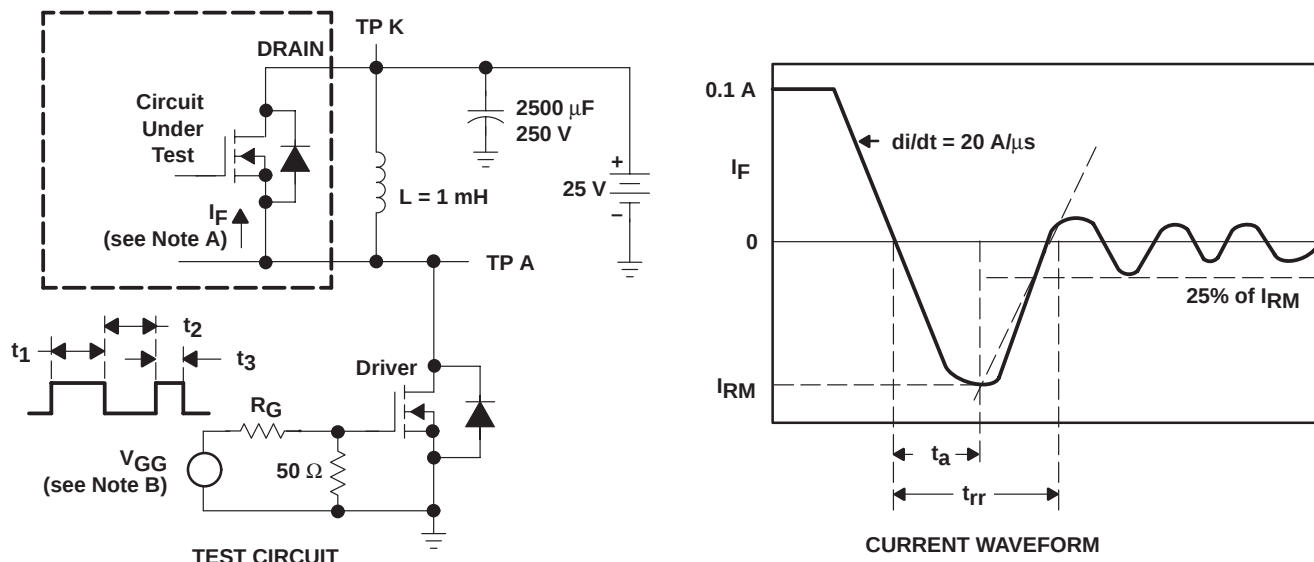
Figure 2. Test Circuit, Switching Times, and Voltage Waveforms

- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $t_w = 300 \text{ ns}$ , pulsed repetition rate (PRR) = 5 KHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

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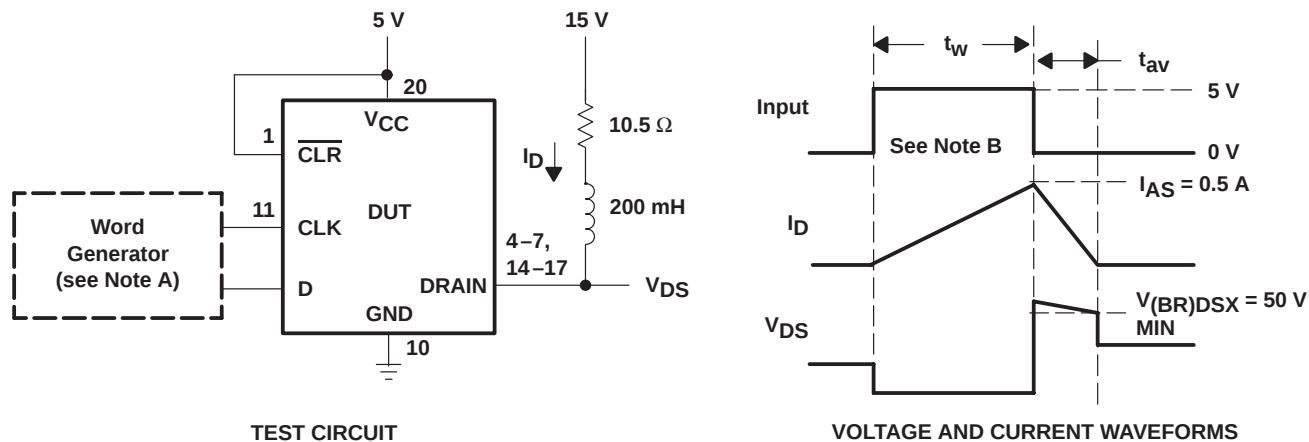
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## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
- B. The  $V_{GG}$  amplitude and  $R_G$  are adjusted for  $di/dt = 20 \text{ A}/\mu\text{s}$ . A  $V_{GG}$  double-pulse train is used to set  $I_F = 0.1 \text{ A}$ , where  $t_1 = 10 \mu\text{s}$ ,  $t_2 = 7 \mu\text{s}$ , and  $t_3 = 3 \mu\text{s}$ .

**Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode**



- NOTES: A. The word generator has the following characteristics:  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ ,  $Z_O = 50 \Omega$ .
- B. Input pulse duration,  $t_w$ , is increased until peak current  $I_{AS} = 0.5 \text{ A}$ .  
Energy test is defined as  $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30 \text{ mJ}$ .

**Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms**

# TYPICAL CHARACTERISTICS

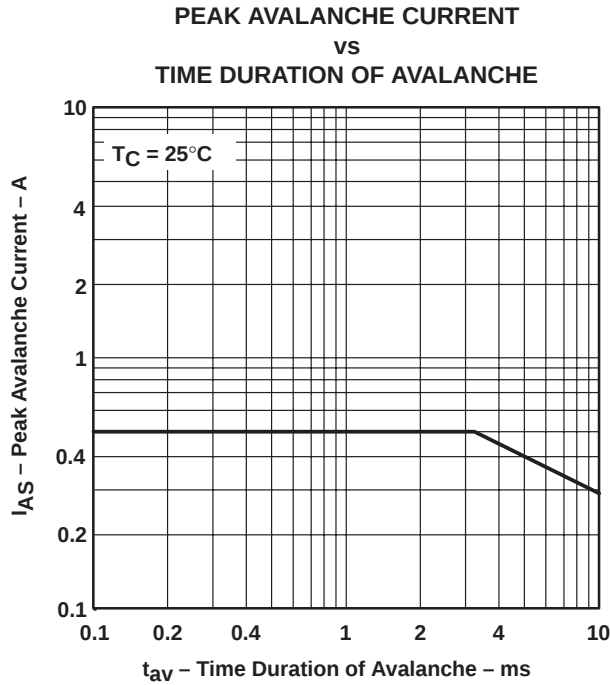


Figure 5

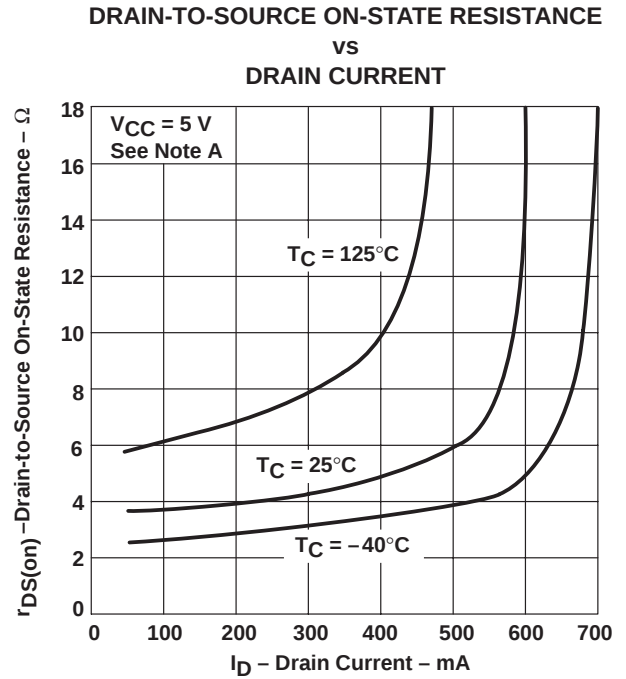


Figure 6

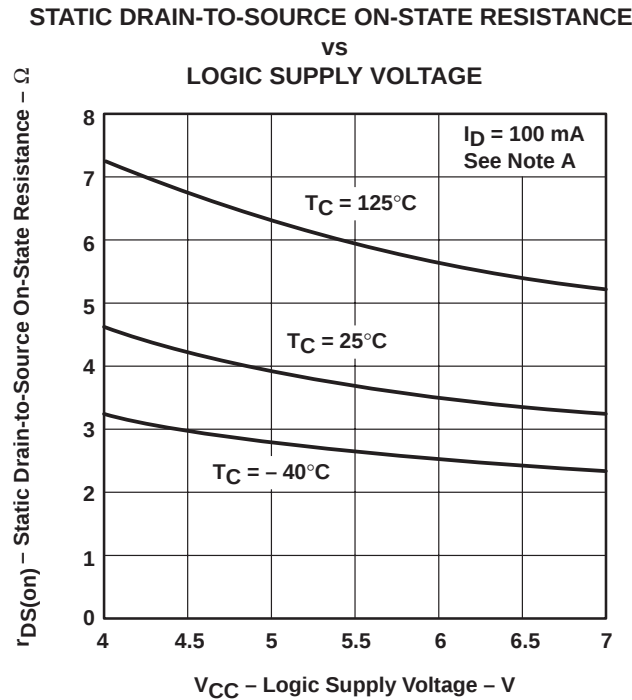


Figure 7

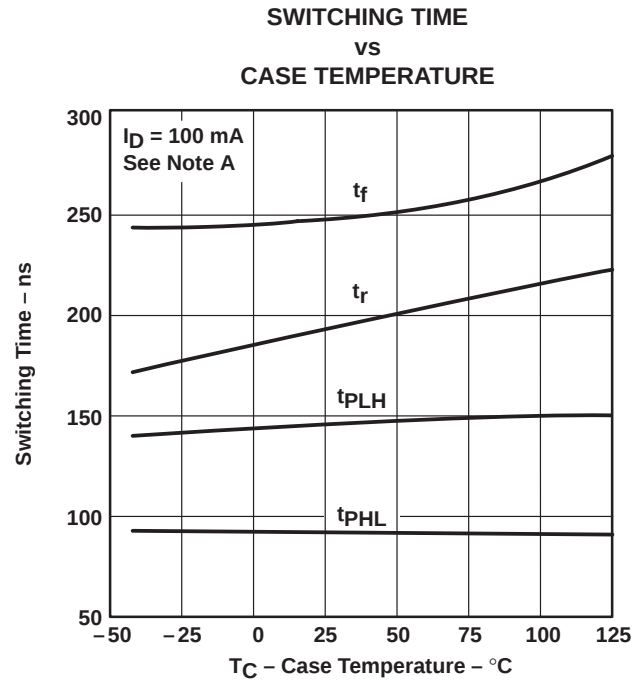


Figure 8

NOTE C: Technique should limit  $T_J - T_C$  to  $10^\circ\text{C}$  maximum.

TPIC6B273  
POWER LOGIC OCTAL D-TYPE LATCH

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THERMAL INFORMATION

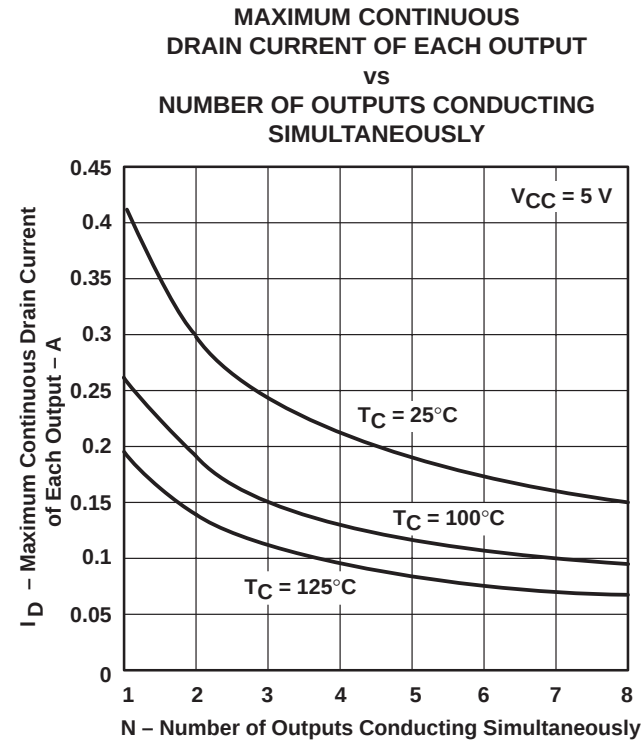


Figure 9

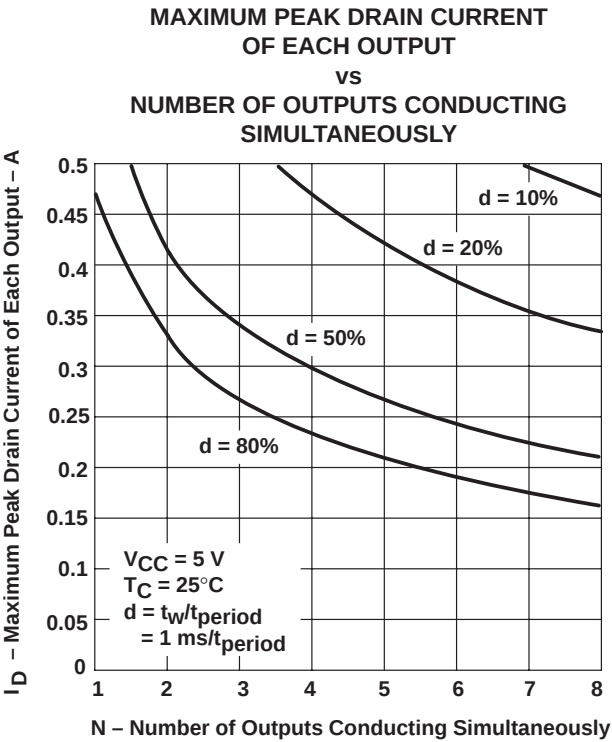


Figure 10

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/ Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|-------------------|------------------------------|--------------------------|
| TPIC6B273DW      | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| TPIC6B273DWG4    | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| TPIC6B273DWR     | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| TPIC6B273DWRG4   | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| TPIC6B273N       | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU         | N / A for Pkg Type           |                          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPIC6B273DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.1    | 2.65    | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPIC6B273DWR | SOIC         | DW              | 20   | 2000 | 346.0       | 346.0      | 41.0        |

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



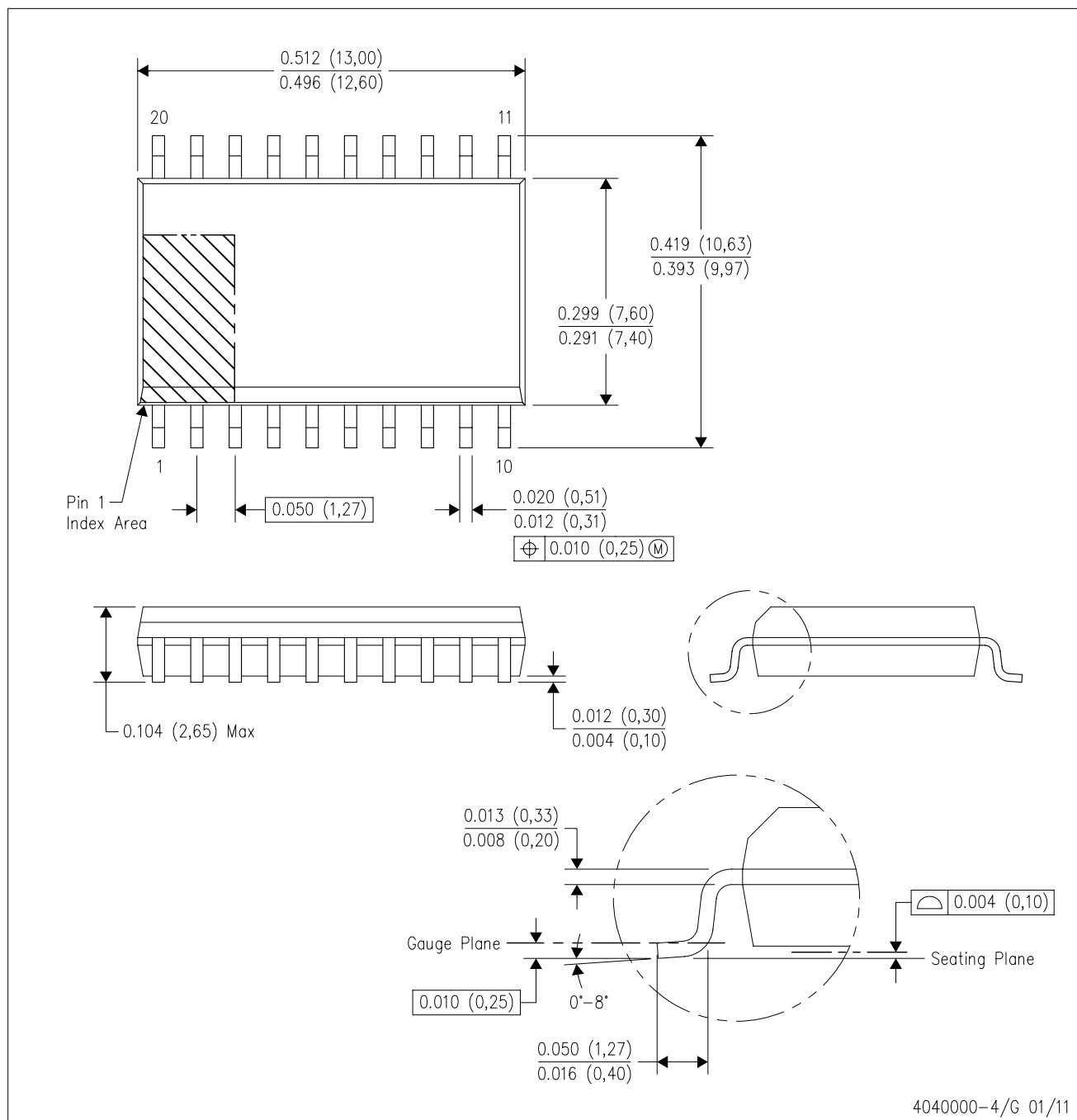
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

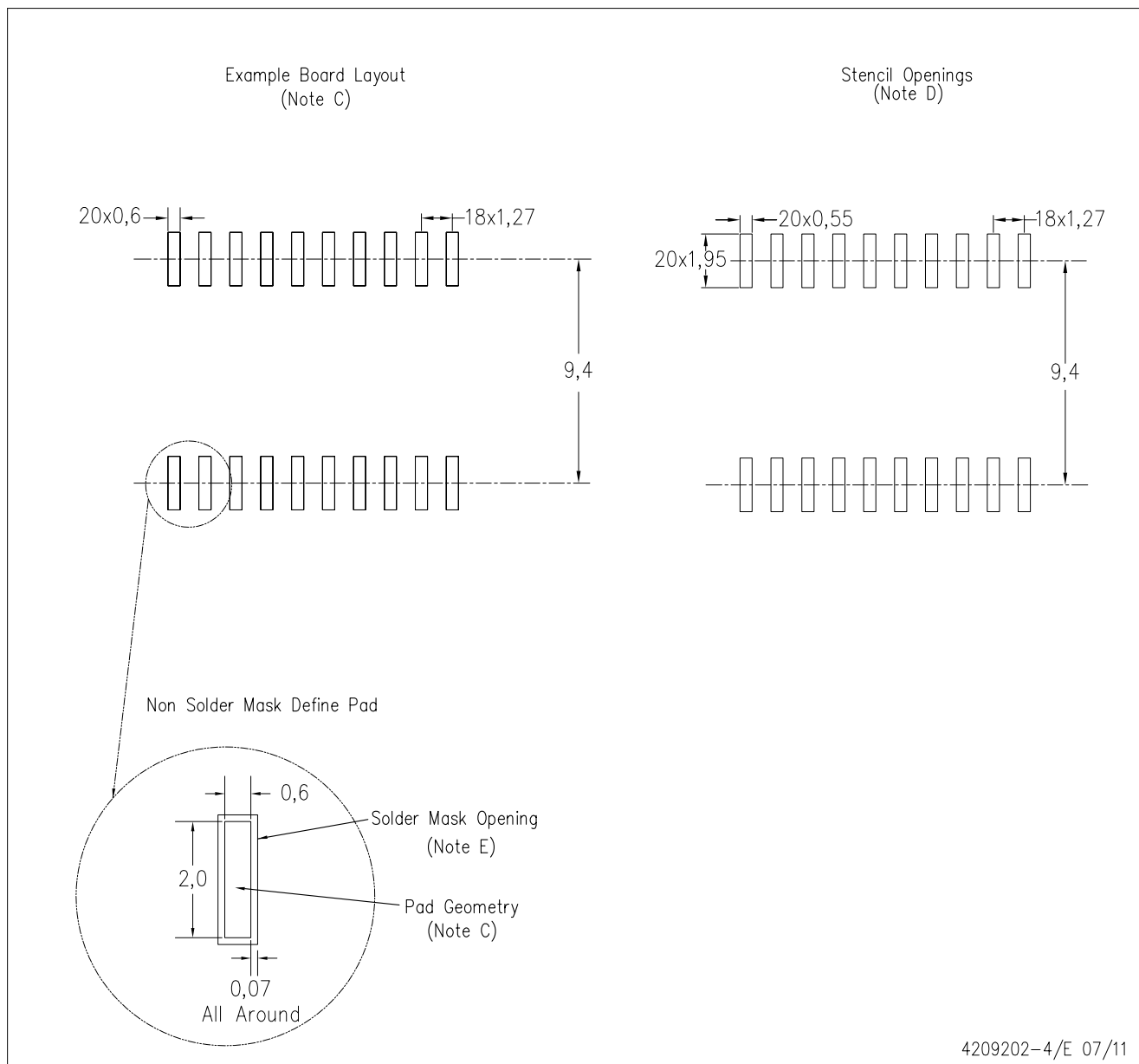
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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| DLP® Products          | <a href="http://www.dlp.com">www.dlp.com</a>                                         |
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| Clocks and Timers      | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface              | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                  | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt             | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers       | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                   | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Mobile Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity  | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

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