2.5 Gbps 3-TO-1 DVI/HDMI SWITCH

FEATURES

- **Compatible with HDMI 1.3a**
- **Supports 2.5 Gbps Signaling Rate for 480i/p, 720i/p, and 1080i/p Resolutions up to 12-Bit Color Depth**
- **Integrated Receiver Termination**
- **Selectable Receiver Equalization to Accommodate to Different Input Cable Lengths**
- **Intra-Pair Skew < 40 ps**
- **Inter-Pair Skew < 65 ps**
- **HBM ESD Protection Exceeds 8 kV to TMDS Inputs**
- **3.3-V Fixed Supply to TMDS I/Os**
- **5-V Fixed Supply to HPD, DDC, and Source Selection Circuits**
- **64-Pin TQFP Package**
- **ROHS Compatible and 260°C Reflow Rated**

APPLICATIONS

- **Digital TV**
- **Digital Projector**

DESCRIPTION

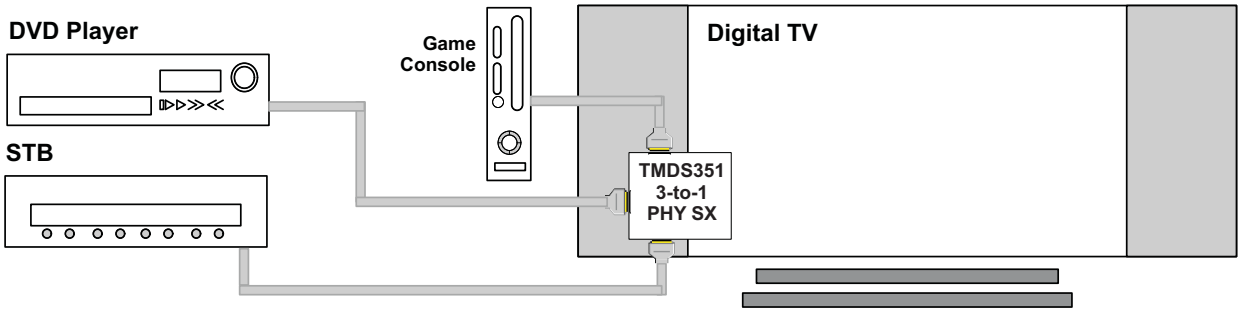
The TMDS351 is a 3-port digital video interface (DVI) or high-definition multimedia interface (HDMI) switch that allows up to 3 DVI or HDMI ports to be switched to a single display terminal. Four TMDS channels, one hot plug detector, and a digital display control (DDC) interface are supported on each port. Each TMDS channel supports signaling rates up to 2.5 Gbps to allow 1080p resolution in 12-bit color depth.

When S1 is high and S2 is low, all input terminations are disconnected, TMDS inputs are high impedance with standard TMDS terminations, all internal MOSFETs are turned off to disable the DDC links, and all HPD outputs are connected to the HPD_SINK. This allows the initiation of the HDMI physical address discovery process.

Termination resistors (50-Ω), pulled up to V_{CC}, are integrated at each TMDS receiver input. External terminations are not required. A precision resistor is connected externally from the VSADJ pin to ground for setting the differential output voltage to be compliant with the TMDS standard.

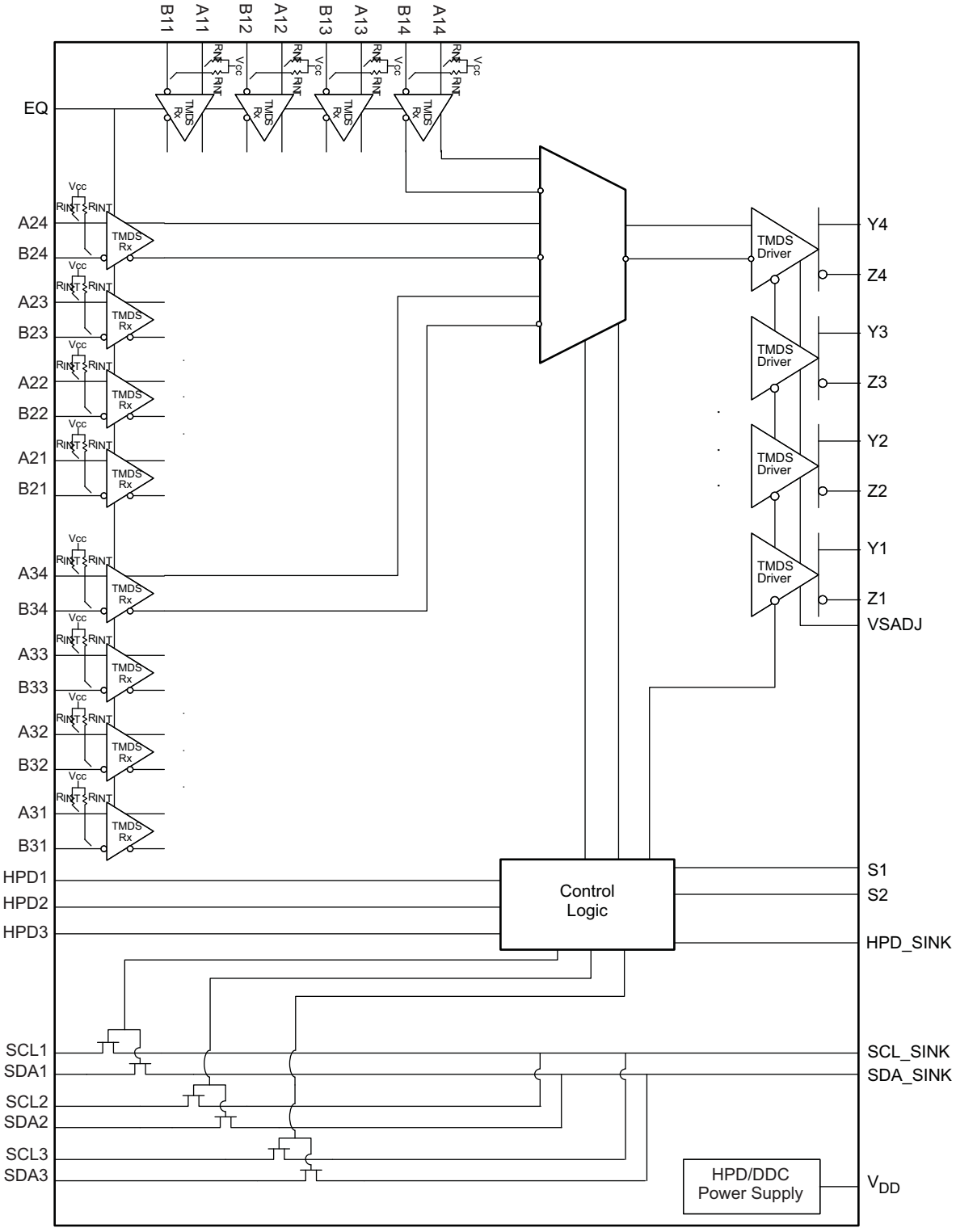
The TMDS351 provides two levels of receiver input equalization for different ranges of cable lengths. Each TMDS receiver owns frequency responsive equalization circuits. When EQ sets low, the receiver supports the input connection in short range HDMI cables. When EQ sets high, the receiver supports the input connection in long range HDMI cables. The TMDS351 supports power saving operation. When a system is under standby mode and there is no digital audio/visual content from a connected source, the 3.3-V supply voltage, V_{CC}, can be powered off to minimize power consumption from the TMDS inputs, outputs, and internal switching circuits. The HPD, DDC, and source selection circuits are powered up by the 5-V supply voltage, V_{DD}, to maintain the system hot plug detect response, the DDC link from the selected source to the sink under system standby operation. The device is characterized for operation from 0°C to 70°C.

Typical Application

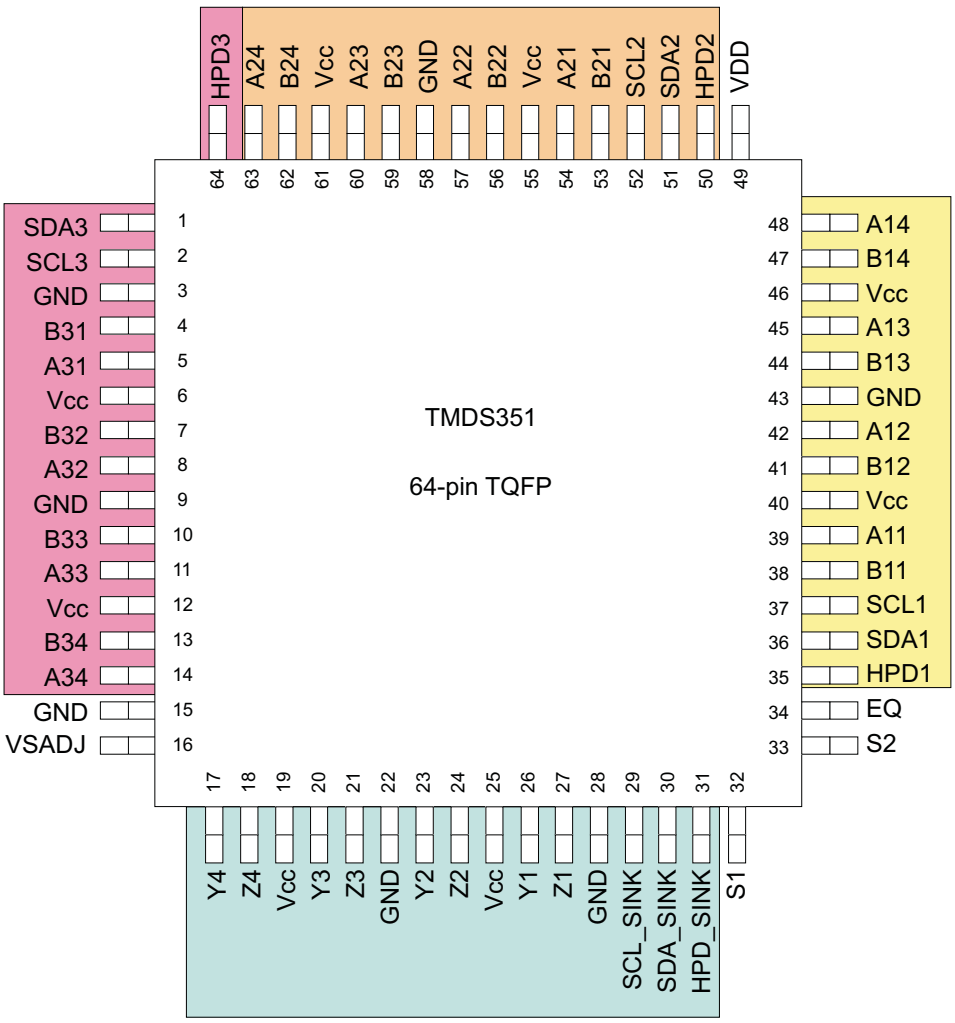


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



PAG PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
A11, A12, A13, A14	39, 42, 45, 48	I	Source port 1 TMDS positive inputs
A21, A22, A23, A24	54, 57, 60, 63	I	Source port 2 TMDS positive inputs
A31, A32, A33, A34	5, 8, 11, 14	I	Source port 3 TMDS positive inputs
B11, B12, B13, B14	38, 41, 44, 47	I	Source port 1 TMDS negative inputs
B21, B22, B23, B24	53, 56, 59, 62	I	Source port 2 TMDS negative inputs
B31, B32, B33, B34	4, 7, 10, 13	I	Source port 3 TMDS negative inputs
GND	3, 9, 15, 22, 28, 43, 58		Ground
EQ	34	I	TMDS Input equalization selector (control pin) EQ = Low – HDMI 1.3 compliant cable EQ = High – 10m 28 AWG HDMI cable
HPD1	35	O	Source port 1 hot plug detector output (status pin)
HPD2	50	O	Source port 2 hot plug detector output (status pin)
HPD3	64	O	Source port 3 hot plug detector output (status pin)
HPD_SINK	31	I	Sink port hot plug detector input (status pin)
SCL1	37	I/O	Source port 1 DDC I^2C clock line
SCL2	52	I/O	Source port 2 DDC I^2C clock line
SCL3	2	I/O	Source port 3 DDC I^2C clock line
SCL_SINK	29	I/O	Sink port DDC I^2C clock line
SDA1	36	I/O	Source port 1 DDC I^2C data line
SDA2	51	I/O	Source port 2 DDC I^2C data line
SDA3	1	I/O	Source port 3 DDC I^2C data line
SDA_SINK	30	I/O	Sink port DDC I^2C data line
S1, S2	32. 33	I	Source selector
V_{CC}	6, 12, 19, 25, 40, 46, 55, 61		Power supply
V_{DD}	49		HPD/DDC Power supply
VSADJ	16	I	TMDS compliant voltage swing control (control pin)
Y1, Y2, Y3, Y4	26,23,20,17	O	Sink port TMDS positive outputs
Z1, Z2, Z3, Z4	27,24,21,18	O	Sink port TMDS negative outputs

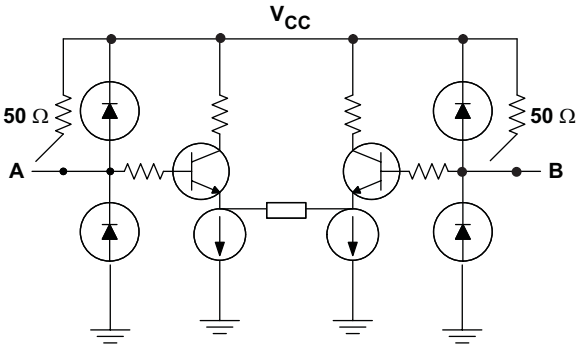
Table 1. Source Selection Lookup(1)

CONTROL PINS		I/O SELECTED		HOT PLUG DETECT STATUS		
S2	**S1**	**Y/Z**	**SCL_SINK SDA_SINK**	**HPD1**	**HPD2**	**HPD3**
H	H	A1/B1 Terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	HPD_SINK	L	L
H	L	A2/B2 Terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	HPD_SINK	L
L	L	A3/B3 Terminations of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	HPD_SINK
L	H	None (Z) All terminations are disconnected	None (Z) Are pulled HIGH by external pull-up termination	HPD_SINK	HPD_SINK	HPD_SINK

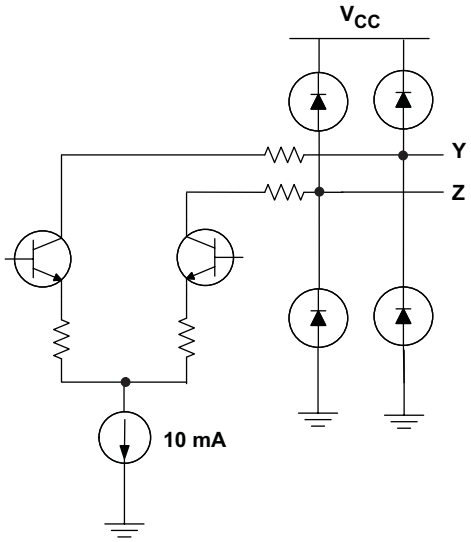
(1) H: Logic high; L: Logic low; X: Don't care; Z: High impedance

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

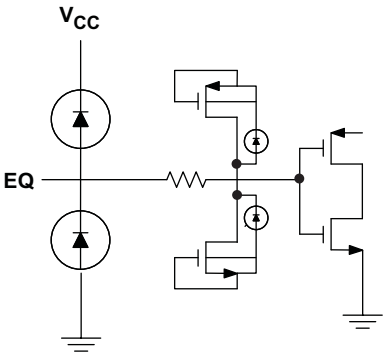
TMDS Input Stage



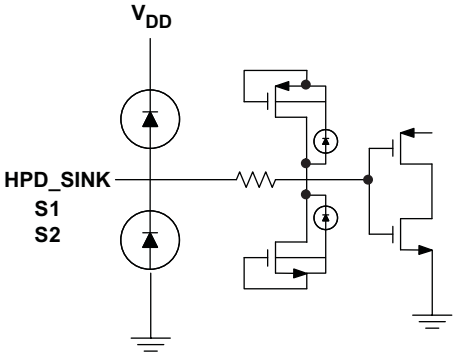
TMDS Output Stage



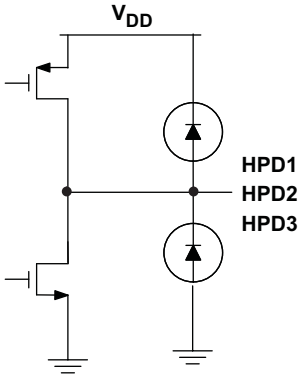
Control Input Stage



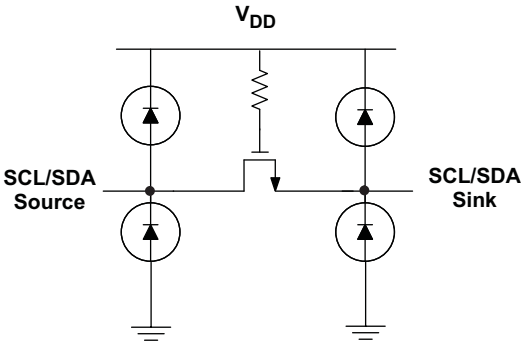
Status and Source Selector



HPD output stage



DDC pass gate



ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
TMDS351PAG	TMDS351	64-PIN TQFP
TMDS351PAGR	TMDS351	64-PIN TQFP Tape/Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
Supply voltage range(2)	V_{CC}		–0.5 V to 4 V
	V_{DD}		–0.5 V to 6 V
Voltage range	Anm(3), Bnm		2.5 V to 4 V
	Ym, Zm, VSADJ, EQ		–0.5V to 4 V
	SCLn, SCL_SINK, SDAn, SDA_SINK, HPDn, HPD_SINK, S1, S2		–0.5 V to 6 V
Electrostatic discharge	Human body model(4)	Anm, Bnm	±8000 V
		All pins	±4000 V
	Charged-device model(5) (all pins)		±1500 V
	Machine model (6) (all pins)		±200 V
Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) n = 1, 2, 3; m = 1, 2, 3, 4
(4) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(5) Tested in accordance with JEDEC Standard 22, Test Method C101-A
(6) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25°C$	DERATING FACTOR (1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
64-TQFP PAG	Low-K	1111 mW	11.19 mW/°C	611 mW
	High-K	1492 mW	14.92	820 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance			33.4		°C/W
$R_{\theta JC}$	Junction- to-case thermal resistance			15.6		°C/W
P_D	Device power dissipation	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC}$ - 0.6 V, R_T = 50 Ω, AV_{CC} = 3.3V, Am/Bm(2:4) = 2.5-Gbps HDMI data pattern, Am/Bm(1) = 250-MHz clock		590	750	mW

(1) The maximum rating is simulation under 3.6-V V_{CC}, 5.5-V V_{DD}, and 600 mV V_{ID}.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{DD}	Standby supply voltage	4.5	5	5.5	V
T_A	Operating free-air temperature	0		70	°C
TMDS DIFFERENTIAL PINS					
V_{IC}	Input common mode voltage	V_{CC}–0.4		V_{CC}+0.01	V
V_{ID}	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
R_{VSADJ}	Resistor for TMDS compliant voltage swing range	3.66	4.02	4.47	kΩ
AV_{CC}	TMDS output termination voltage, see Figure 1	3	3.3	3.6	V
R_T	Termination resistance, see Figure 1	45	50	55	Ω
	Signaling rate	0		2.5	Gbps
CONTROL PINS					
V_{IH}	LVTTL High-level input voltage	2		V_{CC}	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	V
DDC I/O PINS					
$V_{I(DDC)}$	DDC Input voltage	GND		V_{DD}	V
STATUS and SOURCE SELECTOR PINS					
V_{IH}	LVTTL High-level input voltage	2		V_{DD}	V
V_{IL}	LVTTL Low-level input voltage	GND		0.8	V

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC} – 0.6$ V, $R_T = 50$ Ω, $AV_{CC} = 3.3$ V Am/Bm(2:4) = 2.5 Gbps HDMI data pattern Am/Bm(1) = 250 MHz clock	S1/S2 = Low/Low, Low/High, High/High		176	200	mA
			S1/S2 = High/Low		8	20	
I_{DD}	Power supply current, 5-V	$V_{IH} = V_{CC}$, $V_{IL} = V_{CC} – 0.6$ V, $R_T = 50$ Ω, $AV_{CC} = 3.3$ V Am/Bm(2:4) = 2.5 Gbps HDMI data pattern Am/Bm(1) = 250 MHz clock			2	5	mA
TMDS DIFFERENTIAL PINS							
V_{OH}	Single-ended high-level output voltage	See Figure 2, $AV_{CC} = 3.3$ V, $R_T = 50$ Ω		AV_{CC}–10		AV_{CC}+10	mV
V_{OL}	Single-ended low-level output voltage			AV_{CC}–600		AV_{CC}–400	mV
V_{swing}	Single-ended output swing voltage			400		600	mV
$V_{OD(O)}$	Overshoot of output differential voltage					15%	2× V_{swing}
$V_{OD(U)}$	Undershoot of output differential voltage					25%	2× V_{swing}
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states					5	mV
$I_{(OS)}$	Short circuit output current	See Figure 3		-12		12	mA
$V_{I(open)}$	Single-ended input voltage under high impedance input or open input	$I_I = 10$ µA		V_{CC}–10		V_{CC}+10	mV
R_{INT}	Input termination resistance	$V_{IN} = 2.9$ V		45	50	55	Ω
CONTROL PINS							
I_{IH}	High-level digital input current(2)	$V_{IH} = 2$ V or V_{CC}		-10		10	µA
I_{IL}	Low-level digital input current(2)	$V_{IL} =$ GND or 0.8 V		-10		10	µA
DDC I/O PINS							
I_{lkg}	Input leakage current	$V_I = 0.1$ V_{DD} to 0.9 V_{DD} to isolated DDC inputs		-10		10	µA
C_{IO}	Input/output capacitance	$V_{I(pp)} = 1$ V, 100 kHz				10	pF

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) I_{IH} and I_{IL} specifications are not applicable to the VSADJ pin.

R_{ON}	Switch resistance	I_O = 3 mA, V_O = 0.4 V		27	40	Ω
V_{PASS}	Switch output voltage	V_I = 5 V, I_O = 100 µA	1.9		3.6	V
STATUS AND SOURCE SELECTOR PINS						
I_{IH}	High-level digital input current	V_{IH} = 2 V or V_{DD}	-10		10	µA
I_{IL}	Low-level digital input current	V_{IL} = GND or 0.8 V	-10		10	µA
V_{OH}	TTL High-level output voltage	I_{OH} = –100 µA	2.4		V_{DD}	V
V_{OL}	TTL Low-level output voltage	I_{OL} = 100 µA	GND		0.4	V

SWITCHING CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
TMDS DIFFERENTIAL PINS (Y/Z)						
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, AV_{CC} = 3.3 V, R_T = 50 Ω, PRE = 0 V	400	650	900	ps
t_{PHL}	Propagation delay time, high-to-low-level output		400	650	900	ps
t_r	Differential output signal rise time (20% - 80%)		60	80	140	ps
t_f	Differential output signal fall time (20% - 80%)		60	80	140	ps
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)(3)			6	20	ps
$t_{sk(D)}$	Intra-pair differential skew, see Figure 4			20	40	ps
$t_{sk(o)}$	Inter-pair channel-to-channel output skew(4)			30	65	ps
$t_{sk(pp)}$	Part-to-part skew (5)				510	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from Yj/Zj(1) residual jitter	See Figure 5, Am/Bm(1) = 250 MHz clock, Am/Bm(2:4) = 2.5 Gbps HDMI pattern		8	20	ps
$t_{jit(pp)}$	Peak-to-peak output jitter from Yj/Zj(2:4) residual jitter			60	80	ps
t_{SX}	Select to switch output	See Figure 6, 10-mA Current source to the input		50	70	ns
t_{en}	Enable time			170	250	ns
t_{dis}	Disable time			9	15	ns
$t_{pd(DDC)}$	Propagation delay from SCLn to SCL_SINK or SDAn to SDA_SINK or SDA_SINK to SDAn	See Figure 7, C_L = 10 pF		8	15	ns
$t_{sx(DDC)}$	Switch time from SCLn to SCL_SINK			8	15	ns
$t_{pd(HPD)}$	Propagation delay (from HPD_SINK to the active port of HPD)			14	20	ns
$t_{sx(HPD)}$	Switch time from port select to the latest valid status of HPD			33	50	ns

(1) Measurements are made with the Agilent 81250 ParBert System with a N4872A generator (600 fs $t_{JIT(CLK)}$, 13 ps $t_{JIT(pp)}$) and a N4873A analyzer.
(2) All typical values are at 25°C and with a 3.3-V supply.
(3) $t_{sk(p)}$ is the magnitude of the time difference between t_{PLH} and t_{PHL} of a specified terminal.
(4) $t_{sk(o)}$ is the magnitude of the difference in propagation delay times between any specified terminals of a sink-port bank when inputs of the active source port are tied together.
(5) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same source, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

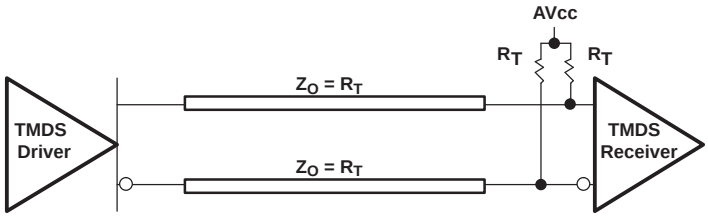
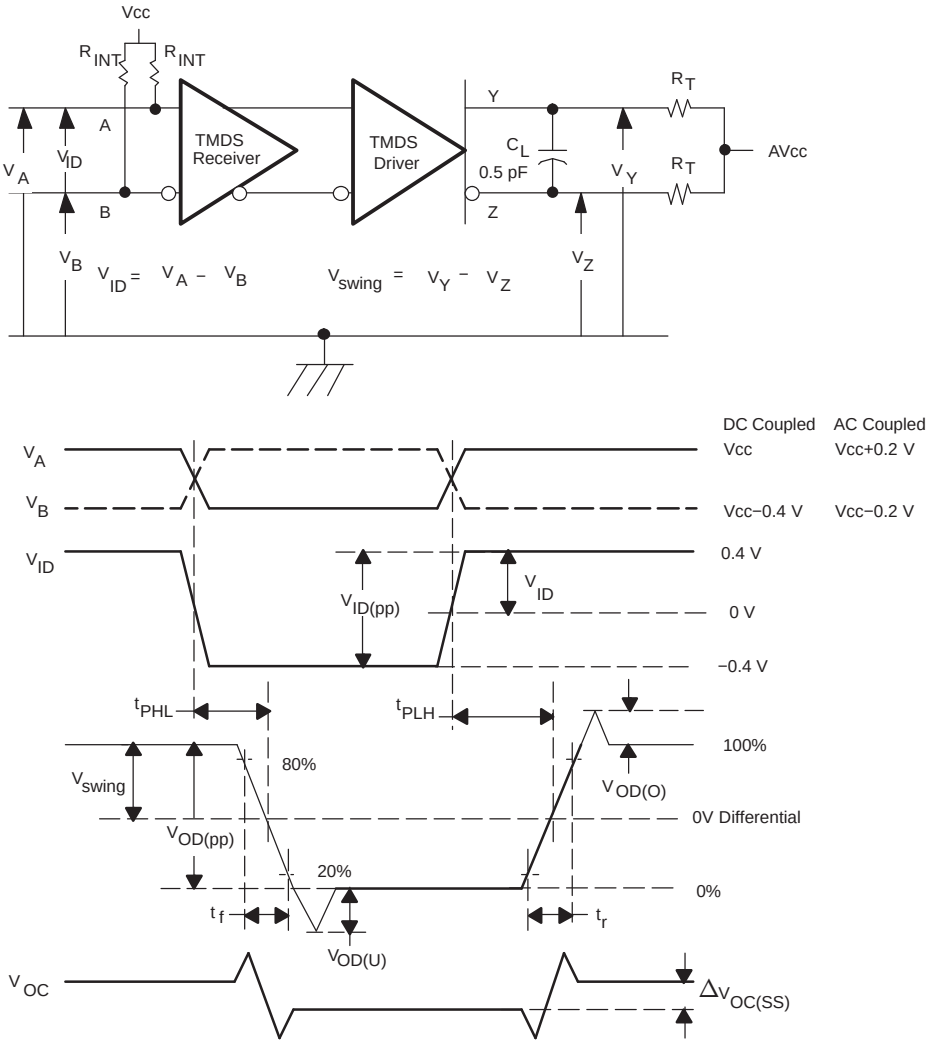


Figure 1. Termination for TMDS Output Driver



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 100 ps, 100 MHz from Agilent 81250. C_L includes instrumentation and fixture capacitance within 0.06 m of the D.U.T. Measurement equipment provides a bandwidth of 20 GHz minimum.

Figure 2. Timing Test Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION (continued)

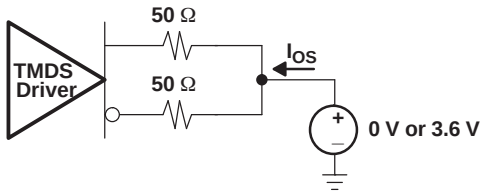


Figure 3. Short Circuit Output Current Test Circuit

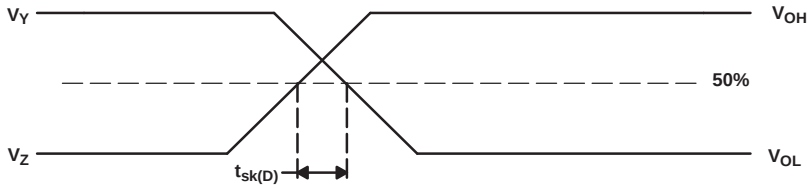
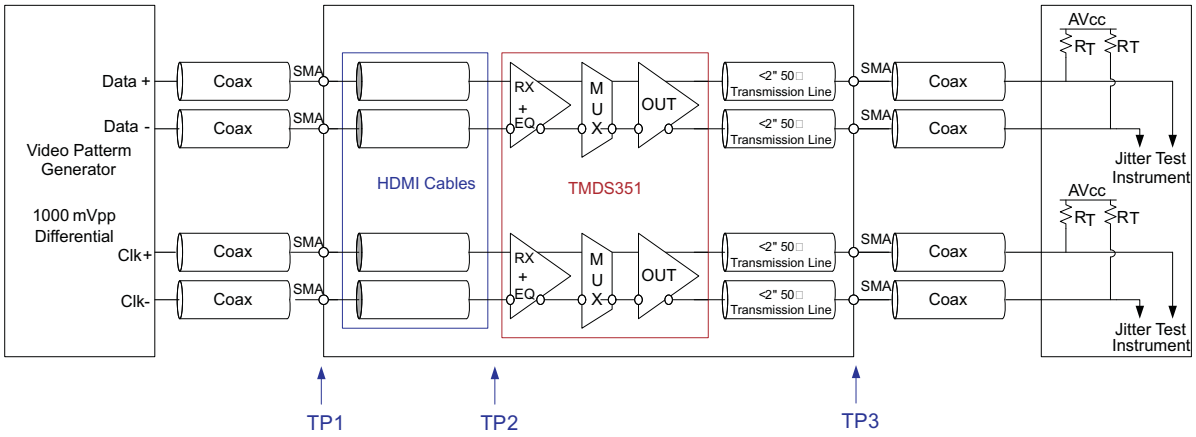


Figure 4. Definition of Intra-Pair Differential Skew



A. HDMI 1.3 compliant cable when EQ = Low, and 10m 28AWG input cable when EQ = High.

B. All jitters are measured in BER of 10^{-9}

C. The residual jitter reflects the total jitter measured at the output of the DUT, TP3, subtract the total jitter from the signal generator, TP1

Figure 5. Jitter Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

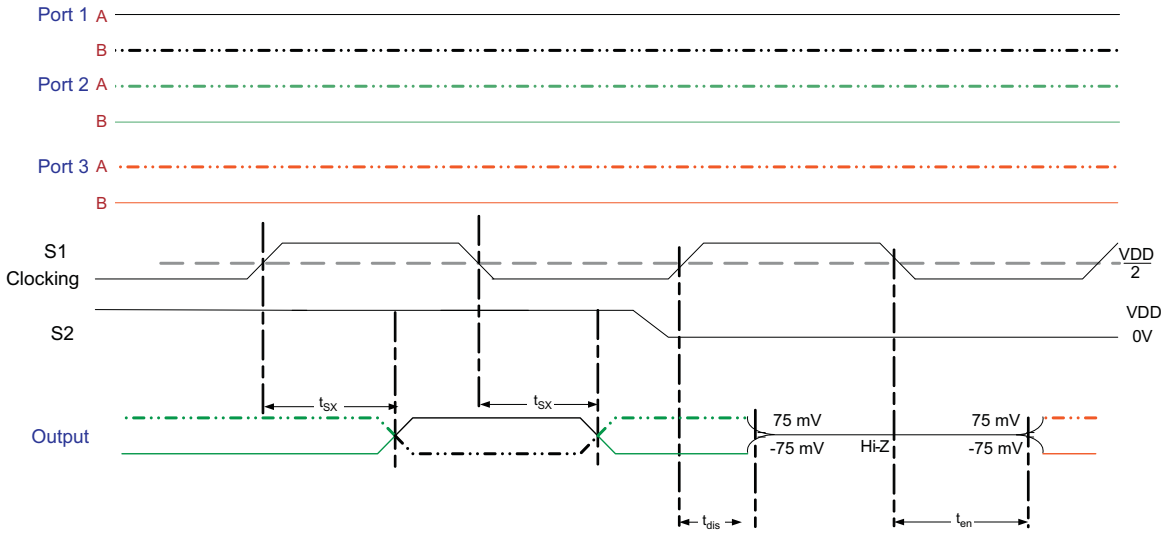


Figure 6. TMDS Outputs Control Timing Definitions

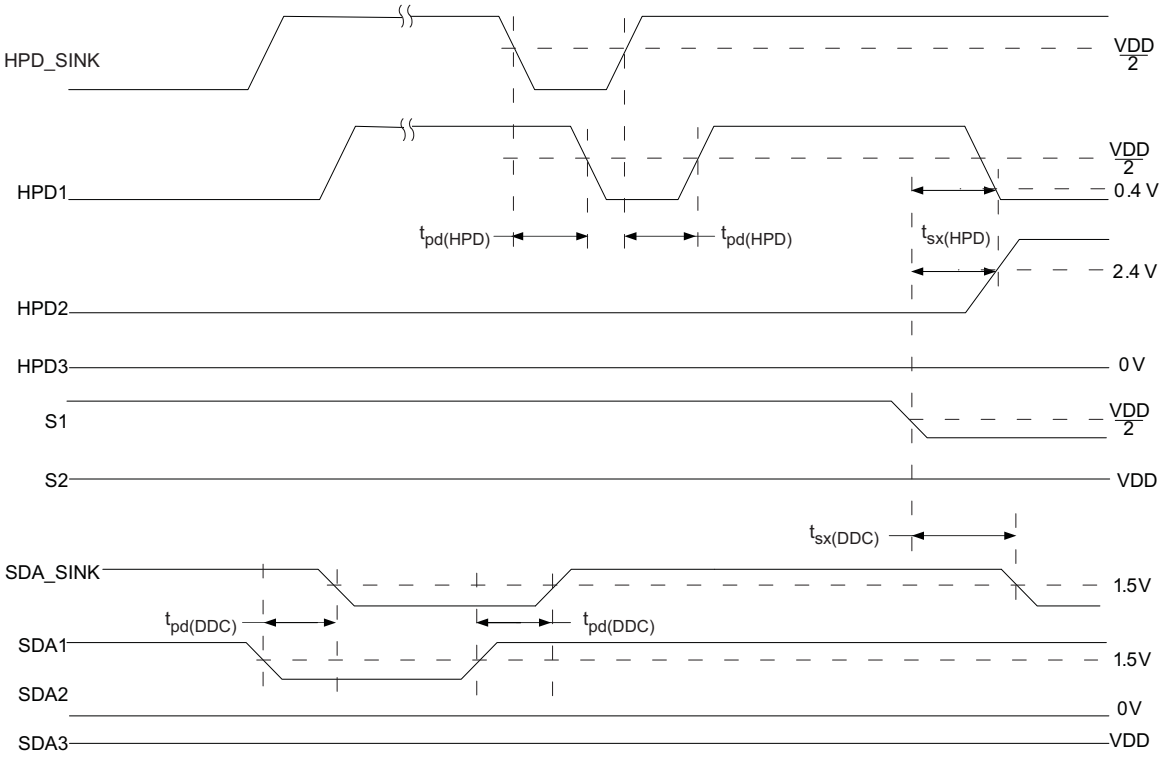


Figure 7. DDC and HPD Timing Definitions

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SIGNAL RATE

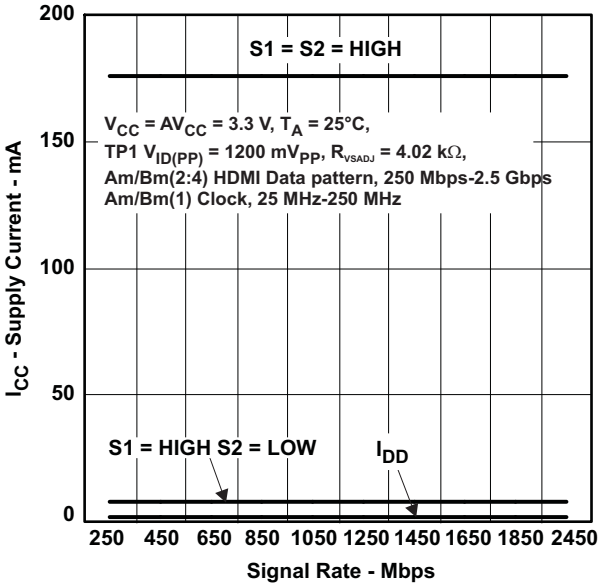


Figure 8.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

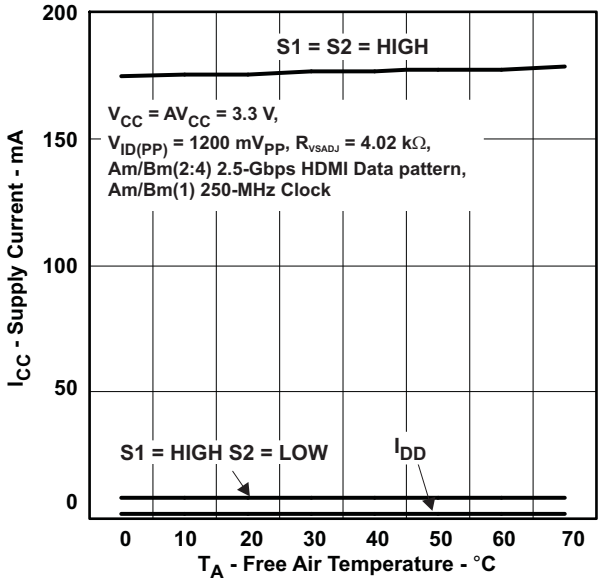
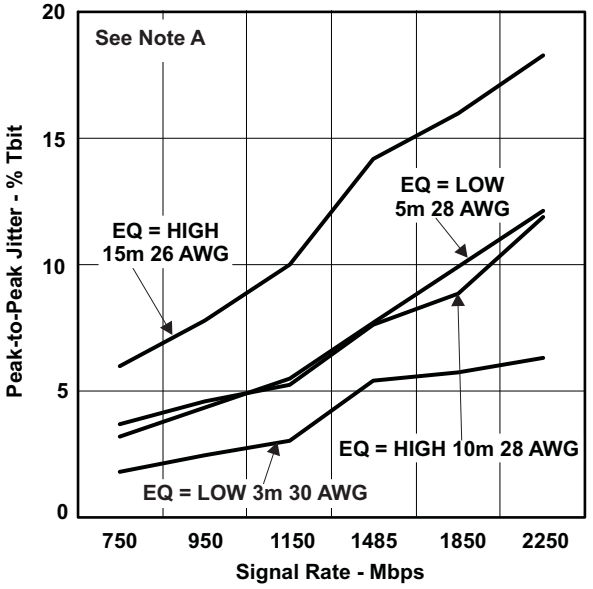


Figure 9.

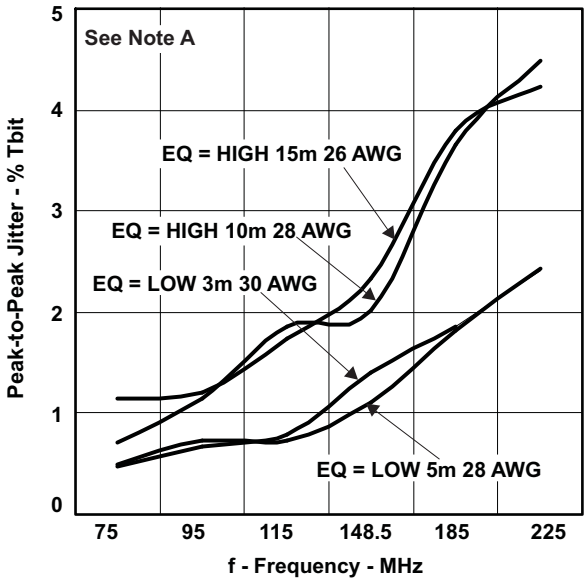
RESIDUAL PEAK-TO-PEAK JITTER
(Data Channels)
vs
SIGNAL RATE



A. Channels 2, 3, 4, V_{CC} = AV_{CC} = 3.3 V, T_A = 25°C, R_{VSADJ} = 4.02 kΩ, See Figure 6

Figure 10.

RESIDUAL PEAK-TO-PEAK JITTER
(Clock Channel)
vs
FREQUENCY

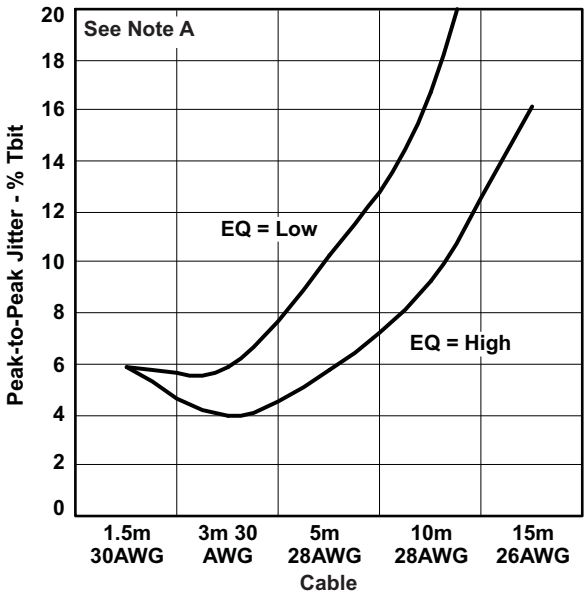


A. Channel 1, V_{CC} = AV_{CC} = 3.3 V, T_A = 25°C, R_{VSADJ} = 4.02 kΩ, See Figure 6

Figure 11.

TYPICAL CHARACTERISTICS (continued)

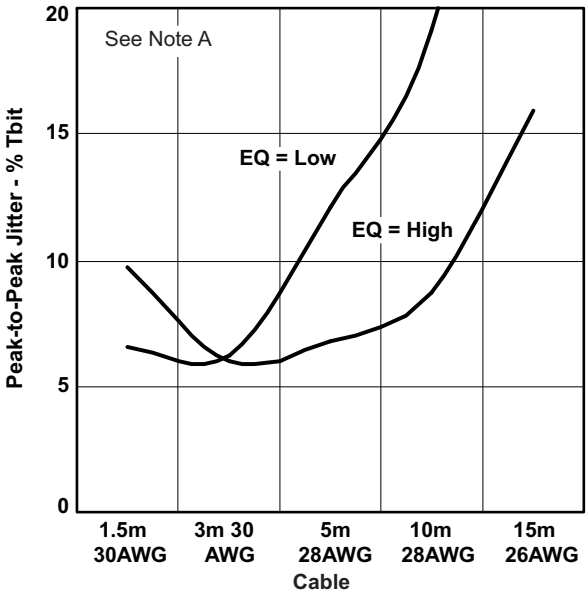
RESIDUAL PEAK-TO-PEAK JITTER (Data Channel) vs CABLE



A. 1080p 10-Bit, V_{CC} = AV_{CC} = 3.3 V, T_A = 25°C, R_{VSADJ} = 4.02 kΩ, See Figure 6, Clock Channel = 185.6 MHz, Data Channel = 1.856 Gbps

Figure 12.

RESIDUAL PEAK-TO-PEAK JITTER (Data Channel) vs CABLE



A. 1080p 12-Bit, V_{CC} = AV_{CC} = 3.3 V, T_A = 25°C, R_{VSADJ} = 4.02 kΩ, See Figure 6, Clock Channel = 222.8 MHz, Data Channel = 2.228 Gbps

Figure 13.

APPLICATION INFORMATION

Supply Voltage

The TMDS351 is powered up with two different power sources. One is 3.3-V V_{CC} for the TMDS circuitry, and the other is 5-V V_{DD} for HPD, DDC, and most of the control logic. It is recommended to provide the same 3.3-V power source to the TMDS circuitry of the TMDS351 and its output termination voltage. This minimizes the leakage current from the ESD protection circuitry. When the digital television (DTV) is in standby mode operation, the same common 3.3-V power source can be turned on or off. Either way will minimize the leakage current in the device, and in the receiver connected at the output where the termination is integrated.

TMDS Inputs

Selectable frequency response equalization circuitries are provided to all twelve differential input to support short range and long range cable connections. The frequency response compensation curves and target cable losses are shown in Figure 14 and Figure 15.

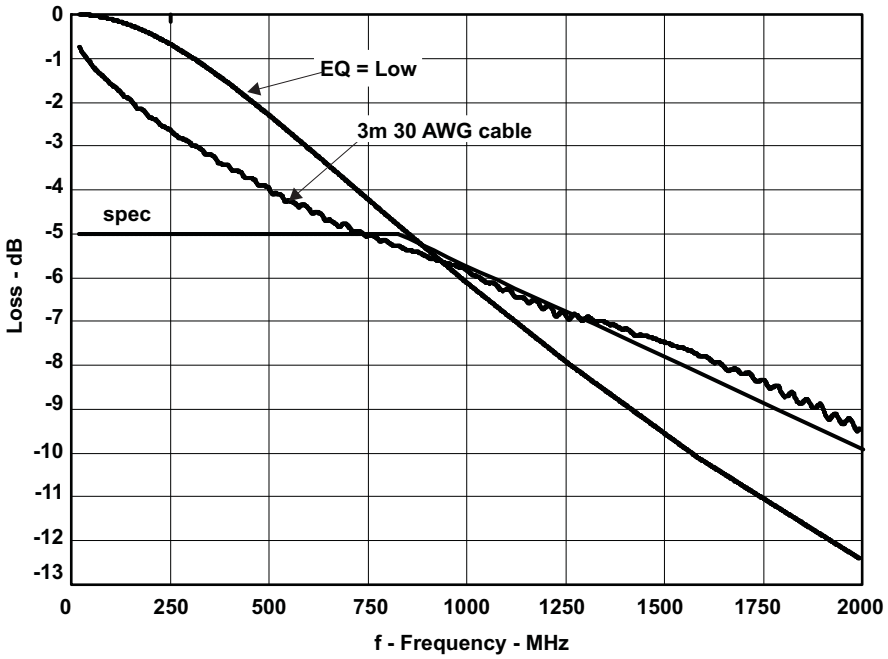


Figure 14. Frequency Response Compensation Curve at EQ = L

APPLICATION INFORMATION (continued)

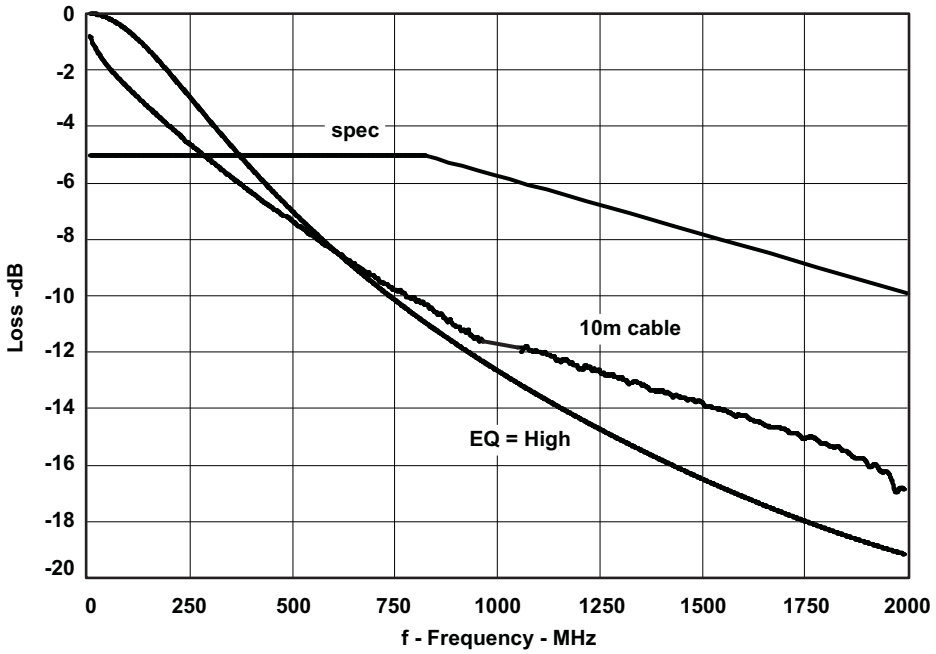


Figure 15. Frequency Response Compensation Curve at EQ = H

Internal termination circuitry which can be switched on or off, provides 50-Ω resistance to each differential input pin when a port is selected. External terminations are not required. When the termination is switched on, current will flow to the TMDS driver. When a port is not selected, the termination is open. This stops supply current flowing from the input pins of the un-selected ports. This switchable termination provides the connected HDMI source another method of determining the sink port status, and whether it is selected or not selected, without referring to the HPD pin status.

TMDS Input Fail-Safe

The TMDS input does not incorporate a fail-safe circuit. To implement fail-safe, the input can be externally biased to prevent output oscillation. One pin can be pulled high to V_{CC} with the other grounded through a 1-kΩ resistor as shown in Figure 16.

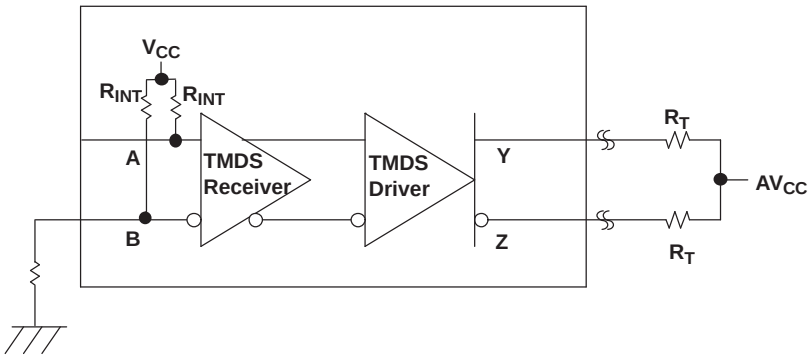


Figure 16. TMDS Input Fail-Safe Recommendation

APPLICATION INFORMATION (continued)

TMDS Outputs

A 10% precision resistor, 4.02-kΩ, is recommended to control the output swing to the HDMI compliant 400 mV to 600 mV range (500 mV typical). The TMDS outputs are high impedance under standby mode operation, S1 = H and S2 = L.

HPD Pins

The HPD circuits are powered by the 5-V supply. They provide 5-V TTL output signals to the SOURCE with a typical 1-kΩ output resistance. An external 1-kΩ resistor is not needed here. The HPD output of the selected source port follows the logic level of the HPD_SINK input. Unselected HPD outputs are kept low. When the device is in standby mode, all HPD outputs follow HPD_SINK. A 1-kΩ resistor to ground keeps all HPD outputs low in standby mode if a fixed low state is preferred.

DDC Channels

The DDC circuits (SDA, SCL) are powered by a 5-V supply. The I/O pins can connect to the 5-V termination voltages directly. A 47-kΩ pull-up resistor to the 5 V is recommended on the SCL1, SCL2, and SCL3 pins. There is no pull-up resistor on the SDA pins. The pull-up resistor can be replaced with a different value.

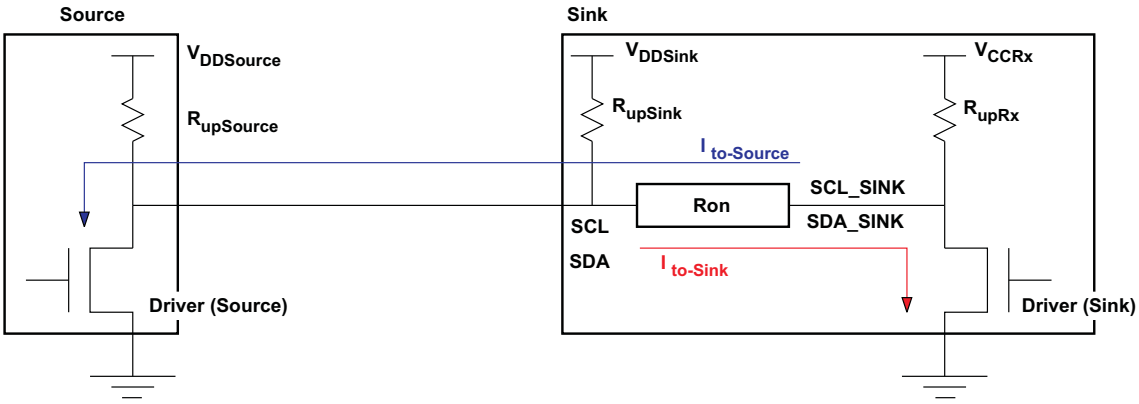


Figure 17. Simplified Electrical Circuit Model for DDC Channel

In Figure 17, when the Driver (Sink) pulls the bus low, the highest voltage level is $V_{ol(Sink)max}$. The current flow through the pass-gate resistor can be presented as:

$$Ito - Sink = \frac{V_{dd} - V_{ol(Sink)max}}{R_{upSource} \parallel R_{upSink}} \quad (1)$$

where the $V_{ddsource} = V_{ddsink} = V_{dd}$

To simplify the equation, $V_{ol(Sink)max}$ is set equal to 0 V to reach equation (2):

$$Ito - Sink = \frac{V_{dd}}{R_{upSource} \parallel R_{upSink}} \quad (2)$$

The voltage at the input of the SINK is Ito - Sink × Ron + $V_{ol(Sink)max}$, which should be lower than the minimum input low threshold voltage of the Driver (Source), $V_{ith(Source)min}$ to keep the bus in correct interoperations.

$$V_{ith(Source)min} > Ito - Sink \times Ron + V_{ol(Sink)max} \quad (3)$$

By combining equations (2) and (3), the minimum pull-up resistor at the Sink input is:

$$R_{upSink} \geq \frac{V_{dd} \times Ron \times R_{upSource}}{(V_{ith(Source)min} - V_{ol(Sink)max}) \times R_{upSource} - V_{dd} \times Ron} \quad (4)$$

APPLICATION INFORMATION (continued)

Applying the same methodology to calculate the pull-up resistor at the input of the Driver (Sink), the minimum pull-up resistor is:

$$R_{upRx} \geq \frac{V_{ccRx} \times Ron}{(V_{ith(Sink)min} - V_{ol(Source)max})} \quad (5)$$

The data sheet V_{PASS} specification ensures the maximum output voltage is clamped at 3.6 V to support a 3.3-V connection. Resistors pulling up to 3.3 V on SCL_SINK and SDA_SINK ensure the high level does not exceed the 3.3-V termination voltage.

Layout Considerations

The high-speed differential TMDS inputs are the most critical paths for the TMDS351. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device:

- Maintain 100-Ω differential transmission line impedance into and out of the TMDS351
- Keep an uninterrupted ground plane beneath the high-speed I/Os
- Keep the ground-path vias to the device as close as possible to allow the shortest return current path
- Keep the trace lengths of the TMDS signals between connector and device as short as possible

Using the TMDS351 in Systems with Different CEC Link Requirements

The TMDS351 supports a DTV with up to three HDMI inputs when used in conjunction with a signal-port HDMI receiver or four HDMI inputs when used in conjunction with a dual-port HDMI receiver. Figure 18 and Figure 19 show simplified application block diagrams for the TMDS351 in different DTVs with different consumer electronic control (CEC) requirements. The CEC is an optional feature of the HDMI interface for centralizing and simplifying user control instructions from multiple audio/video products in an inter-connected system, even when all the audio/video products are from different manufacturers. This feature minimizes the number of remote controls in a system, as well as reducing the number of times buttons need to be pressed.

A DTV Supporting a Passive CEC Link

In Figure 18, the DTV does not have the capability of handling CEC signals, but allows CEC signals to pass over the CEC bus. The source selection is done by the control command of the DTV. The user cannot force the command from any audio/video product on the CEC bus. The selected source reads the E-EDID data after receiving an asserted HPD signal. The micro-controller loads different CEC physical addresses while changing the source by means of the S1 and S2 pins.

E-EDID Reading Configurations in Standby Mode

When the DTV system is in standby mode, the sources will not read the E-EDID memory because the 1-kΩ pull-down resistor keeping the HPD_SINK input at logic low forces all HPD pins to output logic low to all sources. The source will not read the E-EDID data with a low on HPD signal. However, if reading the E-EDID data in the system standby mode is preferred, then TMDS351 can still support this need.

The recommended configuration sequences are:

1. Apply the same 3.3-V power to the V_{CC} of TMDS351 and the TMDS line termination at the HDMI receiver
2. Turn off V_{CC}, and keep V_{DD} on. The TMDS circuit is off, but the HPD, the DDC and the source selection circuits are active.
3. Set S1 and S2 to select the source port which is allowed to read the E-EDID memory.

Please note if the source has a time-out limitation between the 5 V and the HPD signals, the above configuration is not applicable. Uses individual EEPROMs assigned for each input port, see Figure 19. The solution uses E-EDID data to be readable during system power off or standby mode operations.

APPLICATION INFORMATION (continued)

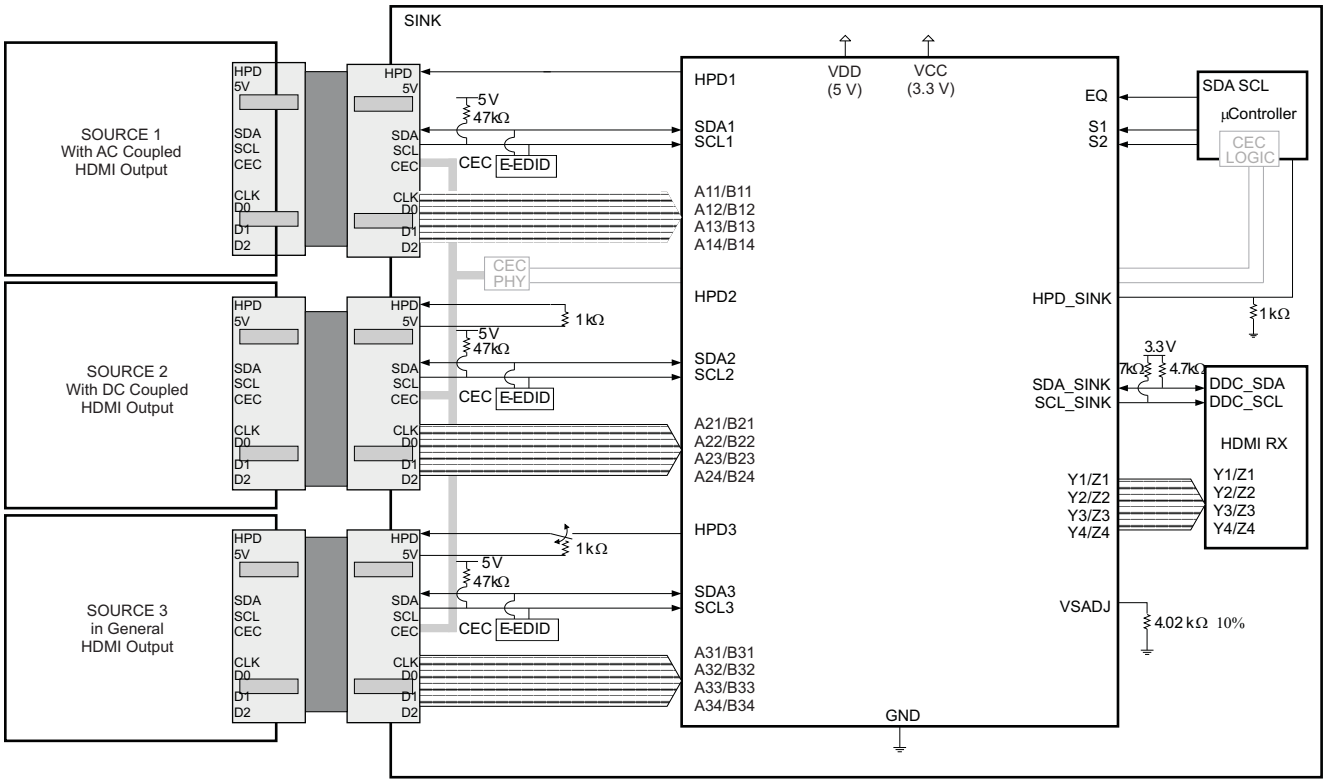


Figure 18. Three-Port HDMI Enabled DTV with TMDS351 – CEC Commands Passing Through

A DTV Supporting an Active CEC Link

In Figure 19, the CEC PHY and CEC LOGIC functions are added. The DTV can initiate and/or react to CEC signals from its remote control or other audio/video products on the same CEC bus. All sources must have their own CEC physical address to support the full functionality of the CEC link.

A source reads its CEC physical address stored its E-EDID memory after receiving a logic-high from the HPD feedback. When HPD is high, the sink-assigned CEC physical address should be maintained. Otherwise, when HPD is low the source sets CEC physical address value to (F.F.F.F).

Case 1 – AC Coupled Source (See Figure 19, Port 1)

When the source TMDS lines are AC coupled or when the source cannot detect the TMDS termination provided in the connected sink, the indication of the source selection can only come from the HPD signal. The TMDS351 HPD1 pin should be applied directly as the HPD signal back to the source.

Case 2 – DC Coupled Source (See Figure 19, Port 2)

When the source TMDS lines are DC coupled, there are two methods to inform the source that it is the active source to the sink. One is checking the HPD signal from the sink, and the other is checking the termination condition in the sink.

In a full CEC operation mode, the HPD signal is set high whether the port is selected or not. The source loads and maintains the CEC physical address when HPD is high. As soon as HPD goes low, the source loses the CEC physical address. To keep the CEC physical address to the source, the HPD signal is looping back from

APPLICATION INFORMATION (continued)

the source provided 5-V signal through a 1-kΩ pull-up resistor in the sink. This method is acceptable in application where the HDMI transmitter can detect the receiver termination by current sensing, and the receiver has switchable termination on the TMDS inputs. The internal termination resistors are connected to the termination voltage when the port is selected, or they are disconnected when the port is not selected. The TMDS351 features switchable termination on the TMDS inputs.

Case 3 – External Logic Control for HPD (See Figure 19, Port 3)

When the HDMI transmitter does not have the capability of detecting the receiver termination, using the HPD signal as a reference for sensing port selections is the only possible method. External control logic for switching the connections of the HPD signals between the HPD pins of the TMDS351 and the 5-V signal from the source provides a good solution.

E-EDID Reading Configurations in Standby Mode

When the TMDS351 is in standby mode operation, S1 = H and S2 = L, all sources can read their E-EDID memories simultaneously with all HPD pins following HPD_SINK in logic-high. HPD_SINK input low will prevent E-EDID reading in standby mode operation.

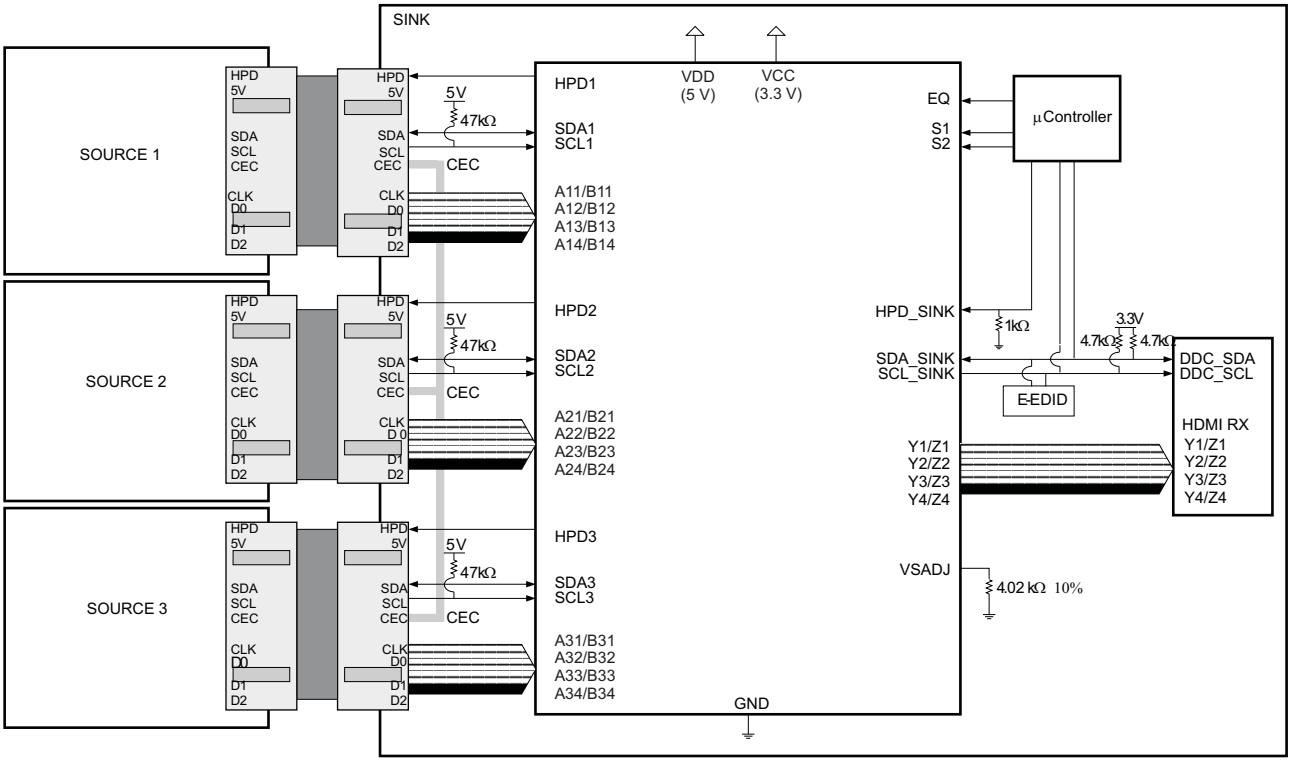
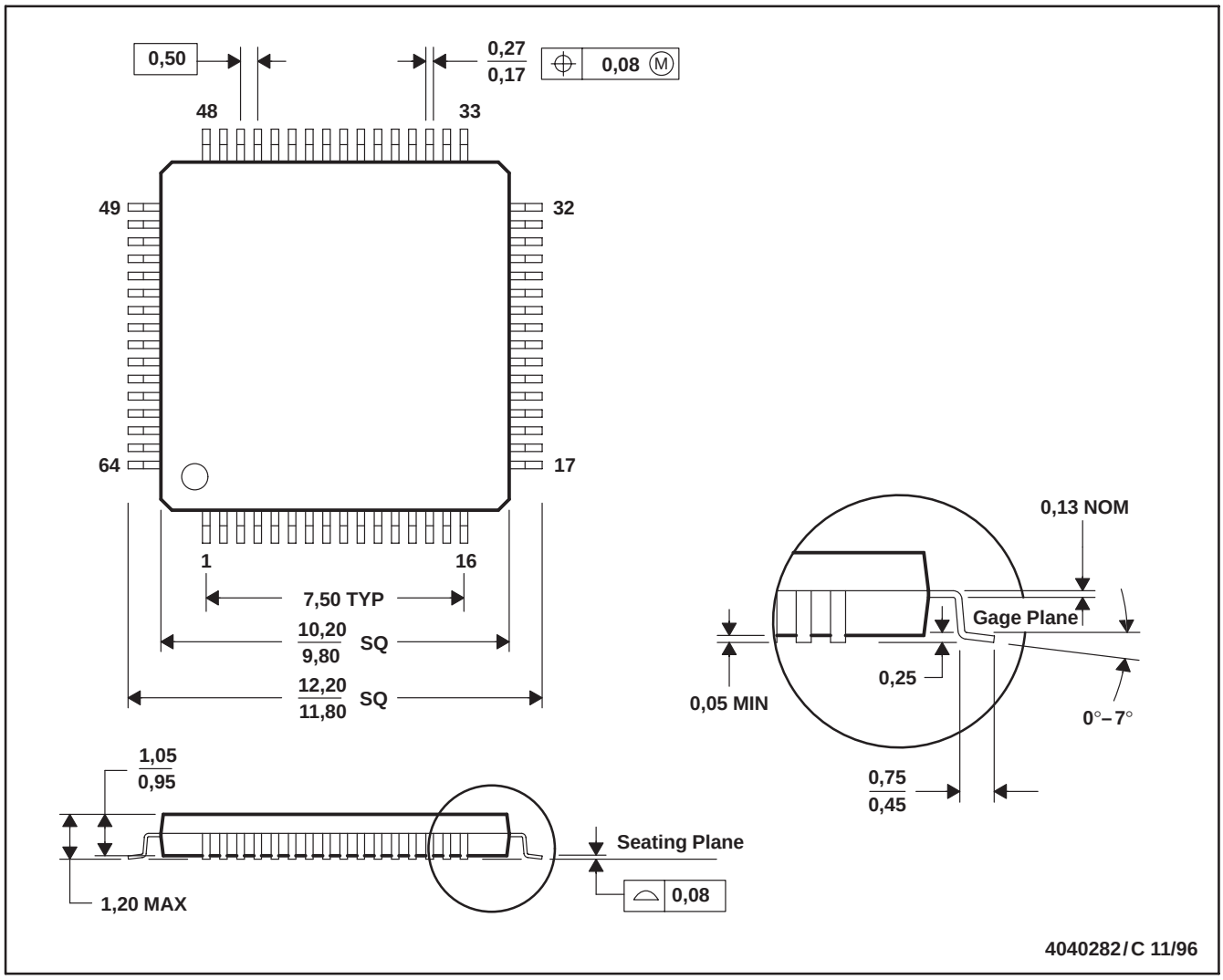


Figure 19. Three-Port HDMI Enabled DTV with TMDS351 – CEC Commands Active

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMDS351PAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TMDS351PAGG4	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TMDS351PAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TMDS351PAGRG4	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

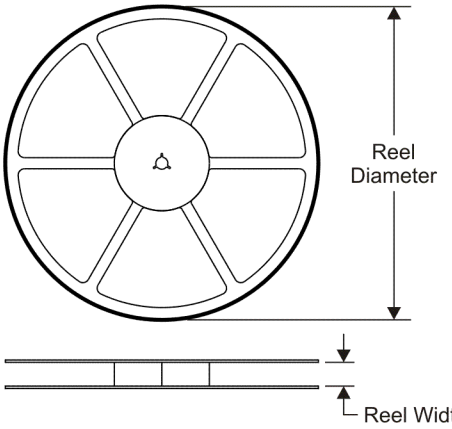
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

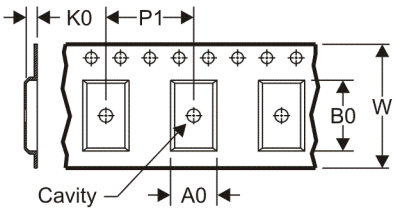
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

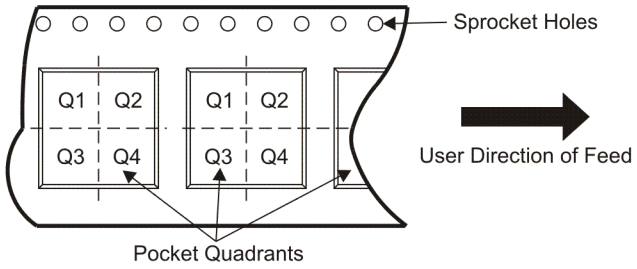


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

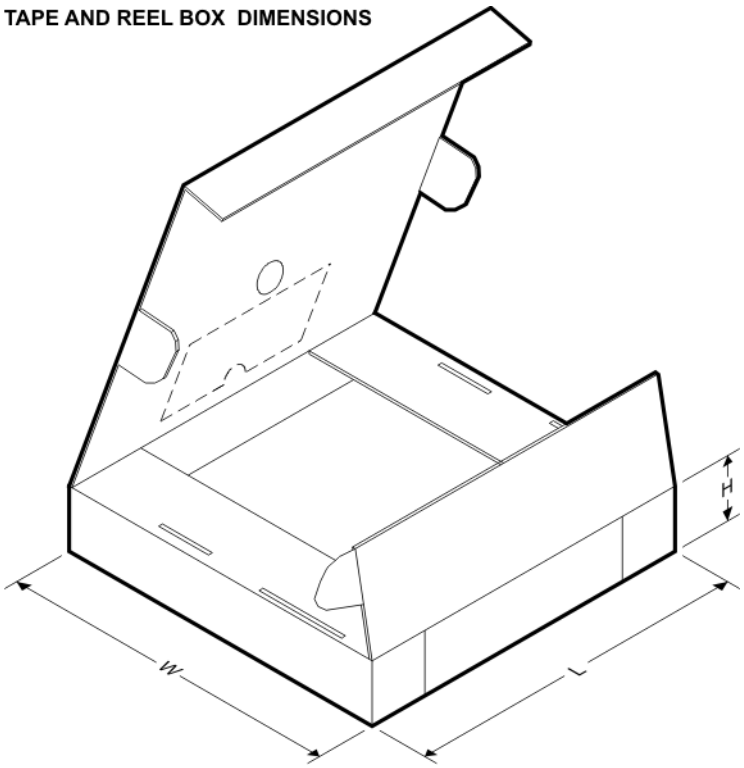
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMDS351PAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.4	16.0	24.0	Q2

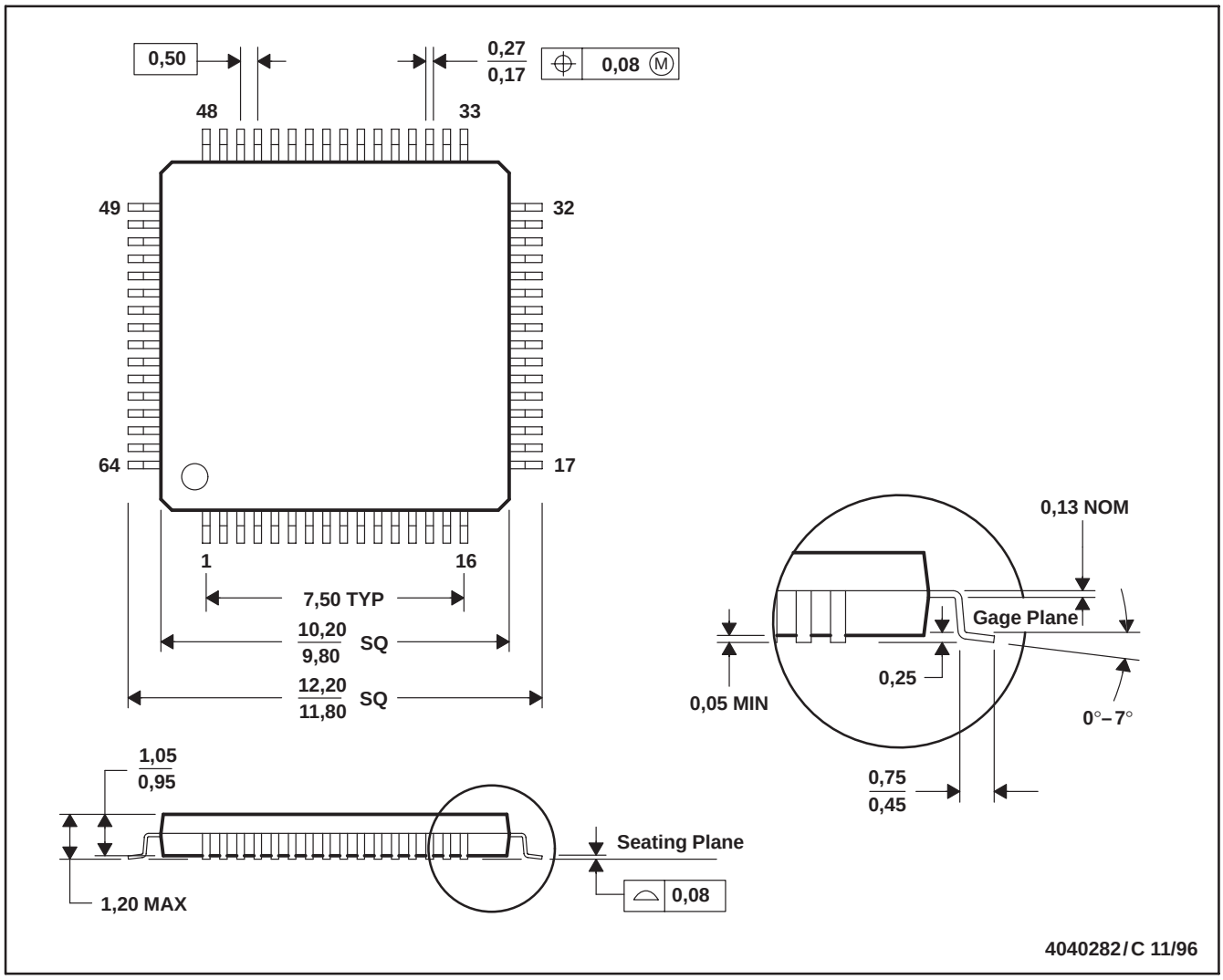
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMDS351PAGR	TQFP	PAG	64	1500	346.0	346.0	41.0

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



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