

TLV2241, TLV2242, TLV2244 FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

SLOS329C – JULY 2000 REVISED - NOVEMBER 2000

- Micropower Operation . . . 1 μ A/Channel
- Rail-to-Rail Input/Output
- Gain Bandwidth Product . . . 5.5 kHz
- Supply Voltage Range . . . 2.5 V to 12 V
- Specified Temperature Range
 - $T_A = 0^\circ\text{C}$ to 70°C . . . Commercial Grade
 - $T_A = -40^\circ\text{C}$ to 125°C . . . Industrial Grade
- Ultrasmall Packaging
 - 5-Pin SOT-23 (TLV2241)
 - 8-Pin MSOP (TLV2242)
- Universal OpAmp EVM

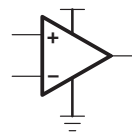
description

The TLV224x family of single-supply operational amplifiers offers very low supply current of only 1 μ A per channel.

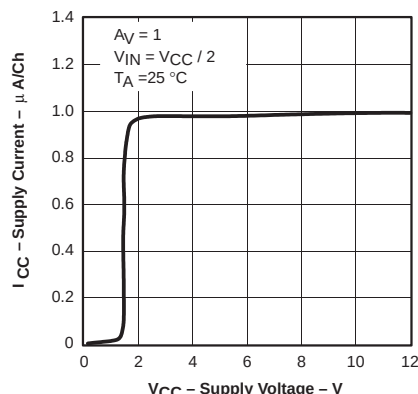
The low supply current is coupled with extremely low input bias currents enabling them to be used with mega- Ω resistors making them ideal for portable, long active life, applications. DC accuracy is ensured with a low typical offset voltage as low as 600 μ V, CMRR of 100 dB, and minimum open loop gain of 100 V/mV at 2.7 V.

The maximum recommended supply voltage is as high as 12 V and ensured operation down to 2.5 V, with electrical characteristics specified at 2.7 V, 5 V and 12 V. The 2.5-V operation makes it compatible with Li-Ion battery-powered systems and many micropower microcontrollers available today including TI's MSP430.

Operational Amplifier



SUPPLY CURRENT
vs
SUPPLY VOLTAGE



FAMILY PACKAGE TABLE

DEVICE	NO. OF Ch	PACKAGE TYPES					UNIVERSAL EVM
		PDIP	SOIC	SOT-23	TSSOP	MSOP	
TLV2241	1	8	8	5	—	—	Refer to the EVM Selection Guide (Lit# SLOU060)
TLV2242	2	8	8	—	—	8	
TLV2244	4	14	14	—	14	—	

SELECTION OF SINGLE SUPPLY OPERATIONAL AMPLIFIER PRODUCTS[†]

DEVICE	V _{DD} (V)	V _{IO} (mV)	BW (MHz)	SLEW RATE (V/ μ s)	I _{DD} (PER CHANNEL) (μ A)	RAIL-TO-RAIL
TLV240x [‡]	2.5–16	0.390	0.005	0.002	0.880	I/O
TLV224x	2.5–12	0.600	0.005	0.002	1	I/O
TLV2211	2.7–10	0.450	0.065	0.025	13	O
TLV245x	2.7–6	0.020	0.22	0.110	23	I/O
TLV225x	2.7–8	0.200	0.2	0.12	35	O

[†] All specifications are typical values measured at 5 V.

[‡] This device also offers 18-V reverse battery protection and 5-V over-the-rail operation on the inputs.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TLV2241, TLV2242, TLV2244

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TLV2241 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	SOT-23‡ (DBV)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	3000 μ V	TLV2241CD	—	—	—
–40°C to 125°C		TLV2241ID	TLV2241IDBV	VBEI	TLV2241IP

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2241CDR).

‡ This package is available in a 250 piece mini-reel. To order this package, add a T suffix to the part number (e.g., TLV2241IDBVT). This package is also available in a 3000 piece reel, add a R suffix to the part number (e.g., TLV2241IDBVR).

TLV2242 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES			
		SMALL OUTLINE† (D)	MSOP† (DGK)	SYMBOLS	PLASTIC DIP (P)
0°C to 70°C	3000 μ V	TLV2242CD	—	—	—
–40°C to 125°C		TLV2242ID	TLV2242IDGK	xxTIALE	TLV2242IP

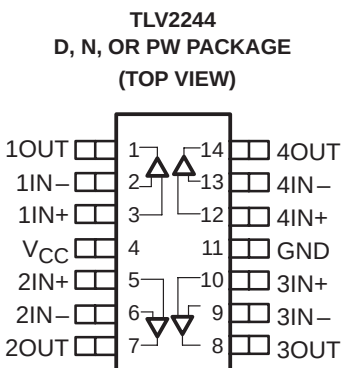
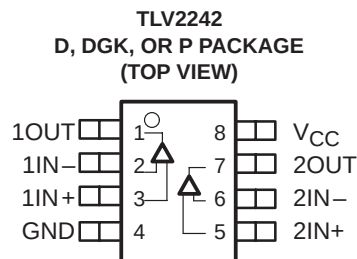
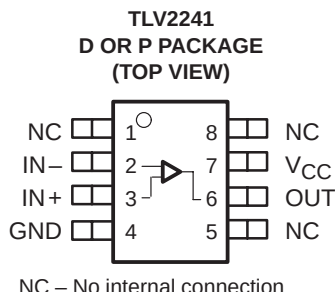
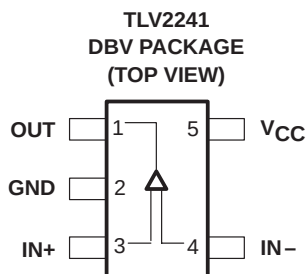
† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2242CDR).

TLV2244 AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGED DEVICES		
		SMALL OUTLINE† (D)	PLASTIC DIP (N)	TSSOP (PW)
0°C to 70°C	3000 μ V	TLV2244CD	—	—
–40°C to 125°C		TLV2244ID	TLV2244IN	TLV2244IPW

† This package is available taped and reeled. To order this packaging option, add an R suffix to the part number (e.g., TLV2244CDR).

TLV224x PACKAGE PINOUTS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	16.5 V
Differential input voltage, V_{ID}	$\pm V_{CC}$
Input current, I_I (any input)	± 10 mA
Output current, I_O	± 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : C suffix	0°C to 70°C
I suffix	–40°C to 125°C
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential voltages, are with respect to GND

DISSIPATION RATING TABLE

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D (8)	38.3	176	710 mW	142 mW
D (14)	26.9	122.6	1022 mW	204.4 mW
DBV (5)	55	324.1	385 mW	77.1 mW
DGK (8)	54.2	259.9	481 mW	96.2 mW
N (14)	32	78	1600 mW	320.5 mW
P (8)	41	104	1200 mW	240.4 mW
PW (14)	29.3	173.6	720 mW	144 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}	Single supply	2.5	12	V
	Split supply	± 1.25	± 6	
Common-mode input voltage range, V_{ICR}		0	V_{CC}	V
Operating free-air temperature, T_A	C-suffix	0	70	°C
	I-suffix	–40	125	

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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 12 V (unless otherwise noted)[†]

dc performance

PARAMETER	TEST CONDITIONS	T_A [†]	MIN	TYP	MAX	UNIT
V_{IO} Input offset voltage	$V_O = V_{CC}/2 \text{ V}$, $V_{IC} = V_{CC}/2 \text{ V}$, $R_S = 50 \Omega$	25°C		600	3000	μV
		Full range			4500	
αV_{IO} Offset voltage drift		25°C		3		$\mu\text{V}/^\circ\text{C}$
CMRR Common-mode rejection ratio	$V_{IC} = 0 \text{ to } V_{CC}$, $R_S = 50 \Omega$	$V_{CC} = 2.7 \text{ V}$		55	100	dB
		25°C		55	100	
		Full range		50		
		$V_{CC} = 5 \text{ V}$		60	100	
		25°C		60	100	
		Full range		53		
AVD Large-signal differential voltage amplification	$V_{CC} = 2.7 \text{ V}$, $V_{O(pp)} = 1 \text{ V}$, $R_L = 500 \text{ k}\Omega$	$V_{CC} = 12 \text{ V}$		60	100	V/mV
		25°C		60	100	
		Full range		55		
		$V_{CC} = 5 \text{ V}$, $V_{O(pp)} = 3 \text{ V}$, $R_L = 500 \text{ k}\Omega$		100	400	
		25°C		100	400	
		Full range		30		
AVD Large-signal differential voltage amplification	$V_{CC} = 5 \text{ V}$, $V_{O(pp)} = 3 \text{ V}$, $R_L = 500 \text{ k}\Omega$	$V_{CC} = 12 \text{ V}$, $V_{O(pp)} = 6 \text{ V}$, $R_L = 500 \text{ k}\Omega$		250	1000	V/mV
		25°C		250	1000	
		Full range		100		
		$V_{CC} = 12 \text{ V}$, $V_{O(pp)} = 6 \text{ V}$, $R_L = 500 \text{ k}\Omega$		700	1500	
		25°C		700	1500	
		Full range		120		

[†] Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

input characteristics

PARAMETER	TEST CONDITIONS	T_A [†]	MIN	TYP	MAX	UNIT
I_{IO} Input offset current	$V_O = V_{CC}/2 \text{ V}$, $V_{IC} = V_{CC}/2 \text{ V}$, $R_S = 50 \Omega$	25°C		25	250	pA
		TLV224xC			300	
		Full range			400	
I_{IB} Input bias current	$V_O = V_{CC}/2 \text{ V}$, $V_{IC} = V_{CC}/2 \text{ V}$, $R_S = 50 \Omega$	25°C		100	500	pA
		TLV224xC			550	
		Full range			1000	
$r_{i(d)}$ Differential input resistance		25°C		300		$\text{M}\Omega$
$C_{i(c)}$ Common-mode input capacitance	$f = 100 \text{ kHz}$	25°C		3		pF

[†] Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

[‡] Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.



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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 12 V (unless otherwise noted)[†] (continued)

output characteristics

PARAMETER		TEST CONDITIONS		T _A [†]	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	V _{IC} = V _{CC} /2, I _{OH} = −2 μA	V _{CC} = 2.7 V	25°C	2.65	2.68		V
				Full range	2.63			
			V _{CC} = 5 V	25°C	4.95	4.98		
				Full range	4.93			
			V _{CC} = 12 V	25°C	11.95	11.98		
				Full range	11.93			
		V _{IC} = V _{CC} /2, I _{OH} = −50 μA	V _{CC} = 2.7 V	25°C	2.62	2.65		
				Full range	2.6			
			V _{CC} = 5 V	25°C	4.92	4.95		
				Full range	4.9			
			V _{CC} = 12 V	25°C	11.92	11.95		
				Full range	11.9			
V _{OL}	Low-level output voltage	V _{IC} = V _{CC} /2, I _{OL} = 2 μA		25°C		90	150	mV
				Full range			180	
		V _{IC} = V _{CC} /2, I _{OL} = 50 μA		25°C		180	230	
				Full range			260	
I _O	Output current	V _O = 0.5 V from rail		25°C		±200		μA

[†] Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

power supply

PARAMETER	TEST CONDITIONS		T_A [†]	MIN	TYP	MAX	UNIT
I_{CC} Supply current (per channel)	$V_O = V_{CC}/2$	$V_{CC} = 2.7 \text{ V}$ or 5 V	25°C		980	1200	nA
			Full range			1500	
		$V_{CC} = 12 \text{ V}$	25°C		1000	1250	
			Full range			1550	
PSRR Power supply rejection ratio ($\Delta V_{CC}/\Delta V_{IO}$)	$V_{CC} = 2.7$ to 5 V , $V_{IC} = V_{CC}/2 \text{ V}$, No load,	TLV224xC	25°C	70	100		dB
			Full range	65			dB
		TLV224xI	25°C	70	100		dB
			Full range	70			dB
	$V_{CC} = 5$ to 12 V , $V_{IC} = V_{CC}/2 \text{ V}$, No load		25°C	70	100		dB
			Full range	70			dB

[†] Full range is 0°C to 70°C for the C suffix and –40°C to 125°C for the I suffix. If not specified, full range is –40°C to 125°C.

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electrical characteristics at recommended operating conditions, $V_{CC} = 2.7, 5 \text{ V}$, and 12 V (unless otherwise noted)[‡] (continued)

dynamic performance

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
UGBW	Unity gain bandwidth	$R_L = 500 \text{ k}\Omega$,	$C_L = 100 \text{ pF}$	25°C		5.5		kHz
SR	Slew rate at unity gain	$V_{O(pp)} = 0.8 \text{ V}$, $R_L = 500 \text{ k}\Omega$,	$C_L = 100 \text{ pF}$	25°C		2		V/ms
ϕM	Phase margin	$R_L = 500 \text{ k}\Omega$, $C_L = 100 \text{ pF}$		25°C		60		
	Gain margin					15		dB
t_s	Settling time	$V_{CC} = 2.7 \text{ or } 5 \text{ V}$, $V_{(STEP)PP} = 1 \text{ V}$, $C_L = 100 \text{ pF}$, $A_V = -1$, $R_L = 100 \text{ k}\Omega$	0.1%	25°C		1.84		ms
		$V_{CC} = 12 \text{ V}$, $V_{(STEP)PP} = 1 \text{ V}$, $C_L = 100 \text{ pF}$, $A_V = -1$, $R_L = 100 \text{ k}\Omega$	0.1%			6.1		
		$V_{CC} = 12 \text{ V}$, $V_{(STEP)PP} = 1 \text{ V}$, $C_L = 100 \text{ pF}$, $A_V = -1$, $R_L = 100 \text{ k}\Omega$	0.01%			32		

noise/distortion performance

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_n	Equivalent input noise voltage	$f = 10 \text{ Hz}$	25°C		800		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100 \text{ Hz}$			500		
I_n	Equivalent input noise current	$f = 100 \text{ Hz}$			8		$\text{fA}/\sqrt{\text{Hz}}$

[‡] Specifications at 5 V are ensured by design and device testing at 2.7 V and 12 V.

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TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Common-mode input voltage	1, 2, 3
I_{IB}	Input bias current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
I_{IO}	Input offset current	vs Free-air temperature	4, 6, 8
		vs Common-mode input voltage	5, 7, 9
CMRR	Common-mode rejection ratio	vs Frequency	10
V_{OH}	High-level output voltage	vs High-level output current	11, 13, 15
V_{OL}	Low-level output voltage	vs Low-level output current	12, 14, 16
$V_{O(PP)}$	Output voltage peak-to-peak	vs Frequency	17
Z_o	Output impedance	vs Frequency	18
I_{CC}	Supply current	vs Supply voltage	19
PSRR	Power supply rejection ratio	vs Frequency	20
A_{VD}	Differential voltage gain	vs Frequency	21
	Phase	vs Frequency	21
	Gain-bandwidth product	vs Supply voltage	22
SR	Slew rate	vs Free-air temperature	23
ϕ_m	Phase margin	vs Capacitive load	24
	Gain margin	vs Capacitive load	25
	Voltage noise over a 10 Second Period		26
	Large-signal voltage follower		27, 28, 29
	Small-signal voltage follower		30
	Large-signal inverting pulse response		31, 32, 33
	Small-signal inverting pulse response		34
	Crosstalk	vs Frequency	35



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TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

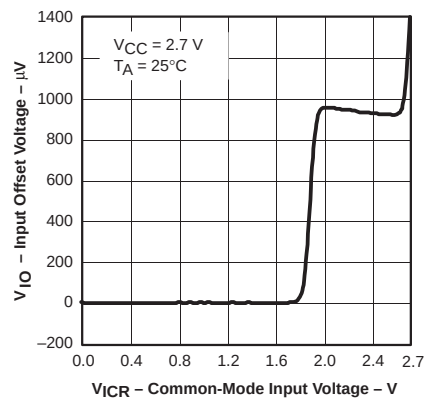


Figure 1

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

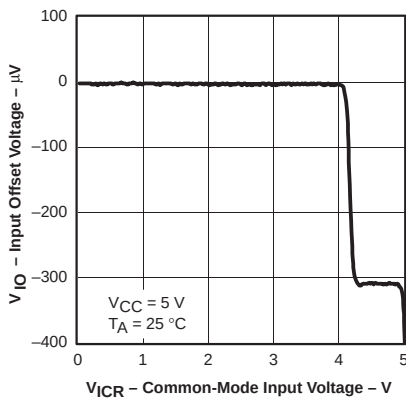


Figure 2

INPUT OFFSET VOLTAGE
vs
COMMON-MODE INPUT
VOLTAGE

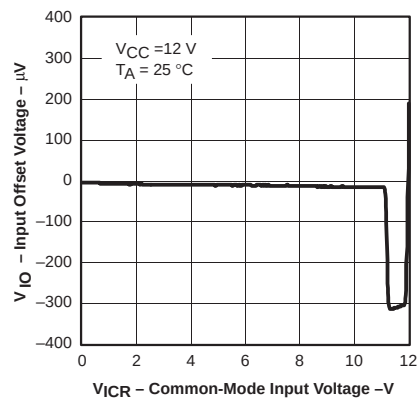


Figure 3

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

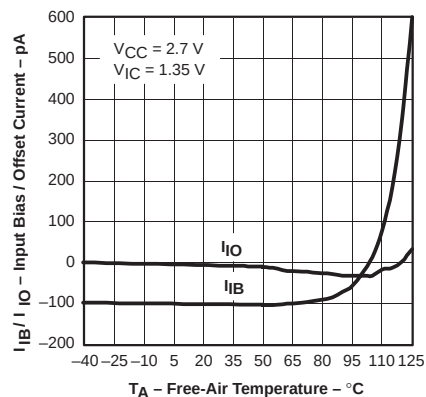


Figure 4

INPUT BIAS / OFFSET CURRENT
vs
COMMON MODE INPUT
VOLTAGE

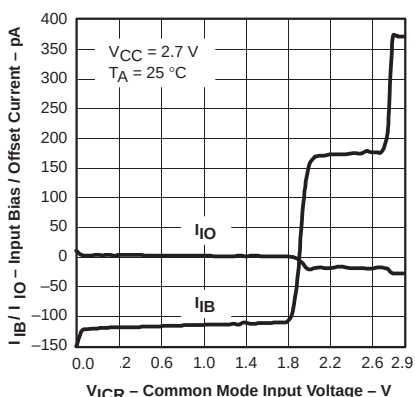


Figure 5

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

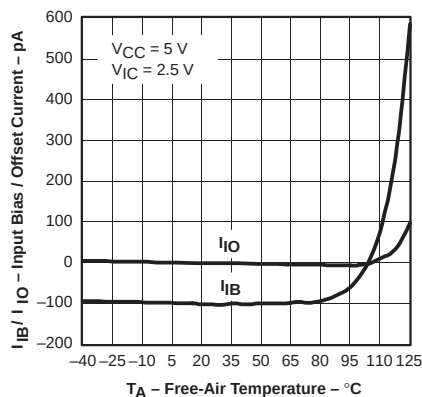


Figure 6

INPUT BIAS / OFFSET CURRENT
vs
COMMON-MODE INPUT
VOLTAGE

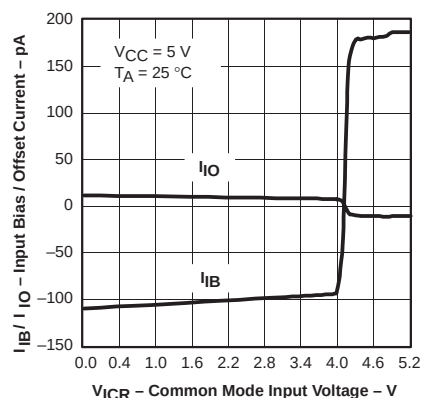


Figure 7

INPUT BIAS / OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

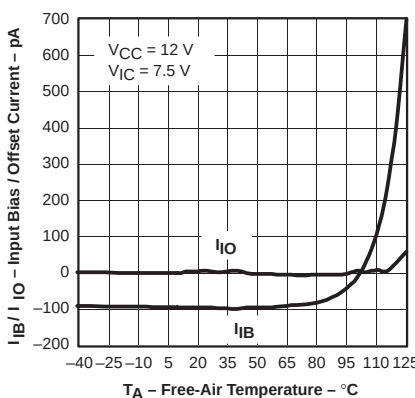


Figure 8

INPUT BIAS / OFFSET CURRENT
vs
COMMON-MODE INPUT
VOLTAGE

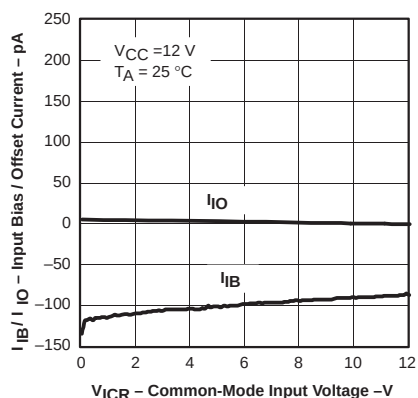


Figure 9



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TYPICAL CHARACTERISTICS

**COMMON-MODE REJECTION RATIO
VS
FREQUENCY**

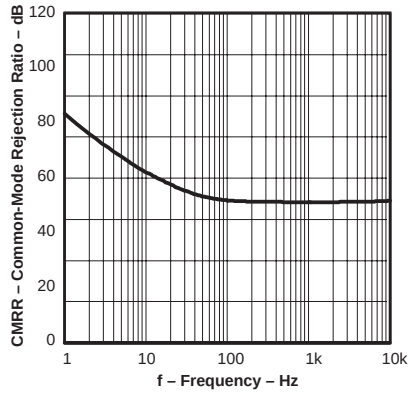


Figure 10

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

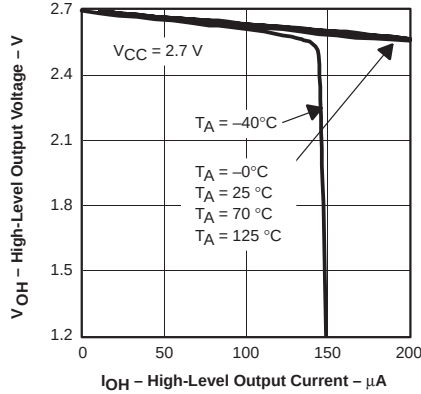


Figure 11

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

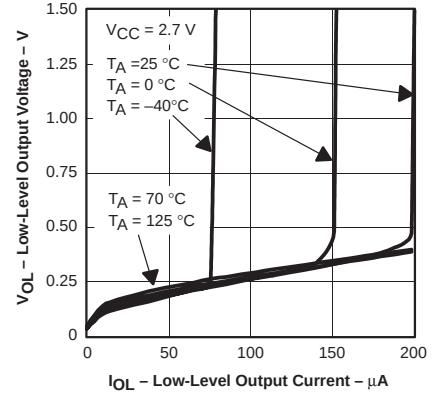


Figure 12

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

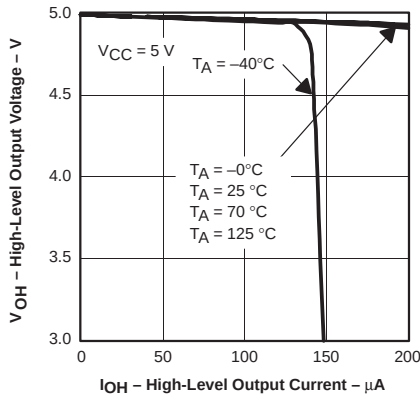


Figure 13

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

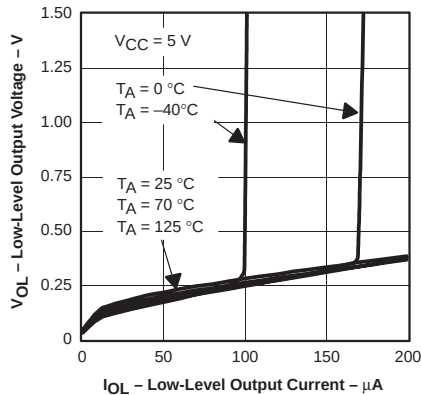


Figure 14

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

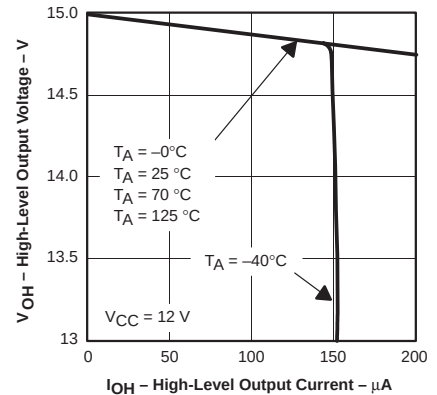


Figure 15

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

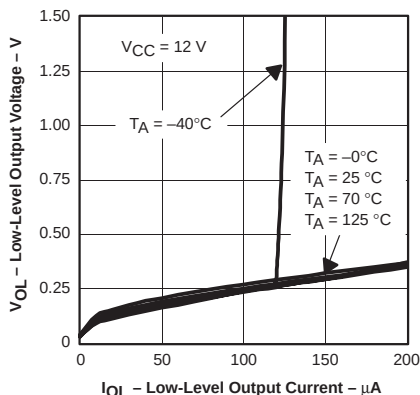


Figure 16

**OUTPUT VOLTAGE
PEAK-TO-PEAK
VS
FREQUENCY**

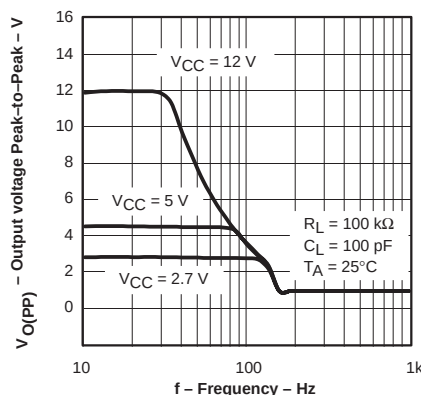


Figure 17

**OUTPUT IMPEDANCE
VS
FREQUENCY**

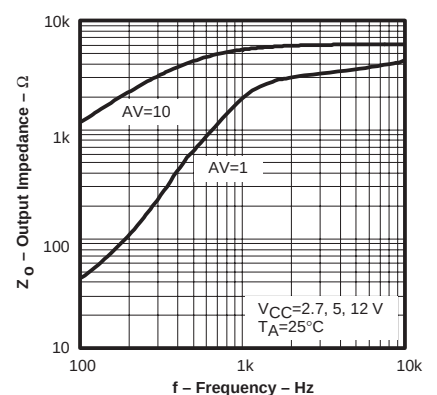


Figure 18

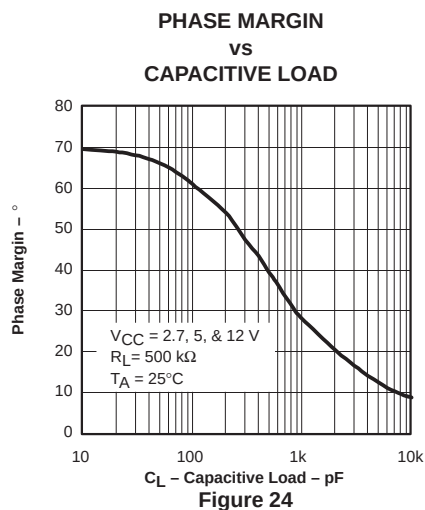
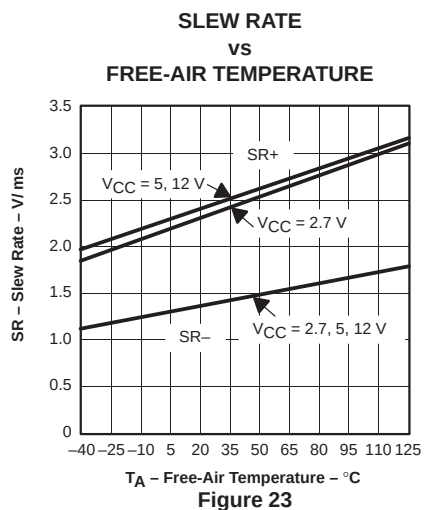
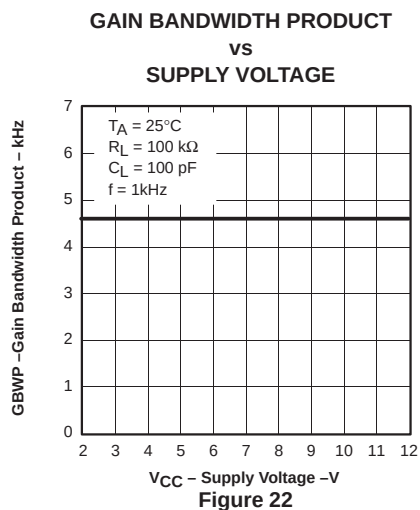
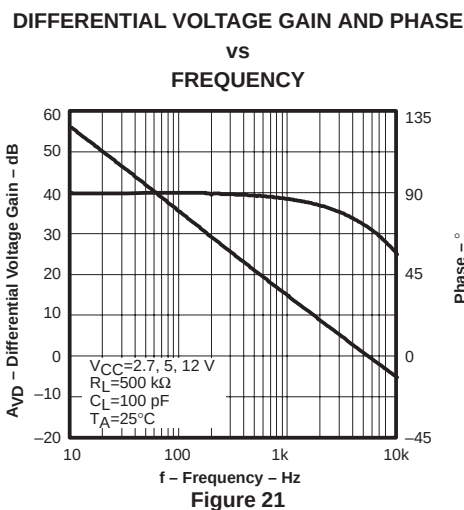
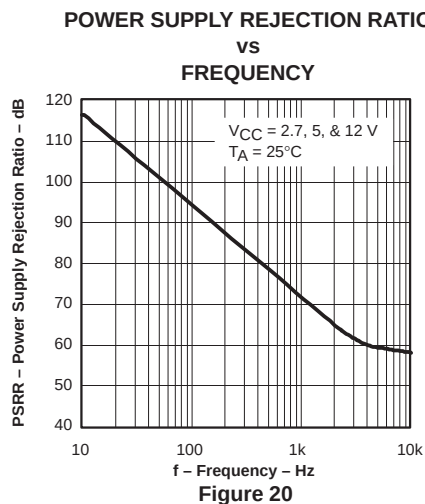
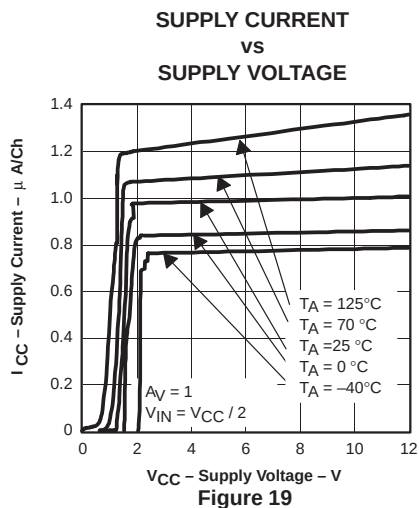


TLV2241, TLV2242, TLV2244

FAMILY OF 1- μ A/ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS



TLV2241, TLV2242, TLV2244

FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

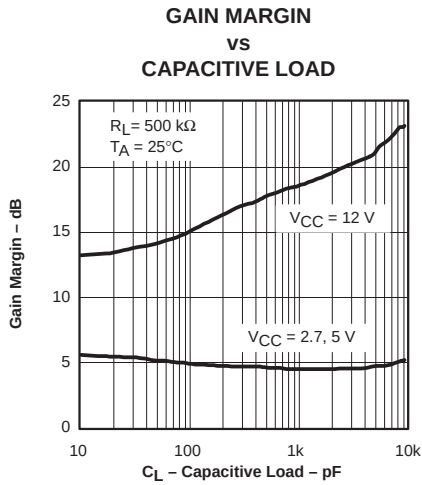


Figure 25

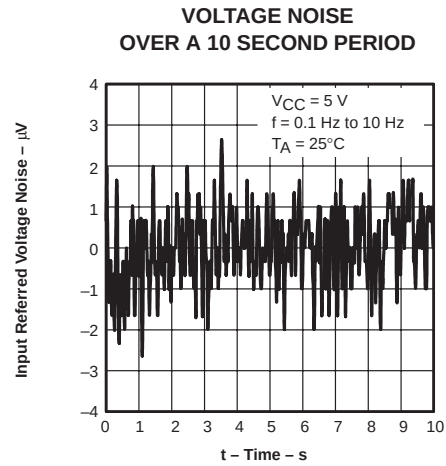


Figure 26

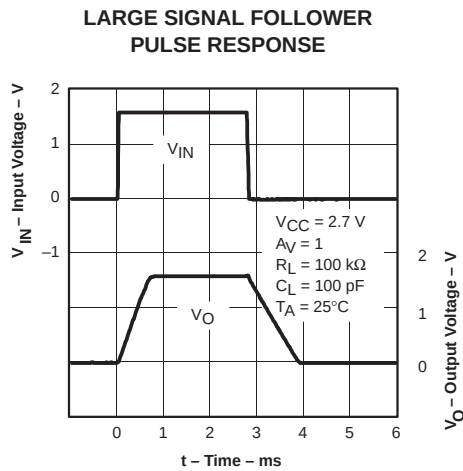


Figure 27

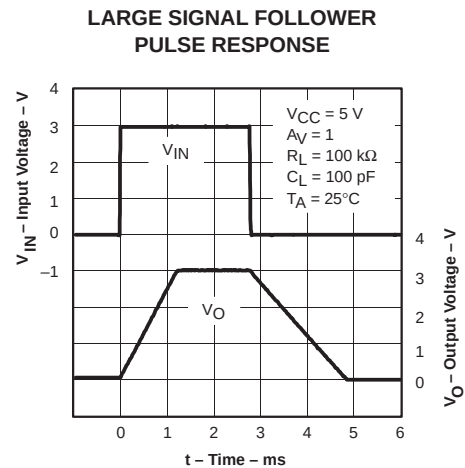


Figure 28

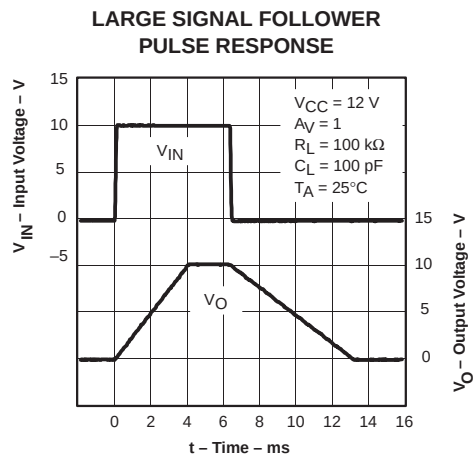


Figure 29

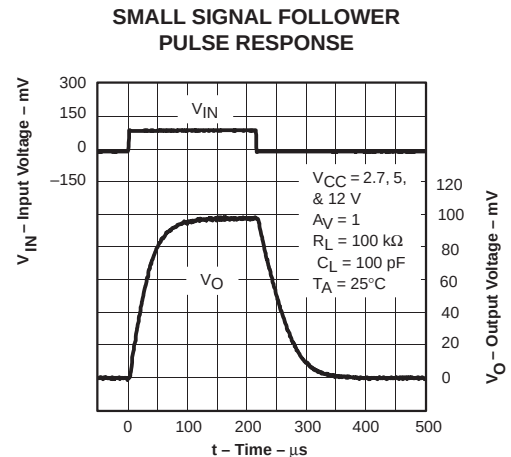


Figure 30

TLV2241, TLV2242, TLV2244

FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT

OPERATIONAL AMPLIFIERS

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TYPICAL CHARACTERISTICS

LARGE SIGNAL INVERTING PULSE RESPONSE

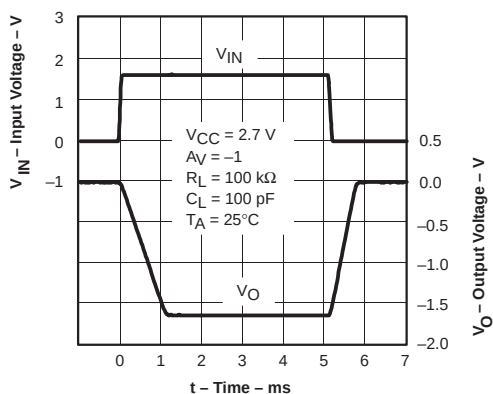


Figure 31

LARGE SIGNAL INVERTING PULSE RESPONSE

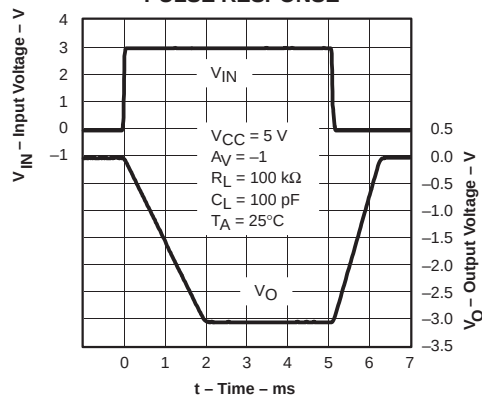


Figure 32

LARGE SIGNAL INVERTING PULSE RESPONSE

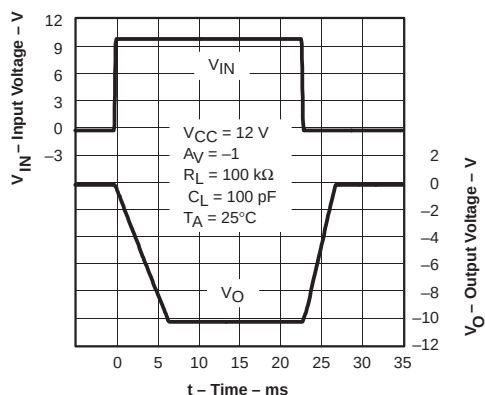


Figure 33

SMALL SIGNAL INVERTING PULSE RESPONSE

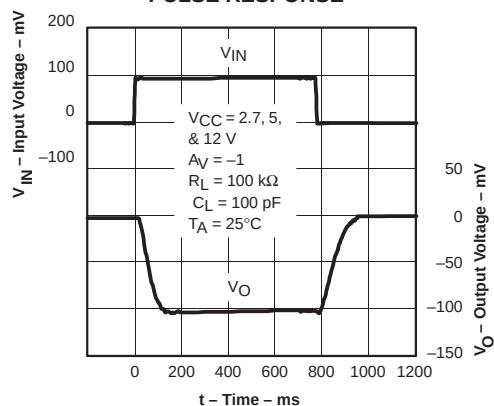


Figure 34

**CROSSTALK
vs
FREQUENCY**

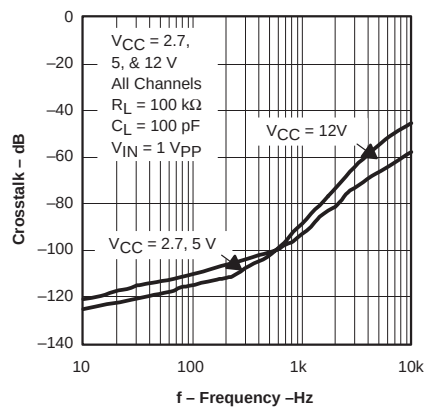
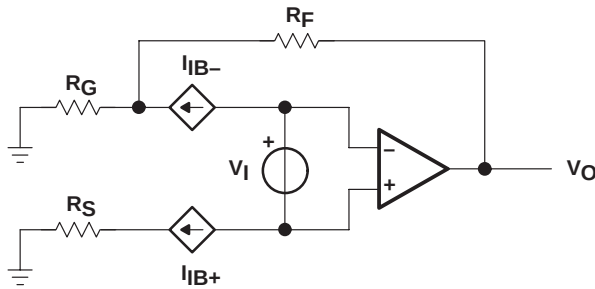


Figure 35

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

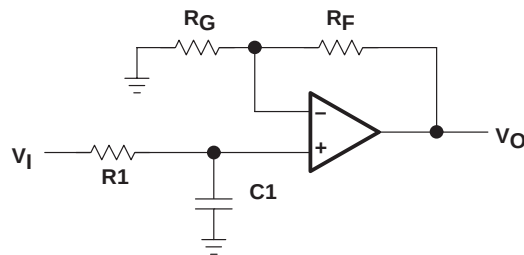


$$V_{OO} = V_{IO} \left(1 + \left(\frac{R_F}{R_G} \right) \right) \pm I_{IB+} R_S \left(1 + \left(\frac{R_F}{R_G} \right) \right) \pm I_{IB-} R_F$$

Figure 36. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 37).

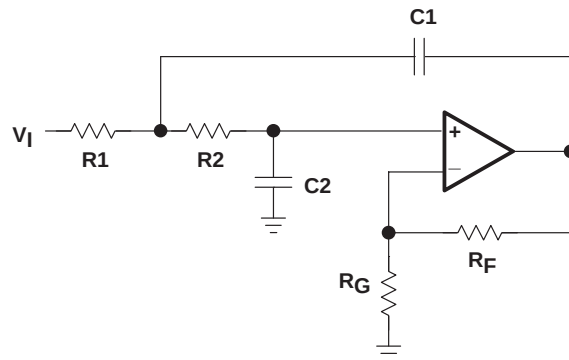


$$f_{-3dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G} \right) \left(\frac{1}{1 + sR_1 C_1} \right)$$

Figure 37. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



$$\begin{aligned} R_1 &= R_2 = R \\ C_1 &= C_2 = C \\ Q &= \text{Peaking Factor} \\ &(\text{Butterworth } Q = 0.707) \end{aligned}$$

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q} \right)}$$

Figure 38. 2-Pole Low-Pass Sallen-Key Filter

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FAMILY OF 1- μ A/ch RAIL-TO-RAIL INPUT/OUTPUT

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APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high performance of the TLV224x, follow proper printed-circuit board design techniques. A general set of guidelines is given in the following.

- **Ground planes**—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- **Proper power supply decoupling**—Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- **Sockets**—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs/compact part placements**—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- **Surface-mount passive components**—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.



APPLICATION INFORMATION

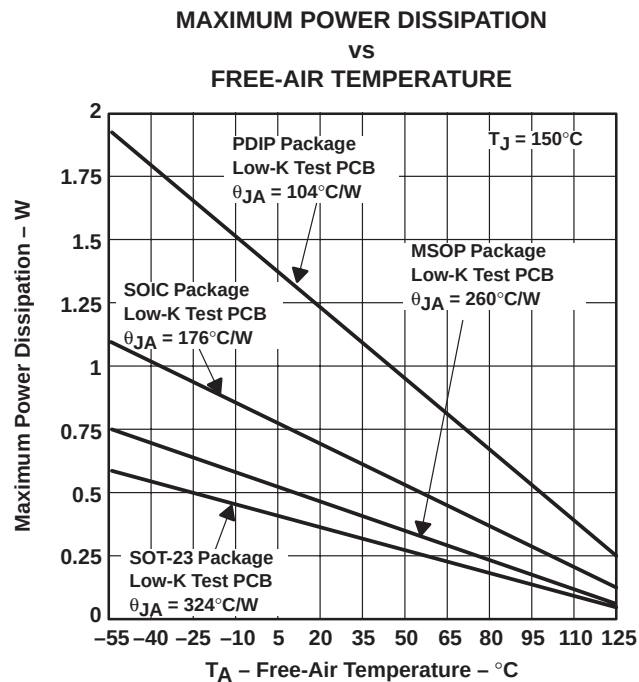
general power dissipation considerations

For a given θ_{JA} , the maximum power dissipation is shown in Figure 39 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of THS224x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 39. Maximum Power Dissipation vs Free-Air Temperature

TLV2241, TLV2242, TLV2244

FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™ Release 8, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 2) and subcircuit in Figure 40 are generated using the TLV224x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 2: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

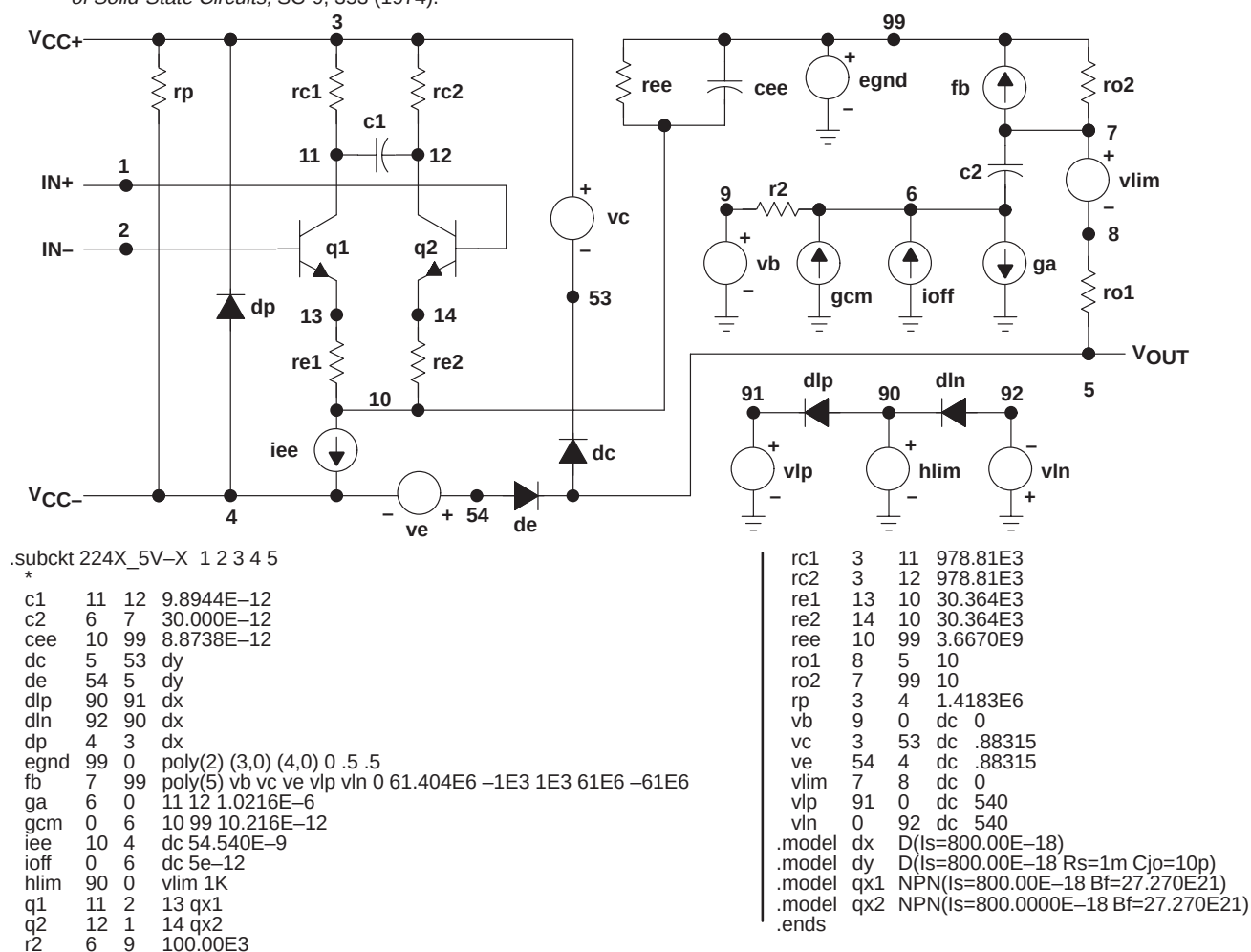


Figure 40. Boyle Macromodels and Subcircuit

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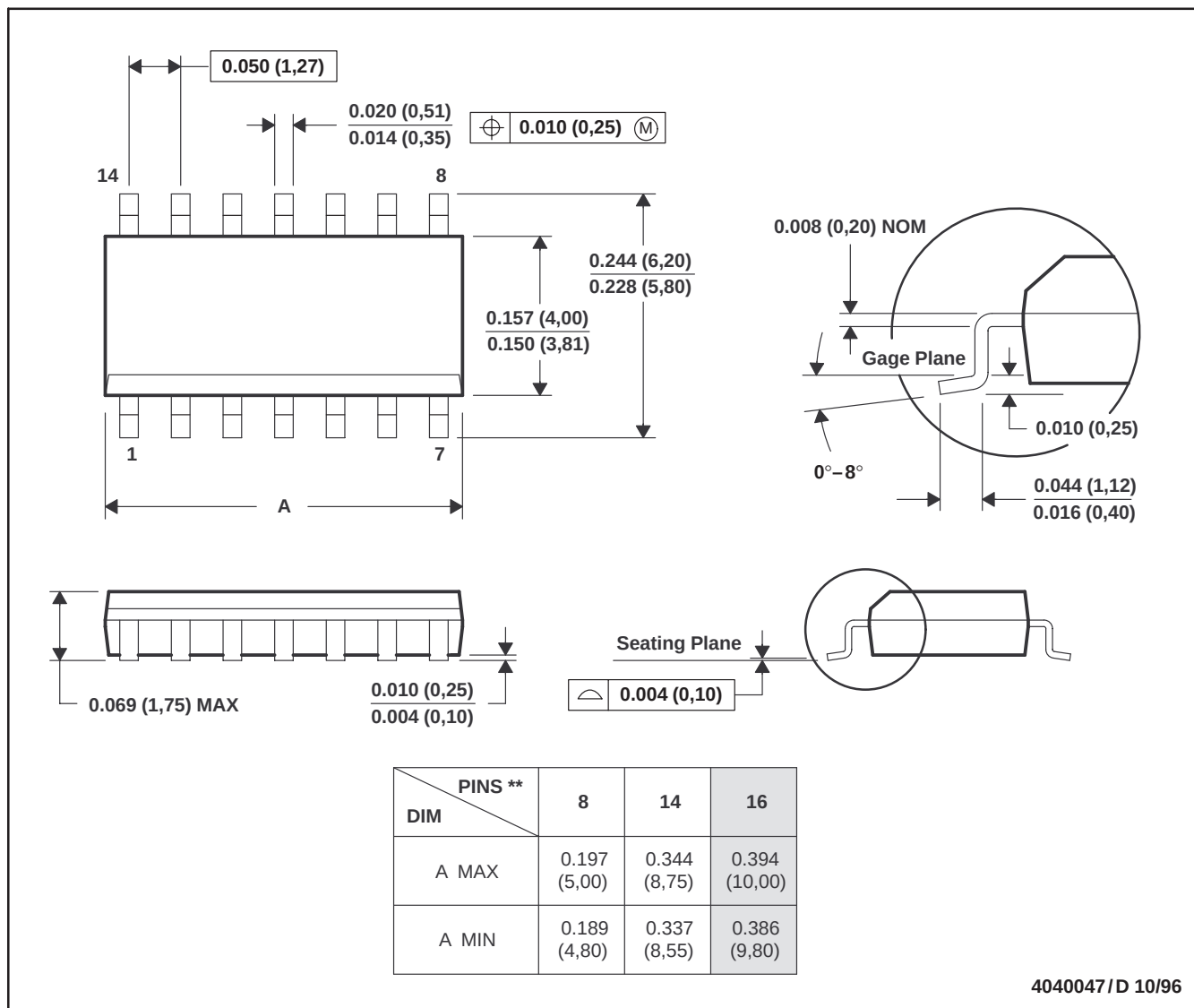
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MECHANICAL DATA

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).

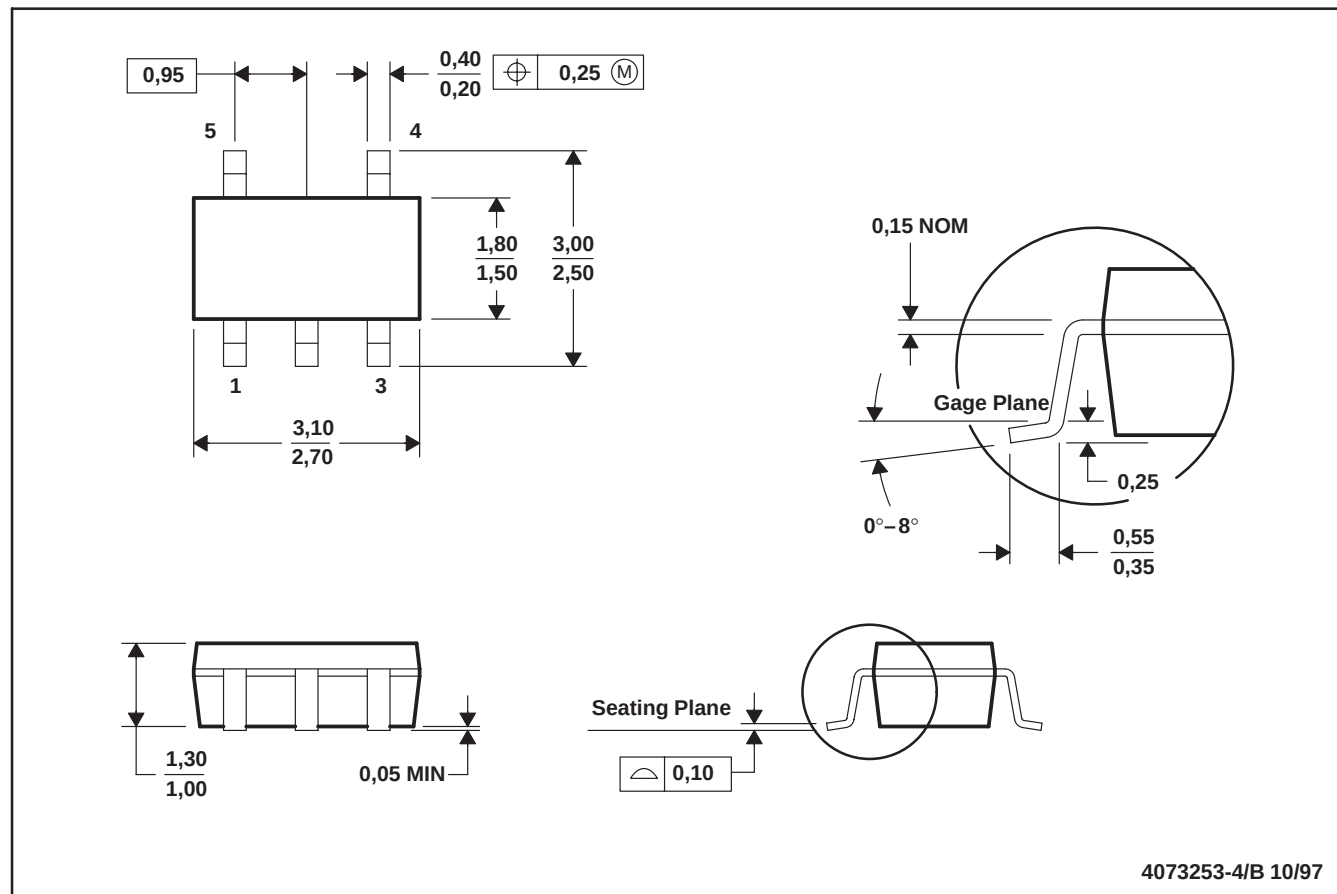
TLV2241, TLV2242, TLV2244
FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS

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MECHANICAL INFORMATION

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions include mold flash or protrusion.

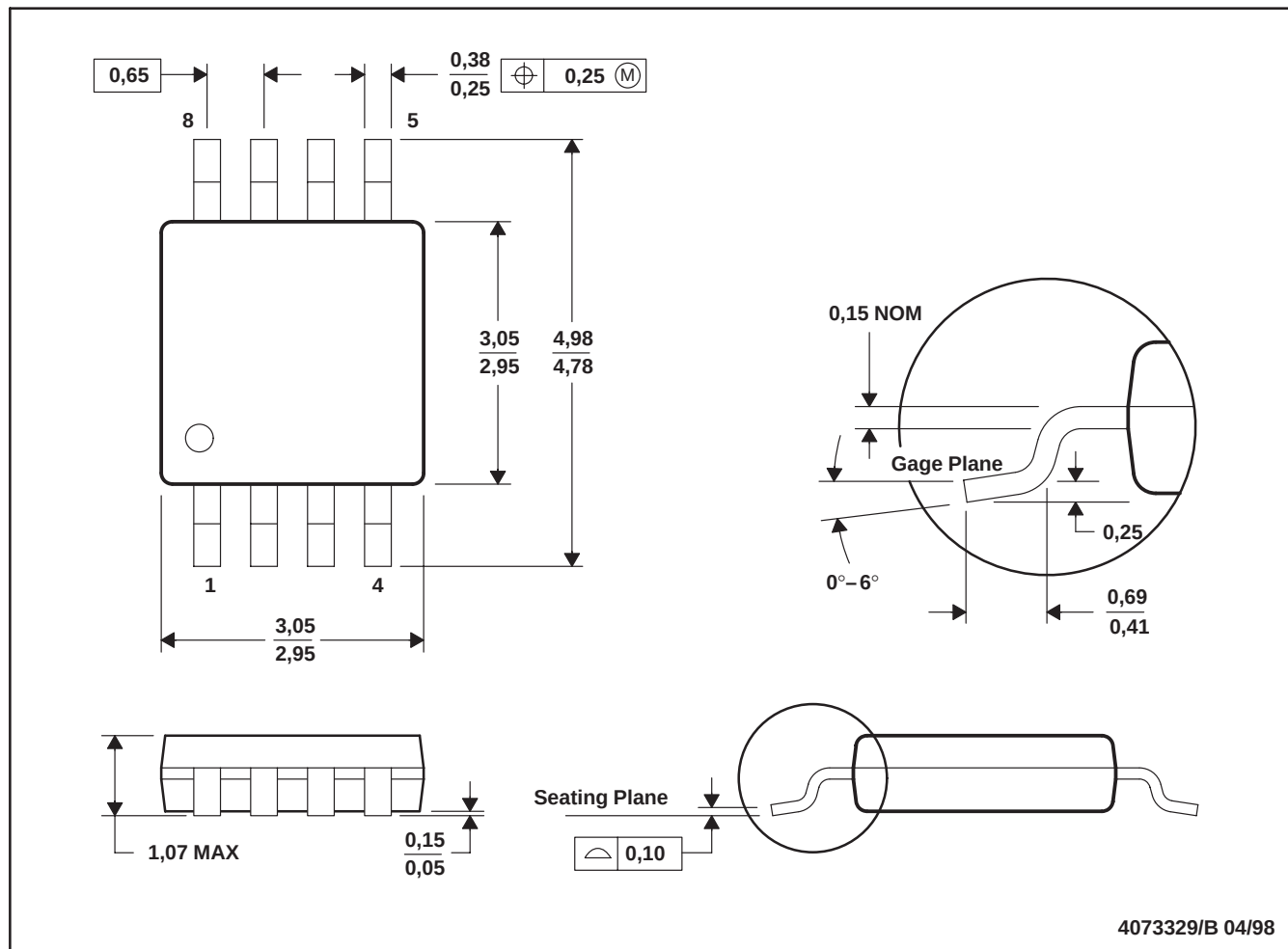
TLV2241, TLV2242, TLV2244
FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS

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MECHANICAL INFORMATION

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

TLV2241, TLV2242, TLV2244

FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT

OPERATIONAL AMPLIFIERS

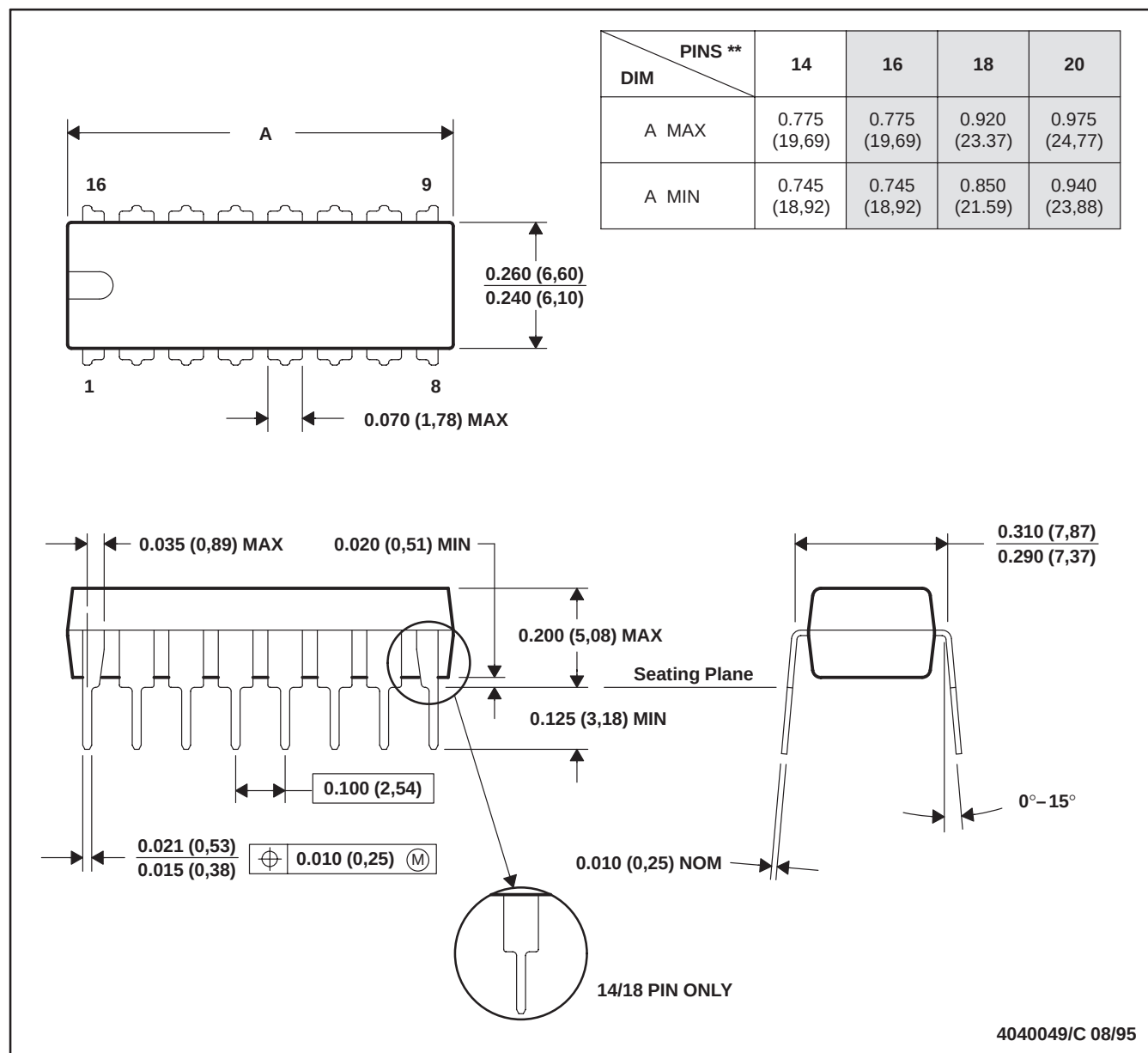
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MECHANICAL INFORMATION

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001 (20 pin package is shorter than MS-001.)

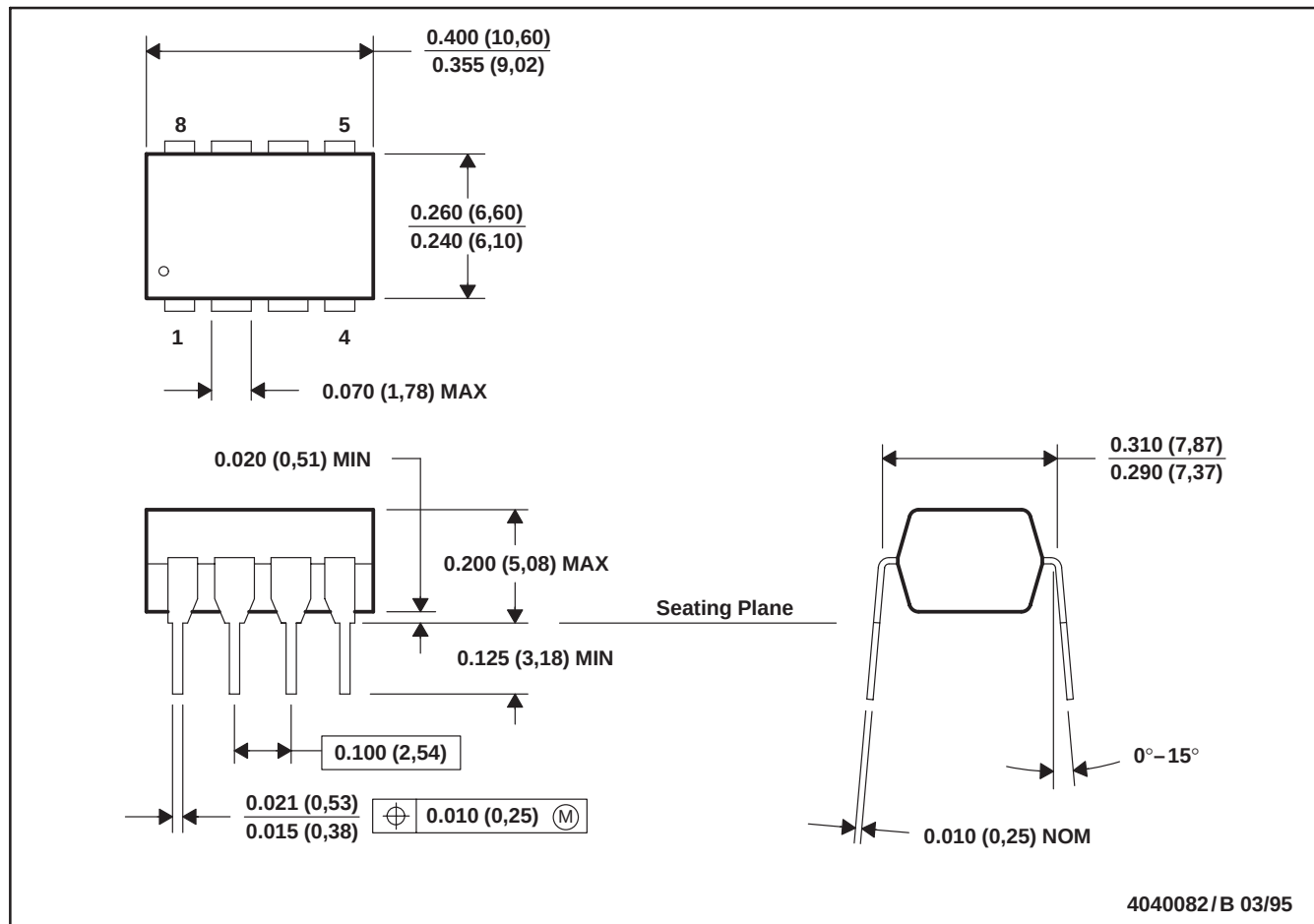
TLV2241, TLV2242, TLV2244
FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT
OPERATIONAL AMPLIFIERS

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MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

TLV2241, TLV2242, TLV2244

FAMILY OF 1- μ A/Ch RAIL-TO-RAIL INPUT/OUTPUT

OPERATIONAL AMPLIFIERS

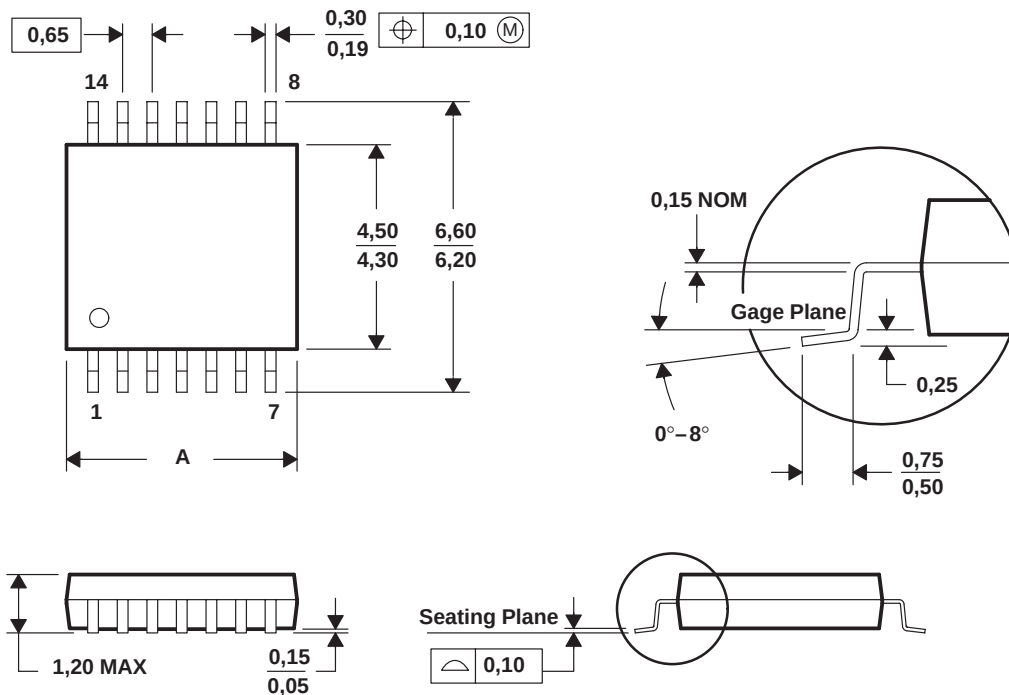
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MECHANICAL INFORMATION

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2241CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2241IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2241IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2242CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242IDGK	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242IDGKG4	ACTIVE	MSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2242IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2242IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2244CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TLV2244CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2244ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2244IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2244IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2244IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM
TLV2244IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2244INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLV2244IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2244IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2244IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLV2244IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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