

TLC225x-EP, TLC225xA-EP Advanced LinCMOS™ RAIL-TO-RAIL VERY LOW-POWER OPERATIONAL AMPLIFIERS

SGLS216 – NOVEMBER 2003

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of -40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 150 V (TLC2252/52A) and 100 V (TLC2254/54A) Using Machine Model (C = 200 pF, R = 0)**
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 19 nV/ $\sqrt{\text{Hz}}$ Typ at $f = 1 \text{ kHz}$**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Very Low Power . . . 35 μA Per Channel Typ**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
850 μV Max at $T_A = 25^{\circ}\text{C}$ (TLC225xA)
- **Macromodel Included**
- **Performance Upgrades for the TS27L2/L4 and TLC27L2/L4**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

description

The TLC2252 and TLC2254 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC225x family consumes only 35 μA of supply current per channel. This micropower operation makes them good choices for battery-powered applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Looking at Figure 1, the TLC225x has a noise level of 19 nV/ $\sqrt{\text{Hz}}$ at 1kHz; four times lower than competitive micropower solutions.

The TLC225x amplifiers, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC225xA family is available and has a maximum input offset voltage of 850 μV . This family is fully characterized at 5 V and $\pm 5 \text{ V}$.

EQUIVALENT INPUT NOISE VOLTAGE
VS
FREQUENCY

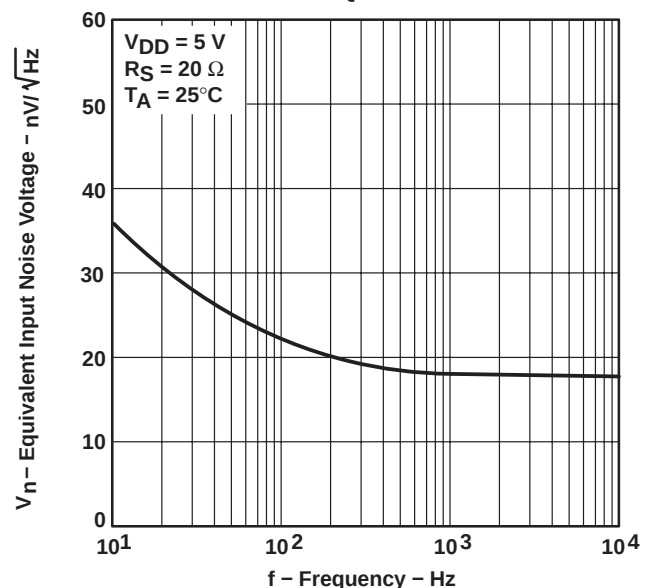


Figure 1



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description/ordering information (continued)

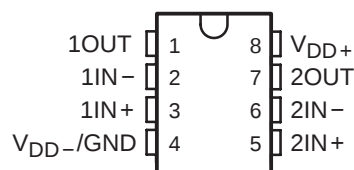
The TLC2252/4 also makes great upgrades to the TLC27L2/L4 or TS27L2/L4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage ranges, see the TLV2432 and TLV2442 devices. If the design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption, make them ideal for high density, battery-powered equipment.

ORDERING INFORMATION

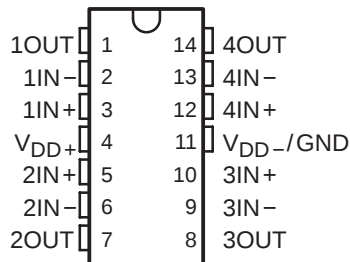
T _A	V _{IO} max AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	850 µV	SOIC (D)	Tape and reel	TLC2252AQDREP	2252AE
	1550 µV	SOIC (D)	Tape and reel	TLC2252QDREP	2252EP
	850 µV	SOIC (D)	Tape and reel	TLC2254AQDREP	TLC2254AEP
	1550 µV	SOIC (D)	Tape and reel	TLC2254QDREP	TLC2254EP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

TLC2252, TLC2252A
D PACKAGE
(TOP VIEW)



TLC2254, TLC2254A
D PACKAGE
(TOP VIEW)



The schematic diagram illustrates a 10-bit SAR ADC. It consists of three main functional blocks: a 10-bit DAC, a 10-bit comparator, and a 10-bit SAR logic block.

- 10-bit DAC:** The DAC is implemented using a current mirror and a resistor ladder. It features a 10-bit input (IN+) and a 10-bit output (OUT). The DAC is composed of 10 transistors (Q1-Q10) and 10 resistors (R1-R10). The input is connected to the gates of Q1-Q10, and the output is connected to the drains of Q1-Q10. The DAC is biased by VDD+ and VDD-/GND.
- 10-bit Comparator:** The comparator is implemented using a current mirror and a resistor ladder. It features a 10-bit input (IN-) and a 10-bit output (OUT). The comparator is composed of 10 transistors (Q11-Q20) and 10 resistors (R1-R10). The input is connected to the gates of Q11-Q20, and the output is connected to the drains of Q11-Q20. The comparator is biased by VDD+ and VDD-/GND.
- 10-bit SAR Logic:** The SAR logic block is implemented using a current mirror and a resistor ladder. It features a 10-bit input (IN+) and a 10-bit output (OUT). The SAR logic is composed of 10 transistors (Q21-Q30) and 10 resistors (R1-R10). The input is connected to the gates of Q21-Q30, and the output is connected to the drains of Q21-Q30. The SAR logic is biased by VDD+ and VDD-/GND.

The schematic diagram shows the internal structure of the 10-bit SAR ADC, including the 10-bit DAC, the 10-bit comparator, and the 10-bit SAR logic block. The circuit is biased by VDD+ and VDD-/GND. The input is connected to the gates of the transistors, and the output is connected to the drains of the transistors. The circuit is designed to convert a 10-bit digital input into a 10-bit analog output.

ACTUAL DEVICE COMPONENT COUNT [†]		
COMPONENT	TLC2252	TLC2254
Transistors	38	76
Resistors	30	56
Diodes	9	18
Capacitors	3	6

[†] Includes both amplifiers and all ESD, bias, and trim circuitry

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	–8 V
Differential input voltage, V_{ID} (see Note 2)	±16 V
Input voltage, V_I (any input, see Note 1)	±8 V
Input current, I_I (each input)	±5 mA
Output current, I_O	±50 mA
Total current into V_{DD+}	±50 mA
Total current out of V_{DD-}	±50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : Q suffix	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current flows when input is brought below $V_{DD-} - 0.3$ V.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D–8	724 mW	5.8 mW/°C	464 mW	377 mW	144 mW
D–14	950 mW	7.6 mW/°C	608 mW	450 mW	190 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	±2.2	±8	V
Input voltage range, V_I	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	–40	125	°C

[‡] Referenced to 2.5 V



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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252-EP			TLC2252A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} \pm \pm 2.5\text{ V}, V_{IC} = 0, V_O = 0, R_S = 50\ \Omega$	25°C		200	1500		200	850	μV
		Full range			1750			1000	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C		0.5			0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		Full range			1000			1000	
I_{IB} Input bias current		25°C		1	60		1	60	pA
		Full range			1000			1000	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98			4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		4.9	4.94		4.9	4.94	
		Full range		4.8			4.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		4.8	4.88		4.8	4.88	
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15		0.09	0.15	
		Full range			0.15			0.15	
	$V_{IC} = 2.5\text{ V}, I_{OL} = 4\text{ mA}$	25°C		0.8	1		0.7	1	
		Full range			1.2			1.2	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350		100	350	V/mV
			Full range	10			10		
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		1700			1700	
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic} Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic} Common-mode input capacitance	$f = 10\text{ kHz}, f = 10\text{ kHz},$	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}, A_V = 10$	25°C		200			200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C		70	83		70	83	dB
		Full range		70			70		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C		80	95		80	95	dB
		Full range		80			80		
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C		70	125		70	125	μA
		Full range			150			150	

† Full range is -40°C to 125°C for Q suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC2252-EP			TLC2252A-EP			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 0.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$		25°C	0.07	0.12		0.07	0.12		V/ μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		36			36		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		0.7			0.7		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 10\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger$	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$, $C_L = 100\text{ pF}^\ddagger$	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$	$C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is -40°C to 125°C for Q suffix.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2252-EP			TLC2252A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, V_O = 0, R_S = 50 \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu V/mo$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		Full range		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		Full range		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50 \Omega, V_{IO} \leq 5$ mV	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2		V
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \mu A$	25°C		4.98			4.98		V
	$I_O = -100 \mu A$	25°C	4.9	4.93		4.9	4.93		
		Full range	4.7			4.7			
	$I_O = -200 \mu A$	25°C	4.8	4.86		4.8	4.86		
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, I_O = 50 \mu A$	25°C		-4.99			-4.99		V
		25°C	-4.85	-4.91		-4.85	-4.91		
	$V_{IC} = 0, I_O = 500 \mu A$	Full range	-4.85			-4.85			
		25°C	-4	-4.3		-4	-4.3		
	$V_{IC} = 0, I_O = 4$ mA	Full range	-3.8			-3.8			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4$ V	$R_L = 100$ k Ω	25°C	40	150	40	150		V/mV
			Full range	10		10			
		$R_L = 1$ M Ω	25°C	3000		3000			
r_{id} Differential input resistance		25°C		10^{12}			10^{12}		Ω
r_{ic} Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
c_{ic} Common-mode input capacitance	f = 10 kHz, P package	25°C		8			8		pF
z_o Closed-loop output impedance	f = 25 kHz, $A_V = 10$	25°C		190			190		Ω
CMRR Common-mode rejection ratio	$V_{IC} = -5$ V to 2.7 V, $V_O = 0, R_S = 50 \Omega$	25°C	75	88		75	88		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm} / \Delta V_{IO}$)	$V_{DD} = \pm 2.2$ V to ± 8 V, $V_{IC} = 0$, No load	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5$ V, No load	25°C	80	125		80	125		μA
		Full range		150			150		

† Full range is -40°C to 125°C for Q suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS	$T_A^\dagger$	TLC2252-EP			TLC2252A-EP			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = \pm 2\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 100\text{ k}\Omega$	25°C	0.07	0.12		0.07	0.12		V/ μs
			Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		38			38		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$	25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		0.8			0.8		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.1			1.1		
I_n	Equivalent input noise current		25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $R_L = 50\text{ k}\Omega$, $f = 10\text{ kHz}$	25°C		0.2%			0.2%		
		$A_V = 1$ $A_V = 10$			1%			1%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$, $R_L = 50\text{ k}\Omega$	25°C		0.21			0.21		MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = 1$	25°C		14			14		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		63°			63°		
	Gain margin		25°C		15			15		dB

† Full range is -40°C to 125°C for Q suffix.

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electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254-EP			TLC2254A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{DD} = \pm 2.5\text{ V}$, $V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	25°C		200	1500		200	850	μV
		Full range			1750			1000	
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C		0.5			0.5		$\mu\text{V}/^\circ\text{C}$
Input offset voltage long-term drift (see Note 4)		25°C		0.003			0.003		$\mu\text{V}/\text{mo}$
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		125°C			1000			1000	
I_{IB} Input bias current		25°C		1	60		1	60	pA
		125°C			1000			1000	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$, $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.98			4.98		V
	$I_{OH} = -75\ \mu\text{A}$	25°C		4.9	4.94		4.9	4.94	
		Full range		4.8			4.8		
	$I_{OH} = -150\ \mu\text{A}$	25°C		4.8	4.88		4.8	4.88	
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01		V
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C		0.09	0.15		0.09	0.15	
		Full range			0.15			0.15	
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 4\text{ mA}$	25°C		0.8	1		0.7	1	
		Full range			1.2			1.2	
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$	$R_L = 100\text{ k}\Omega^\ddagger$	25°C	100	350		100	350	V/mV
		$R_L = 1\text{ M}\Omega^\ddagger$	25°C		1700			1700	
			Full range	10			10		
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25\text{ kHz}$, $A_V = 10$	25°C		200			200		Ω
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C		70	83		70	83	dB
		Full range		70			70		
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C		80	95		80	95	dB
		Full range		80			80		
I_{DD} Supply current (four amplifiers)	$V_O = 2.5\text{ V}$, No load	25°C		140	250		140	250	μA
		Full range			300			300	

† Full range is -40°C to 125°C for Q suffix.

‡ Referenced to 2.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		$T_A^\dagger$	TLC2254-EP			TLC2254A-EP			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$V_O = 0.5\text{ V to }3.5\text{ V}$, $R_L = 100\text{ k}\Omega^\ddagger$, $C_L = 100\text{ pF}^\ddagger$		25°C	0.07	0.12		0.07	0.12		V/ μs
				Full range	0.05			0.05			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		25°C		36			36		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		25°C		19			19		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		25°C		0.7			0.7		μV
		$f = 0.1\text{ Hz to }10\text{ Hz}$		25°C		1.1			1.1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$	25°C		0.2%			0.2%		
			$A_V = 10$			1%			1%		
	Gain-bandwidth product	$f = 50\text{ kHz}$, $C_L = 100\text{ pF}^\ddagger$	$R_L = 50\text{ k}\Omega^\ddagger$	25°C		0.2			0.2		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 50\text{ k}\Omega^\ddagger$	$A_V = 1$, $C_L = 100\text{ pF}^\ddagger$	25°C		30			30		kHz
ϕ_m	Phase margin at unity gain	$R_L = 50\text{ k}\Omega^\ddagger$	$C_L = 100\text{ pF}^\ddagger$	25°C		63°			63°		
	Gain margin			25°C		15			15		dB

† Full range is -40°C to 125°C for Q suffix.

‡ Referenced to 2.5 V

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electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^\dagger$	TLC2254-EP			TLC2254A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0, \quad V_O = 0, \quad R_S = 50 \, \Omega$	25°C	200	1500		200	850		μV
		Full range		1750			1000		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	0.5			0.5			$\mu V/^\circ C$
Input offset voltage long-term drift (see Note 4)		25°C	0.003			0.003			$\mu V/mo$
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA
		125°C		1000			1000		
I_{IB} Input bias current		25°C	1	60		1	60		pA
		125°C		1000			1000		
V_{ICR} Common-mode input voltage range	$R_S = 50 \, \Omega, \quad V_{IO} \leq 5 \, mV$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2		V
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20 \, \mu A$	25°C		4.98			4.98		V
	$I_O = -100 \, \mu A$	25°C	4.9	4.93		4.9	4.93		
		Full range	4.7			4.7			
	$I_O = -200 \, \mu A$	25°C	4.8	4.86		4.8	4.86		
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0, \quad I_O = 50 \, \mu A$	25°C		-4.99			-4.99		V
	$V_{IC} = 0, \quad I_O = 500 \, \mu A$	25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
	$V_{IC} = 0, \quad I_O = 4 \, mA$	25°C	-4	-4.3		-4	-4.3		
		Full range	-3.8			-3.8			
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4 \, V$	$R_L = 100 \, k\Omega$	25°C	40	150	40	150		V/mV
			Full range	10		10			
		$R_L = 1 \, M\Omega$	25°C	3000		3000			
$r_{i(d)}$ Differential input resistance		25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$ Common-mode input resistance		25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$ Common-mode input capacitance	$f = 10 \, kHz, \quad N$ package	25°C		8			8		pF
z_o Closed-loop output impedance	$f = 25 \, kHz, \quad A_V = 10$	25°C		190			190		Ω
$CMRR$ Common-mode rejection ratio	$V_{IC} = -5 \, V$ to $2.7 \, V, \quad V_O = 0, \quad R_S = 50 \, \Omega$	25°C	75	88		75	88		dB
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2 \, V$ to $\pm 8 \, V, \quad V_{IC} = V_{DD}/2, \quad \text{No load}$	25°C	80	95		80	95		dB
		Full range	80			80			
I_{DD} Supply current (four amplifiers)	$V_O = 0, \quad \text{No load}$	25°C	160	250		160	250		μA
		Full range		300			300		

† Full range is -40°C to 125°C for Q suffix.

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at $T_A = 150^\circ C$ extrapolated to $T_A = 25^\circ C$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



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operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A [†]	TLC2254-EP			TLC2254A-EP			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V _O = ±2 V, C _L = 100 pF	R _L = 100 kΩ,	25°C	0.07	0.12		0.07	0.12		V/μs
				Full range	0.05			0.05			
V _n	Equivalent input noise voltage	f = 10 Hz		25°C	38			38			nV/√Hz
		f = 1 kHz		25°C	19			19			
V _{N(PP)}	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C	0.8			0.8			μV
		f = 0.1 Hz to 10 Hz		25°C	1.1			1.1			
I _n	Equivalent input noise current			25°C	0.6			0.6			fA/√Hz
THD + N	Total harmonic distortion plus noise	V _O = ±2.3 V, R _L = 50 kΩ, f = 20 kHz	A _V = 1	25°C	0.2%			0.2%			
			A _V = 10		1%			1%			
	Gain-bandwidth product	f = 10 kHz, C _L = 100 pF	R _L = 50 kΩ,	25°C	0.21			0.21			MHz
B _{OM}	Maximum output-swing bandwidth	V _{O(PP)} = 4.6 V, R _L = 50 kΩ,	A _V = 1, C _L = 100 pF	25°C	14			14			kHz
φ _m	Phase margin at unity gain	R _L = 50 kΩ,	C _L = 100 pF	25°C	63°			63°			
	Gain margin			25°C	15			15			dB

† Full range is -40°C to 125°C for Q suffix.

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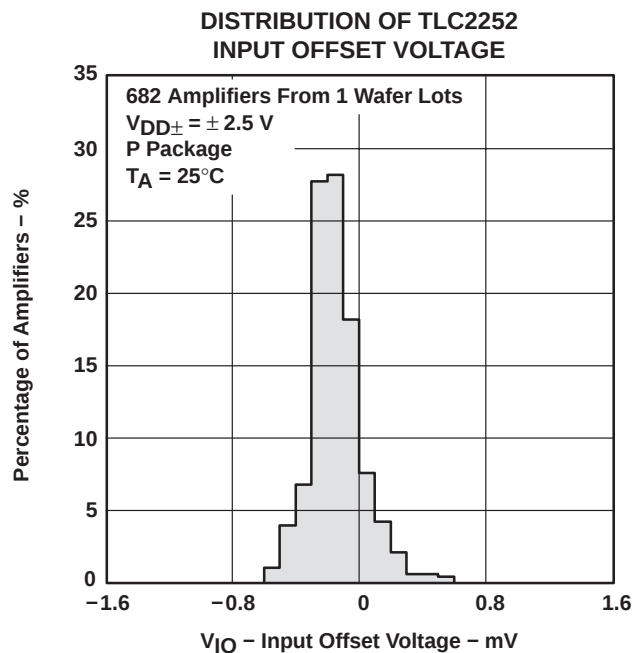


Figure 2

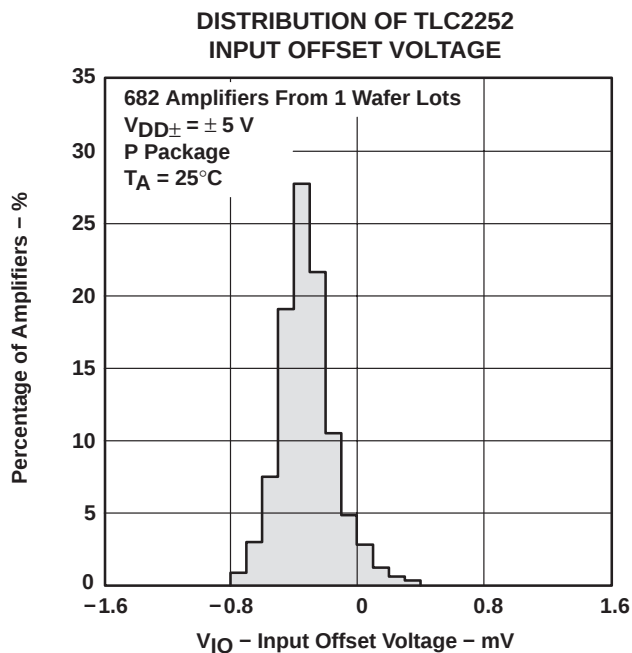


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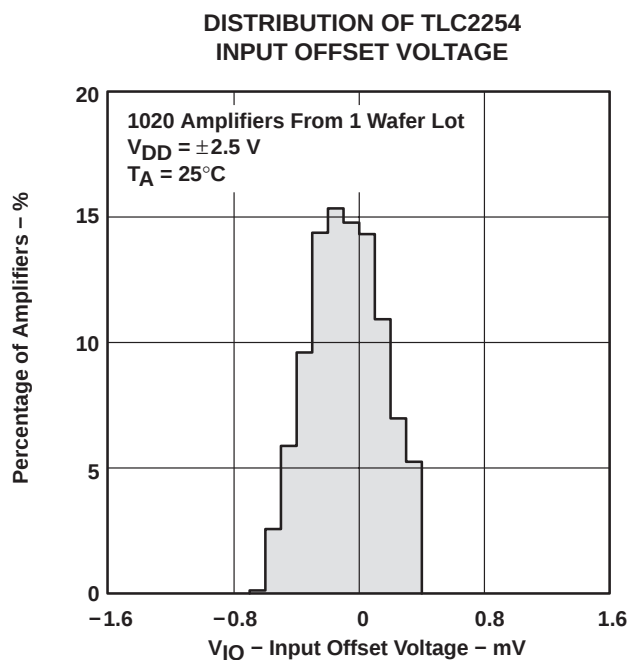


Figure 4

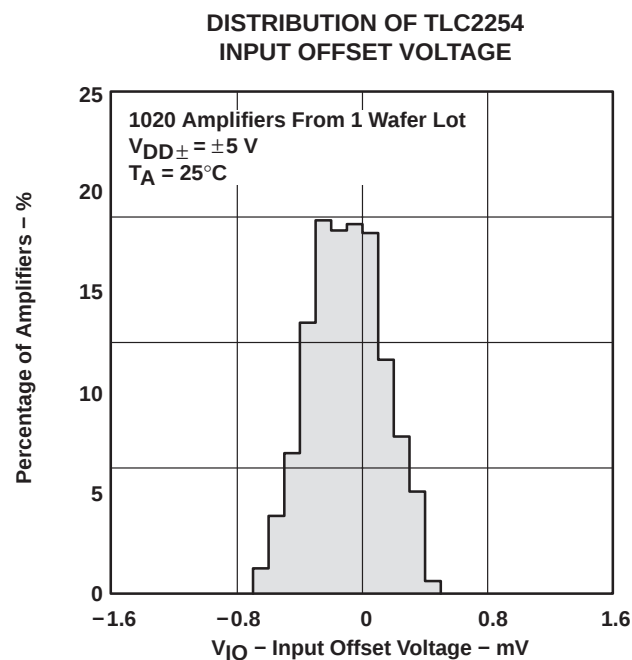


Figure 5

TYPICAL CHARACTERISTICS

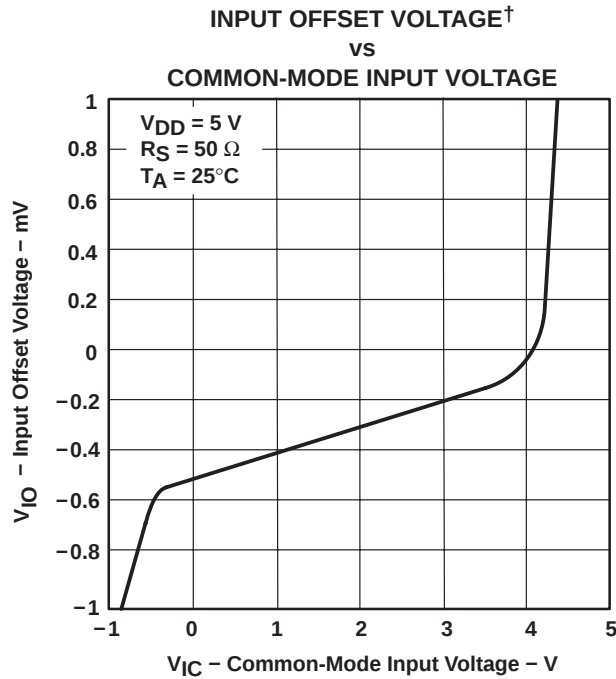


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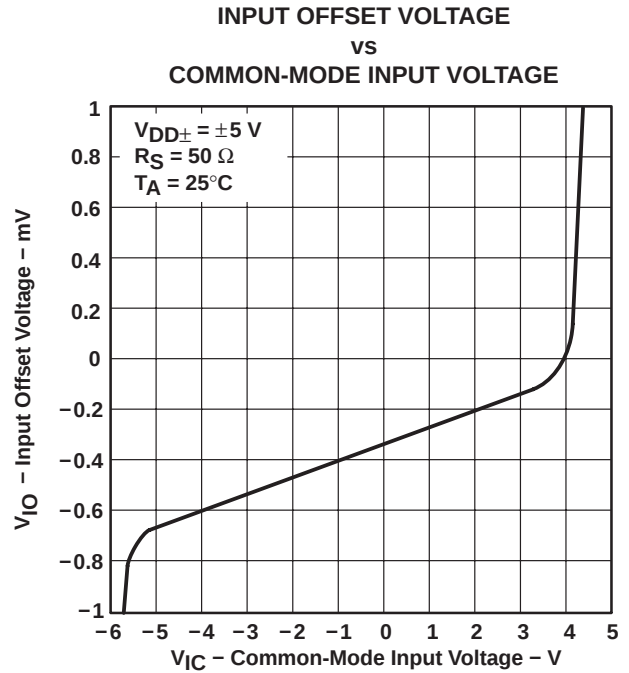


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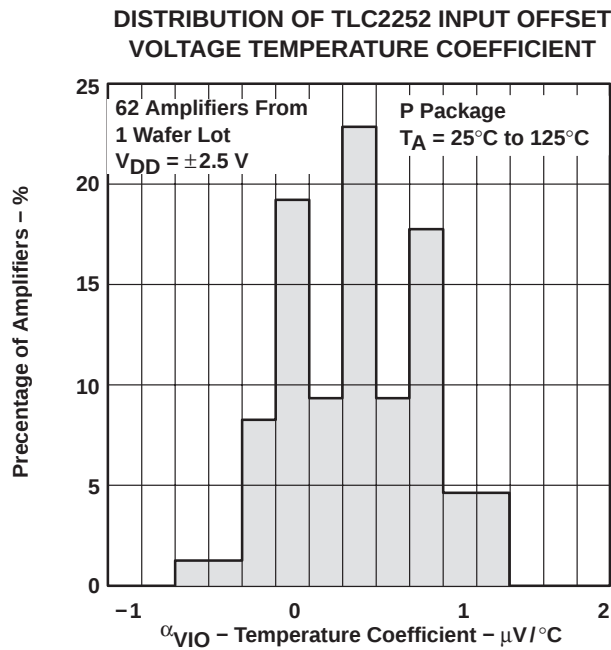


Figure 8

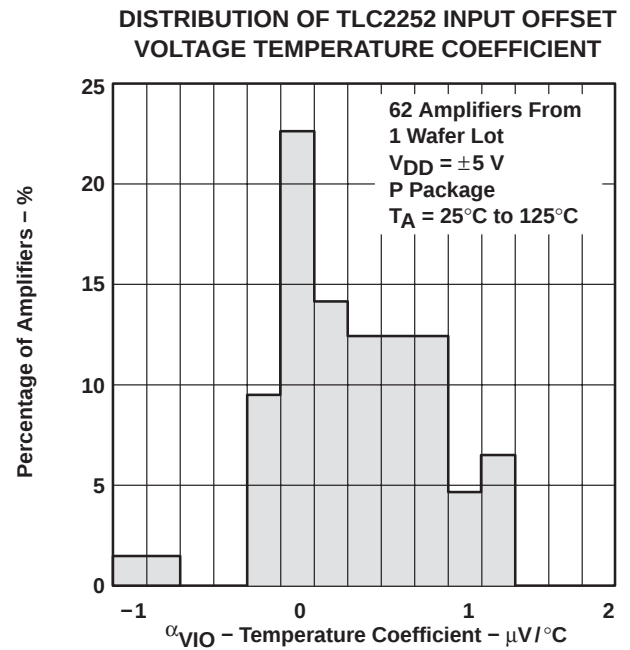


Figure 9

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

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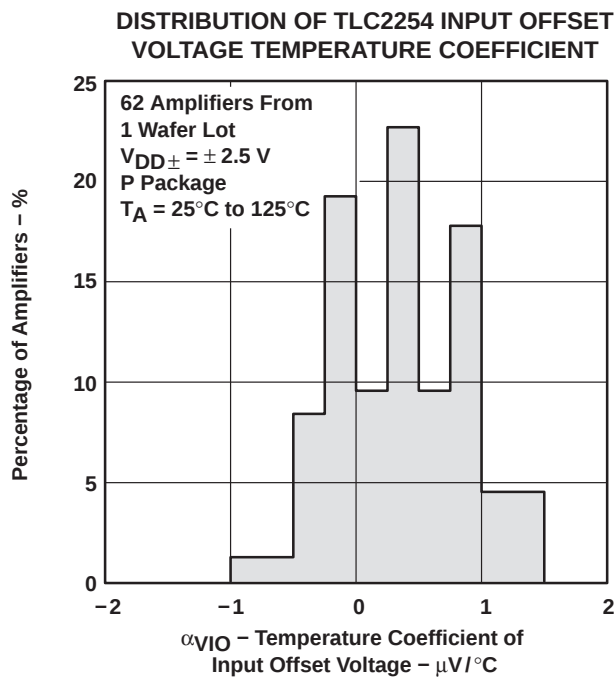


Figure 10

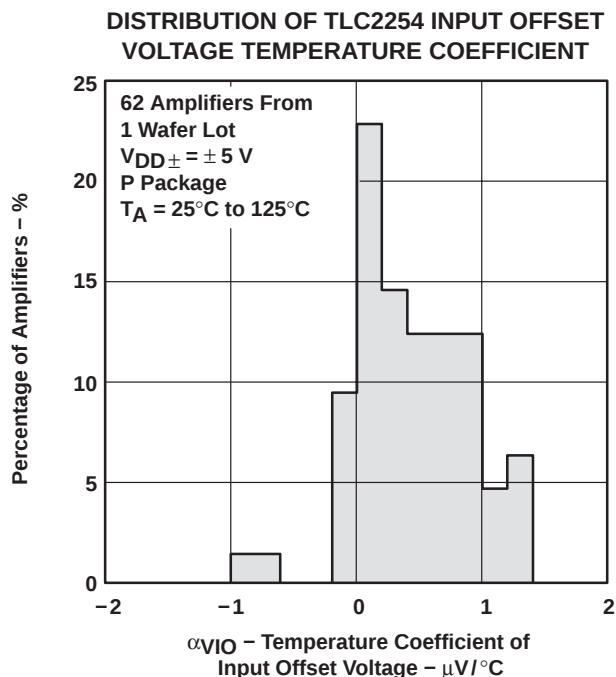


Figure 11

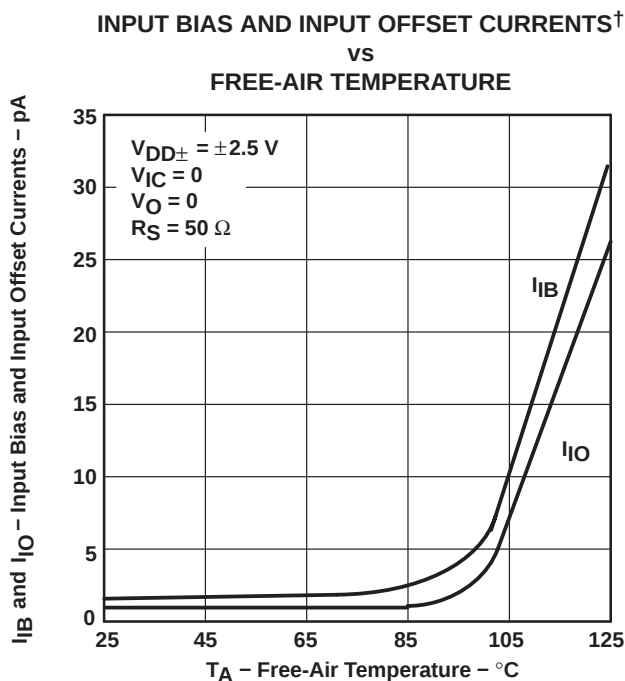


Figure 12

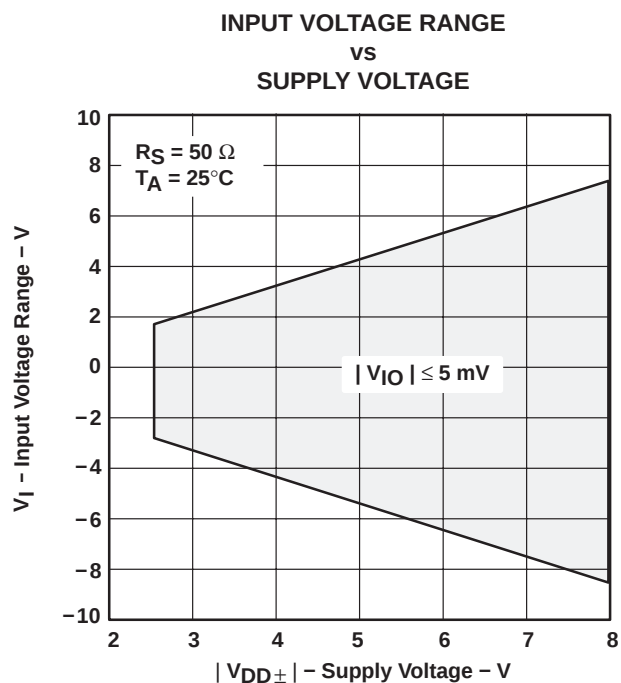
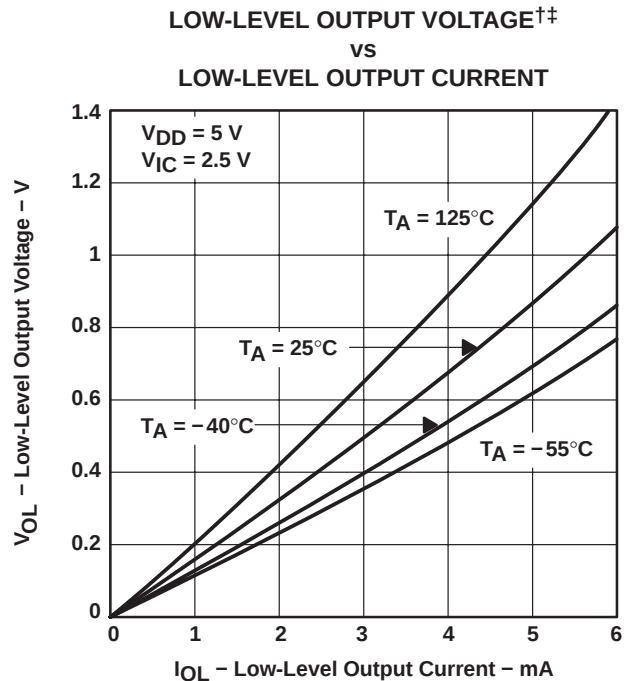
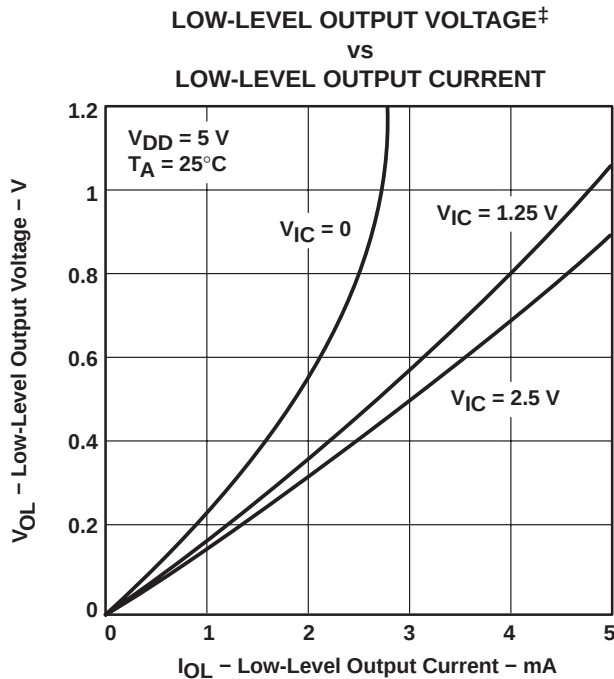
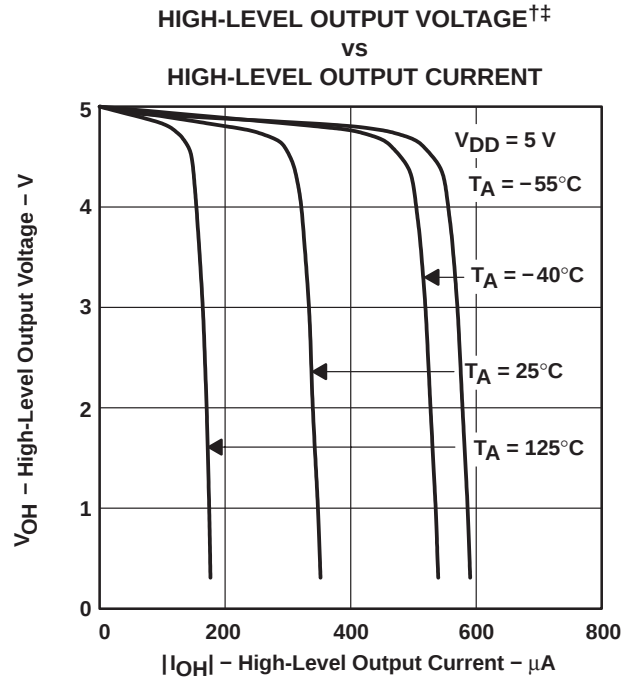
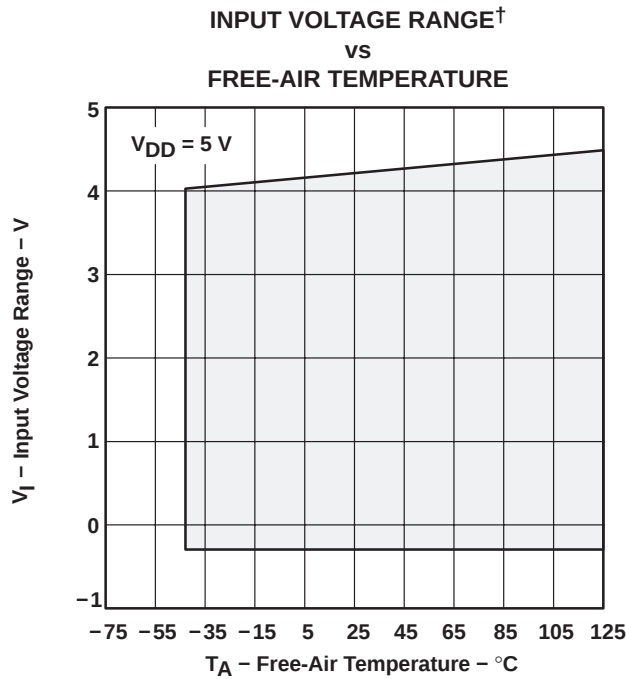


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

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TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE[†]
VS
OUTPUT CURRENT

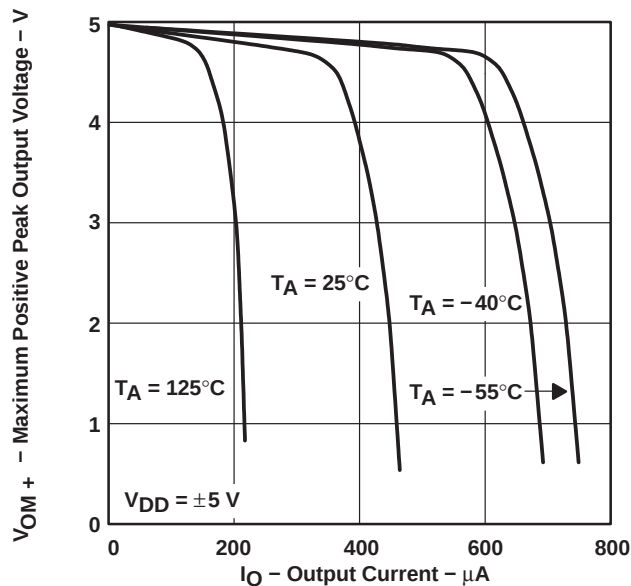


Figure 18

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE[†]
VS
OUTPUT CURRENT

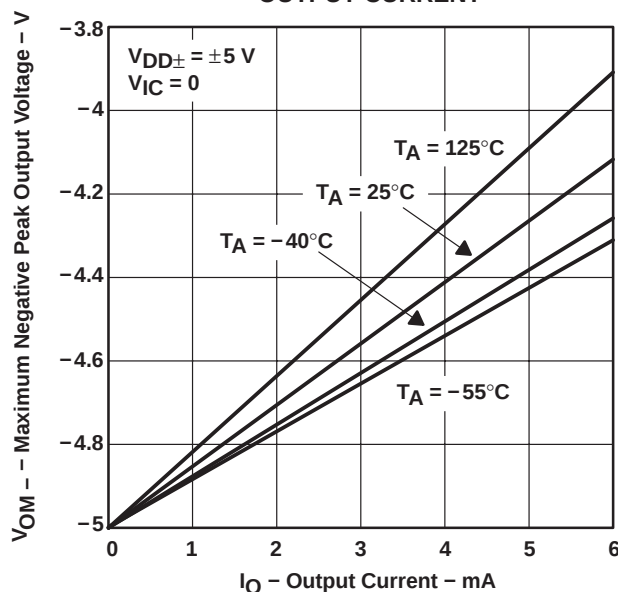


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE[‡]
VS
FREQUENCY

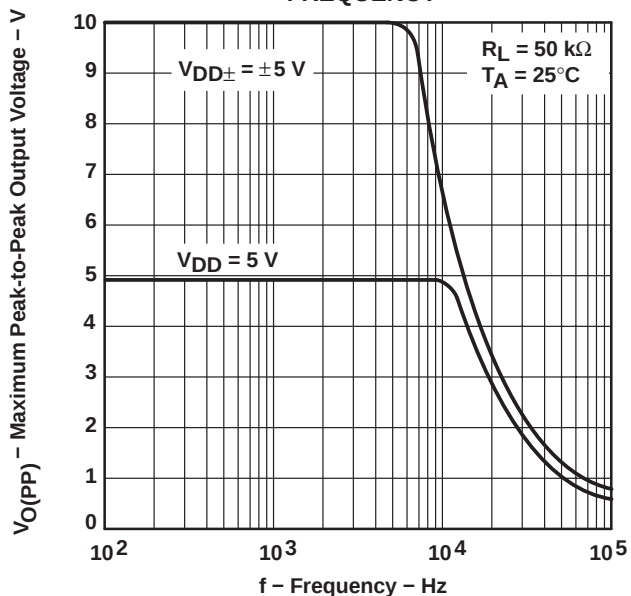


Figure 20

SHORT-CIRCUIT OUTPUT CURRENT
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SUPPLY VOLTAGE

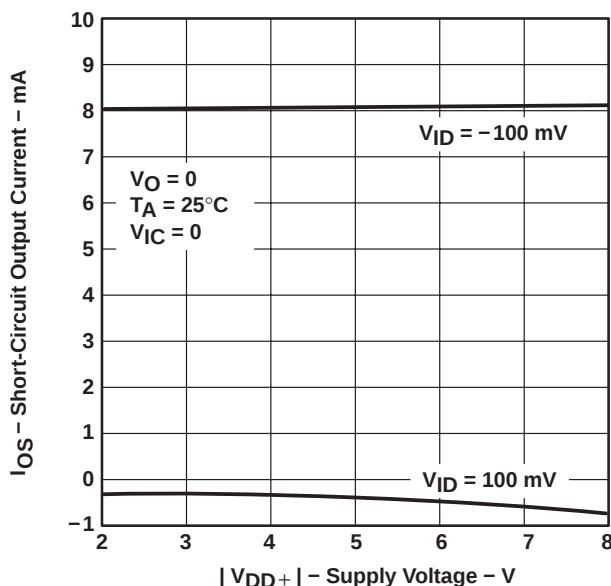
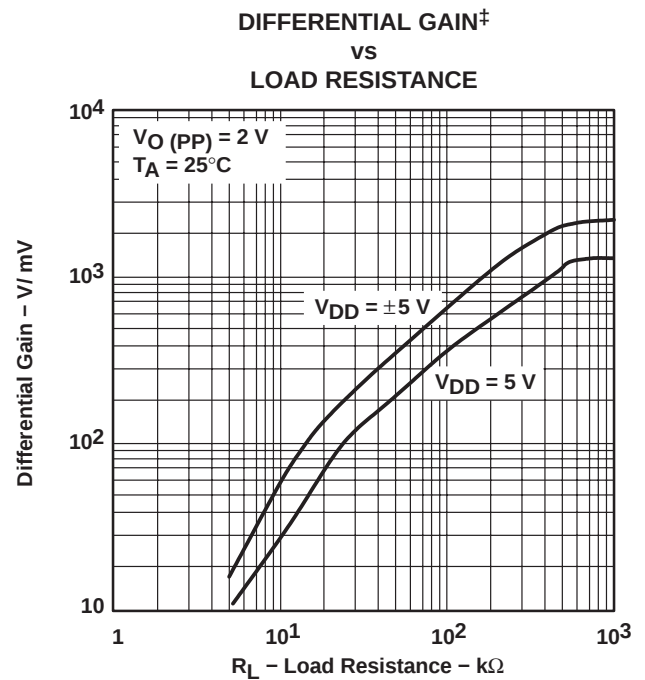
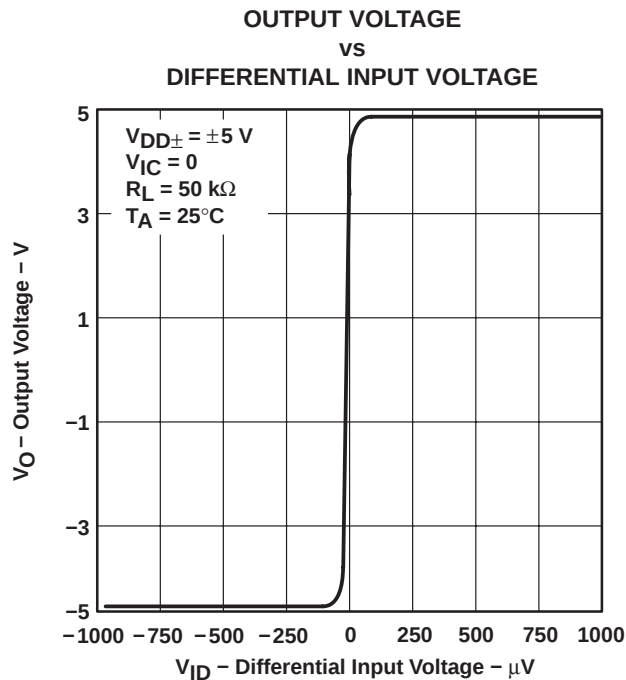
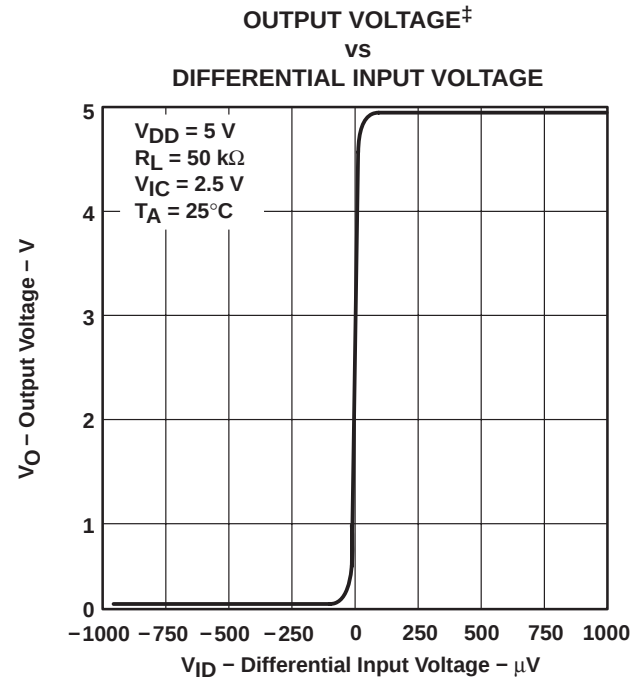
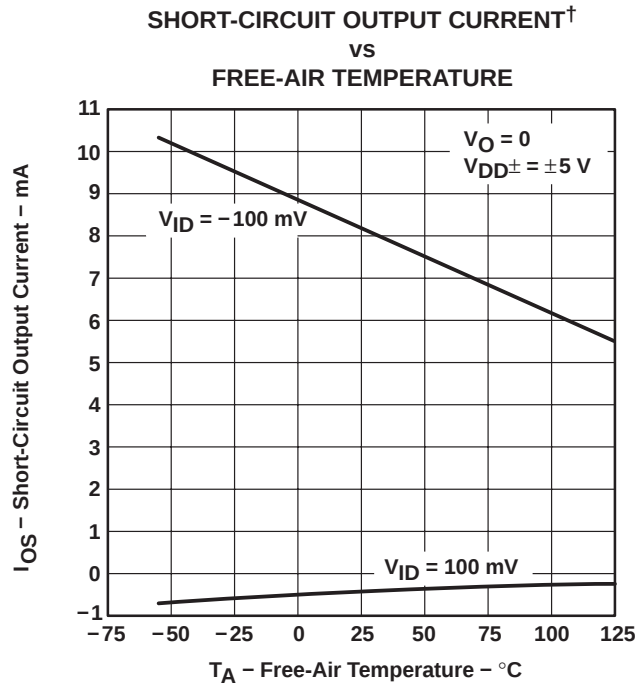


Figure 21

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

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TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN†**

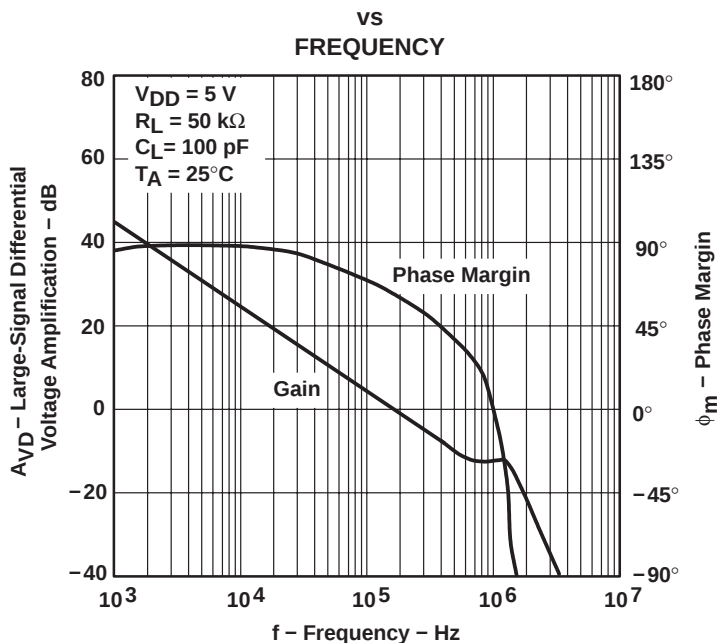


Figure 26

**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN**

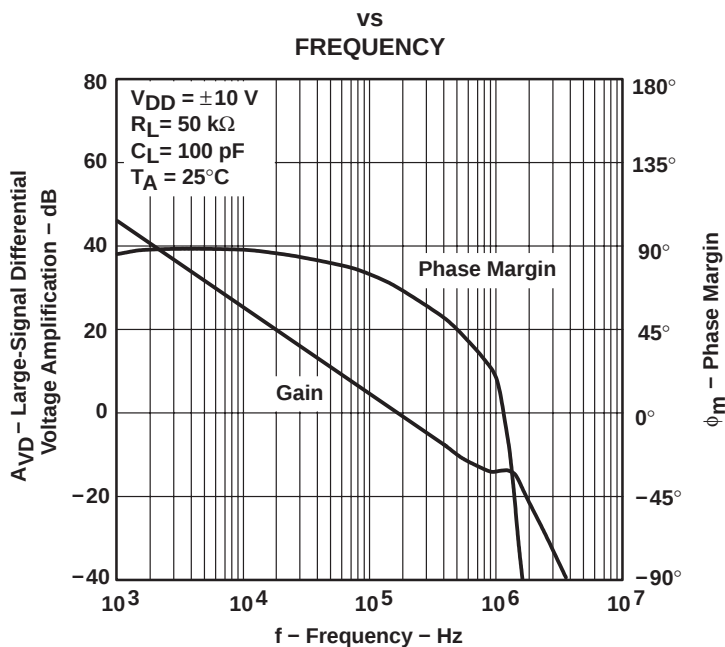
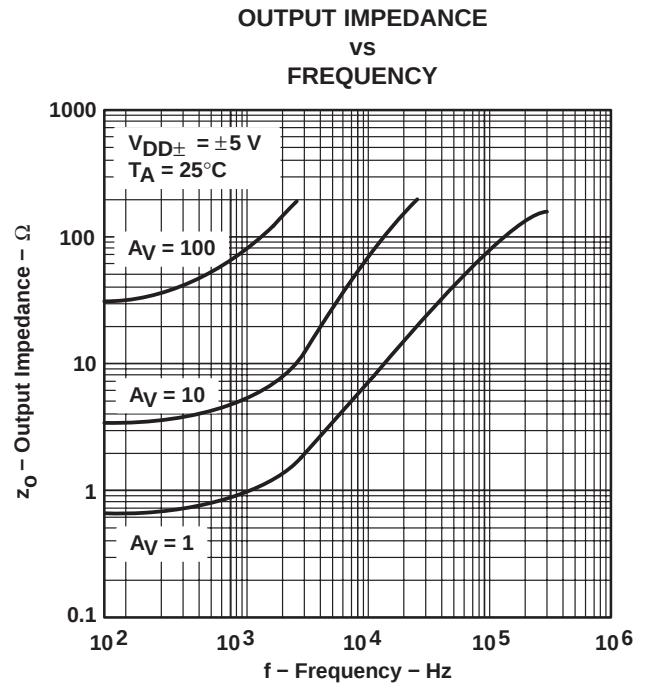
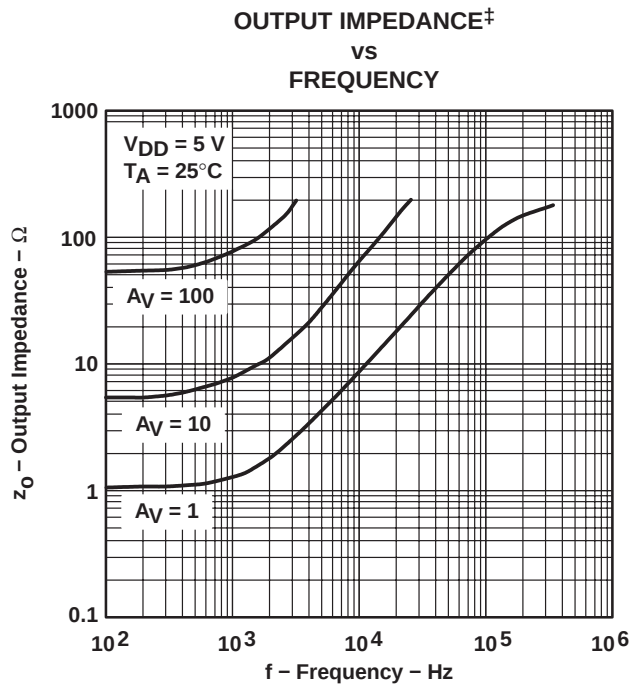
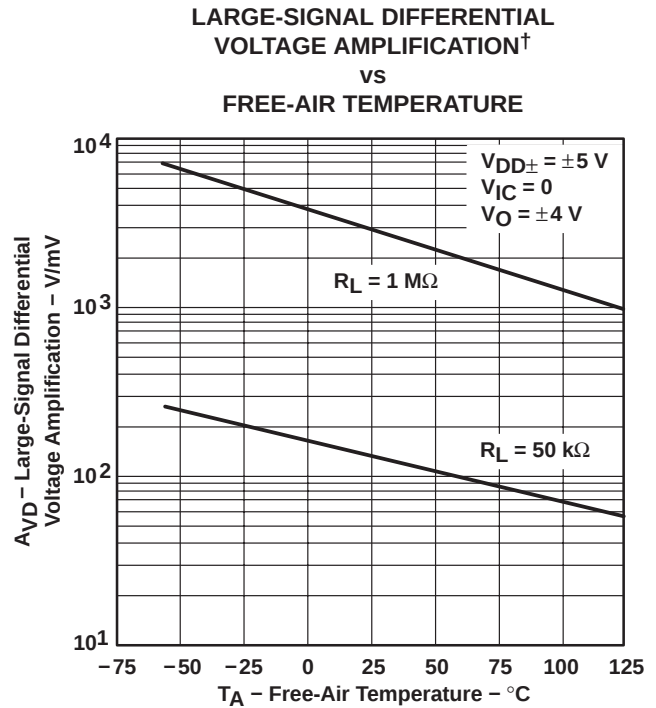
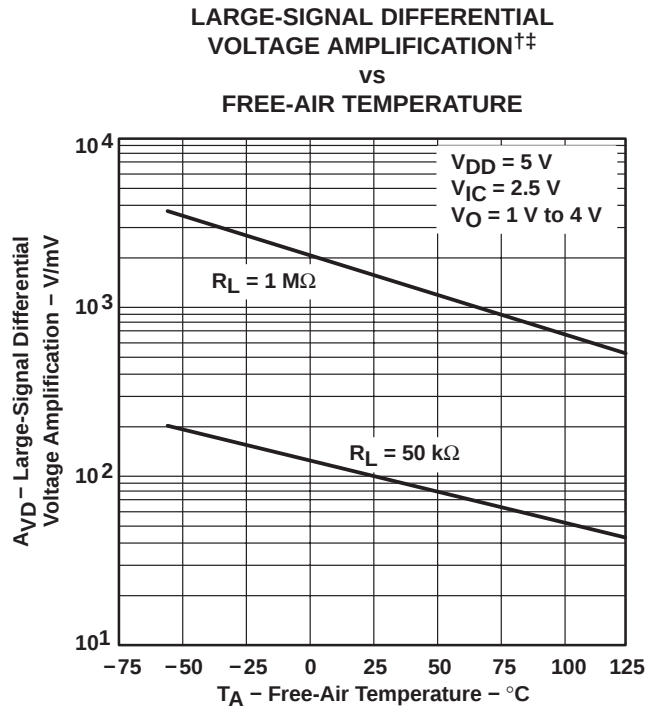


Figure 27

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

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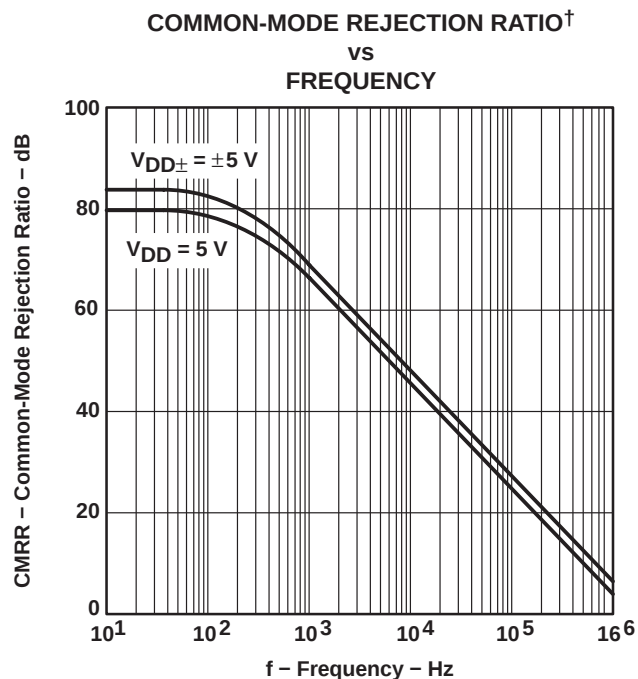


Figure 32

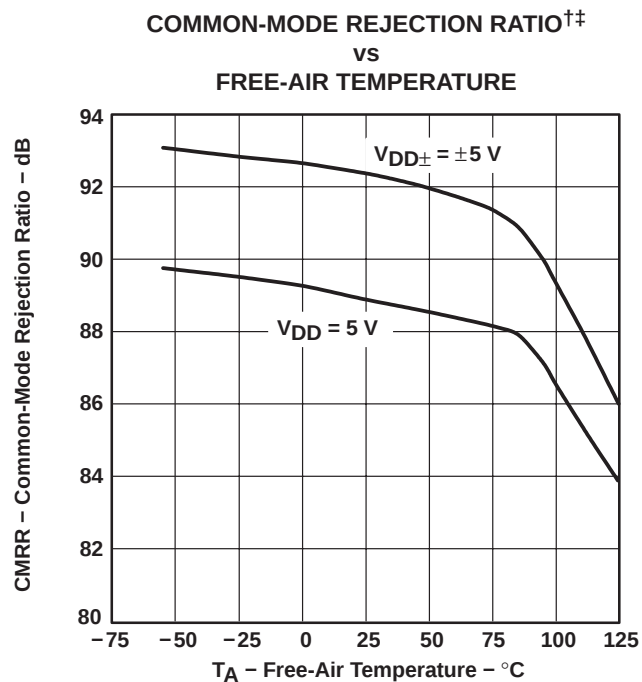


Figure 33

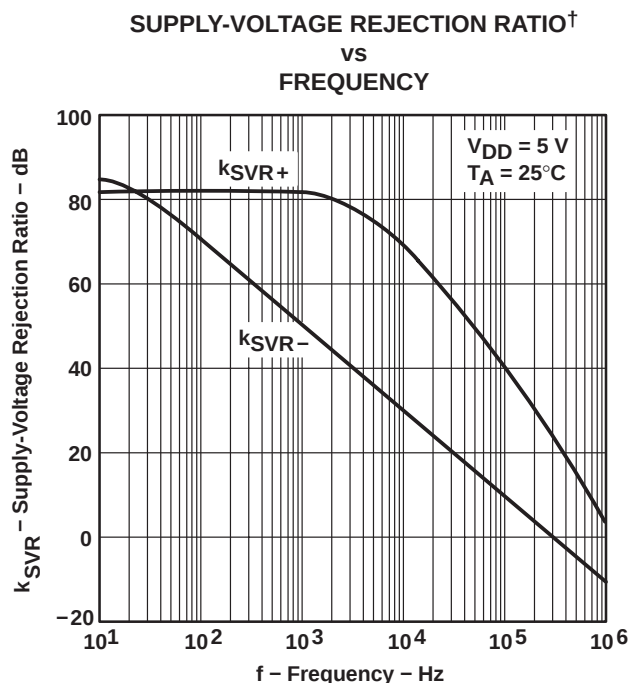


Figure 34

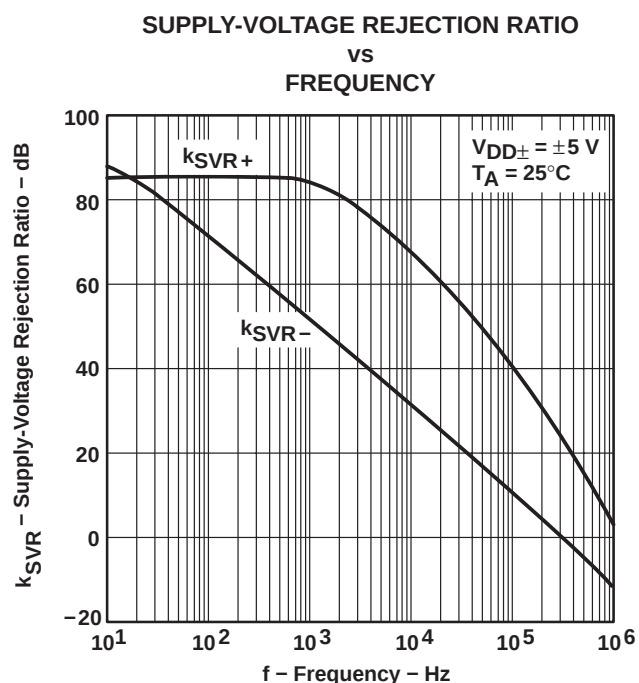


Figure 35

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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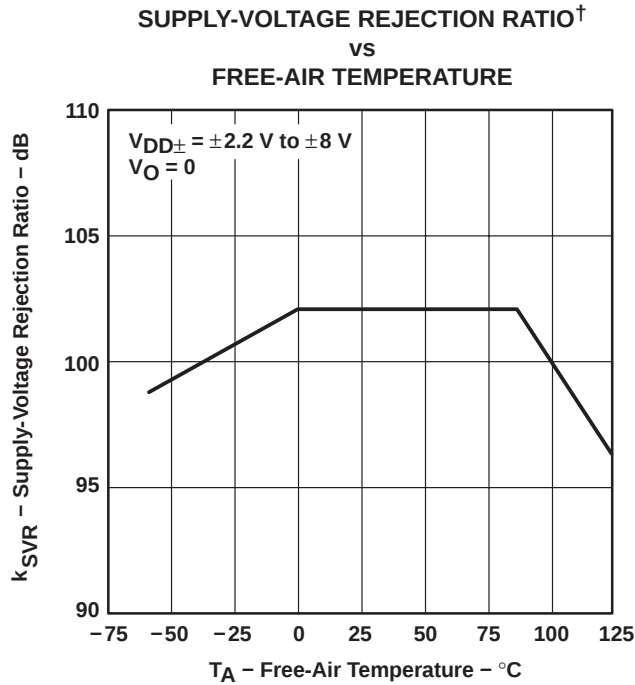


Figure 36

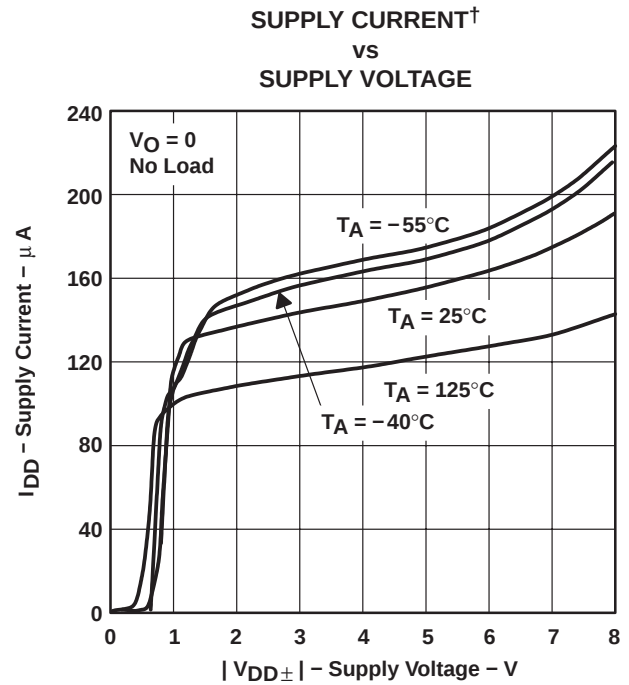


Figure 37

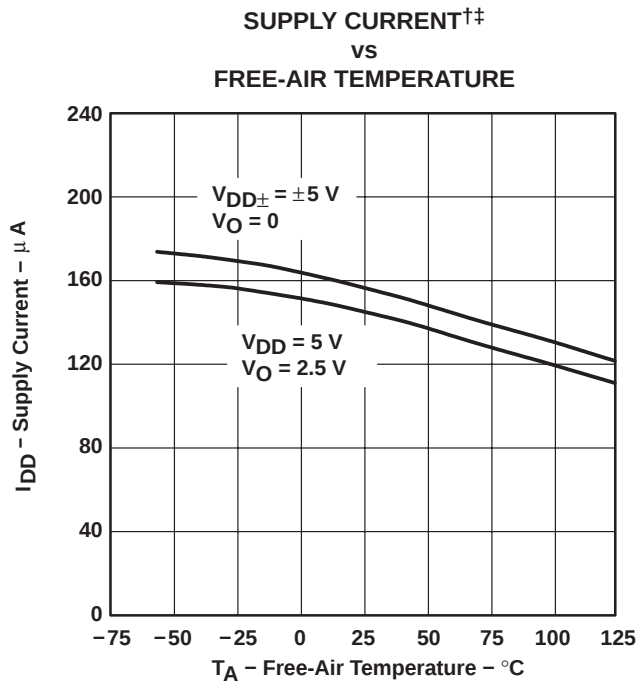


Figure 38

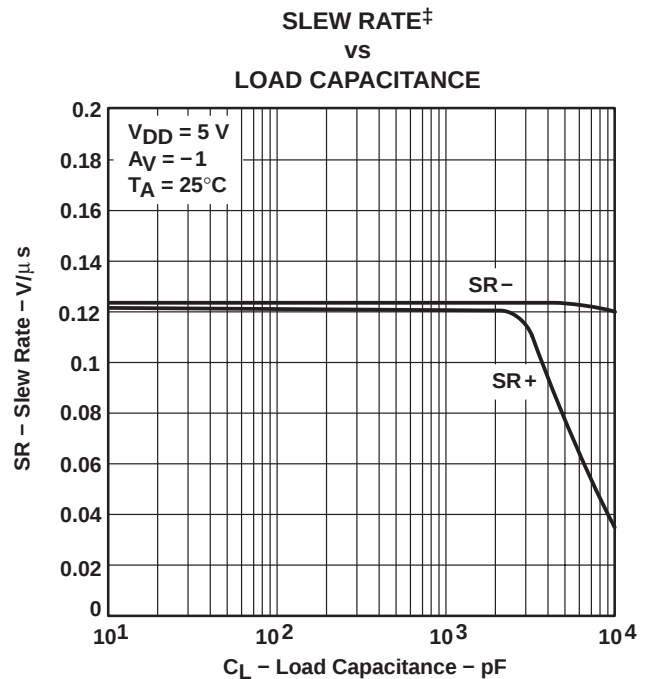


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

‡ For curves where $V_{DD} = 5$ V, all loads are referenced to 2.5 V.

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TYPICAL CHARACTERISTICS

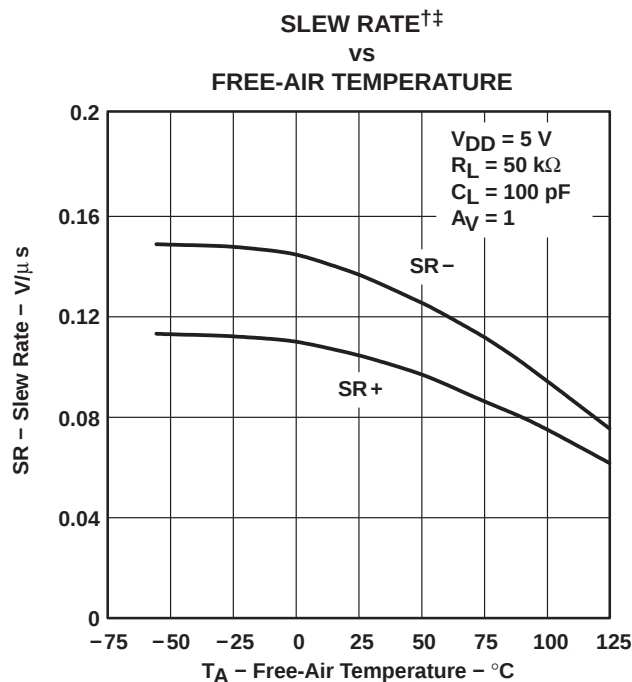


Figure 40

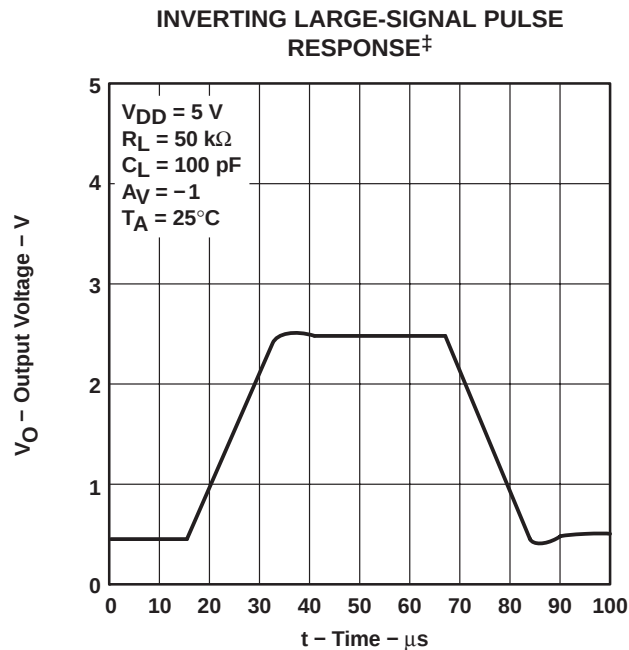


Figure 41

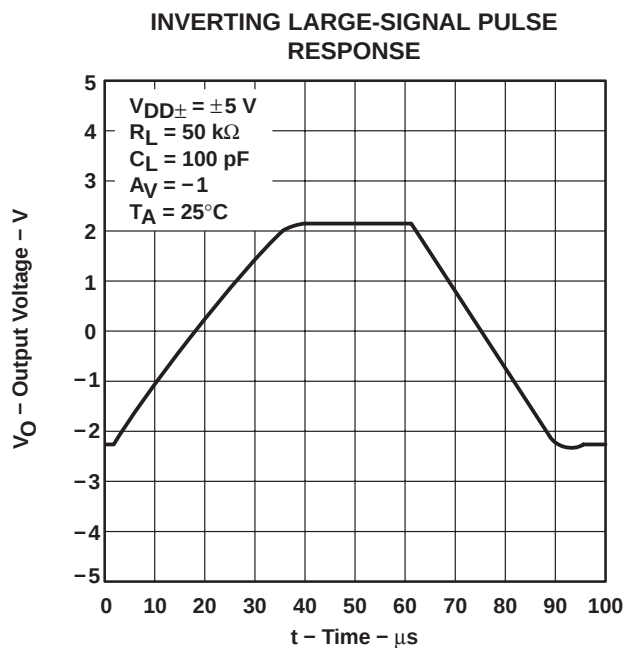


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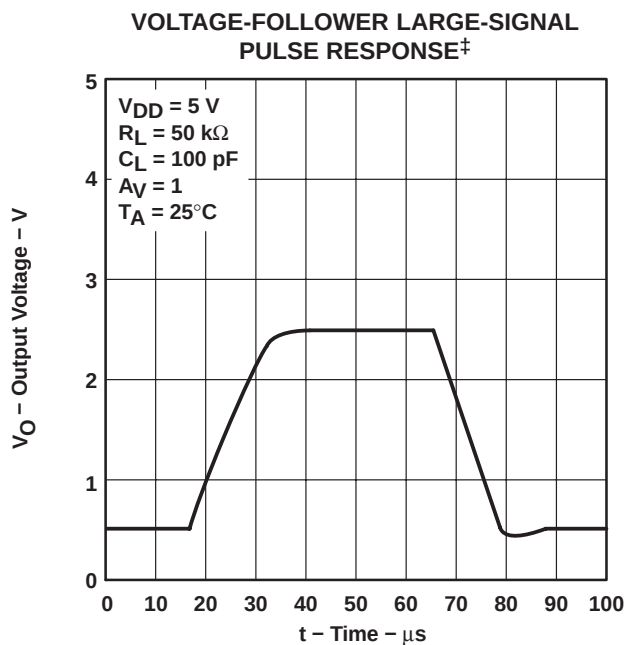


Figure 43

[†] Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

[‡] For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

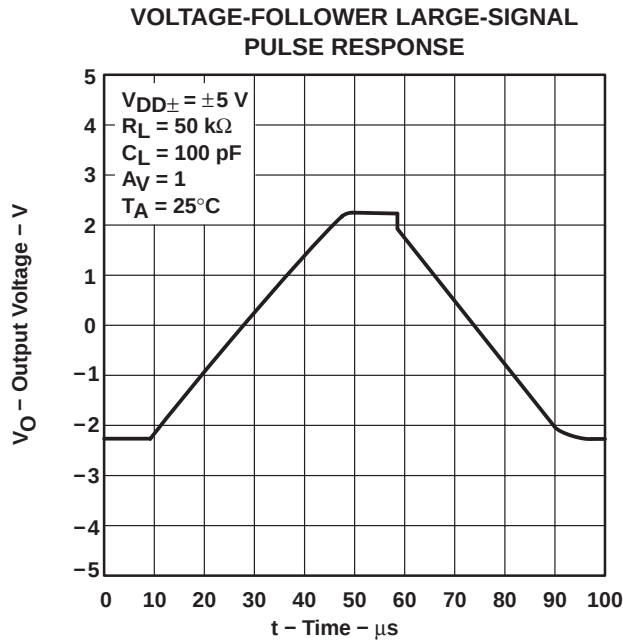


Figure 44

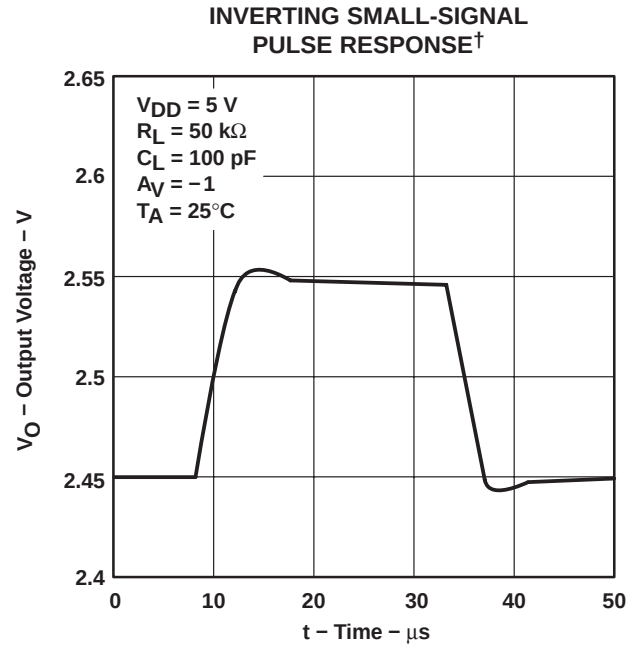


Figure 45

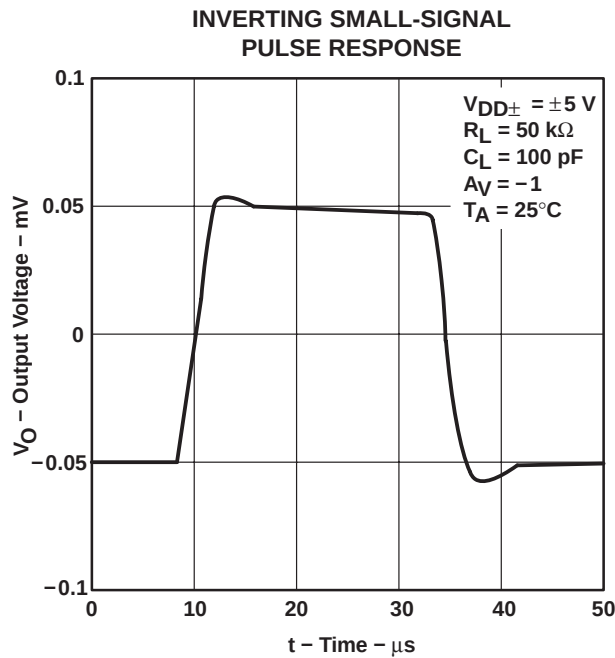


Figure 46

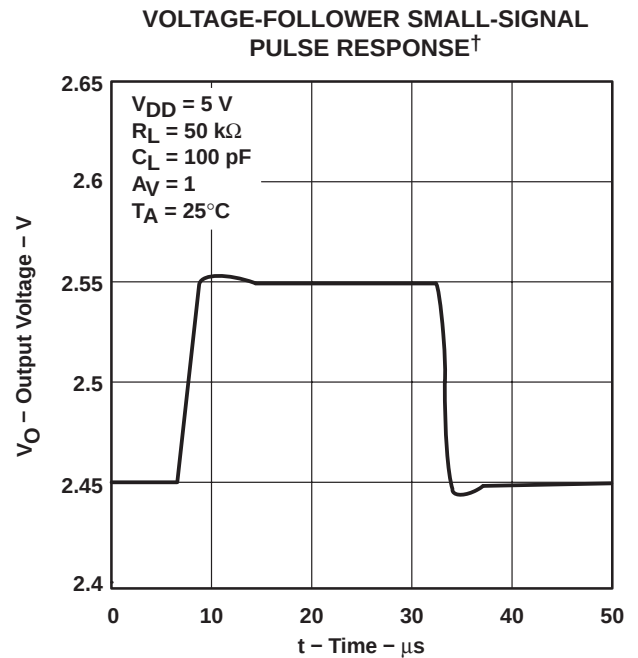


Figure 47

† For curves where $V_{DD} = 5 \text{ V}$, all loads are referenced to 2.5 V.

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TYPICAL CHARACTERISTICS

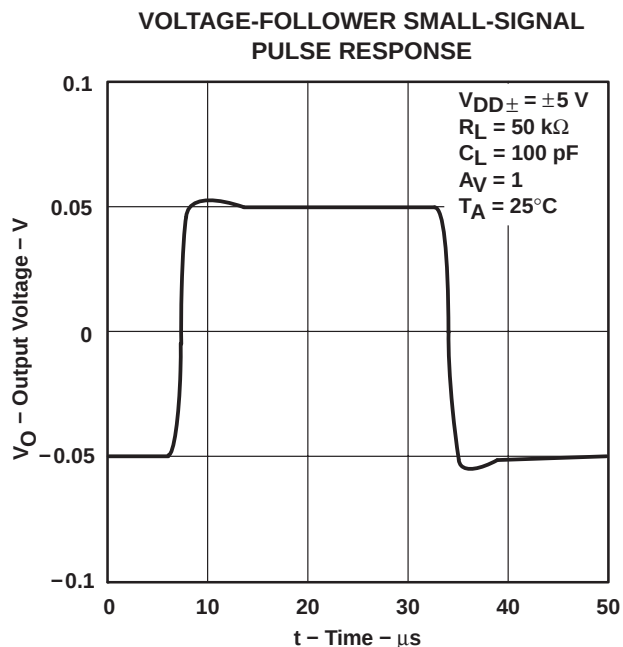


Figure 48

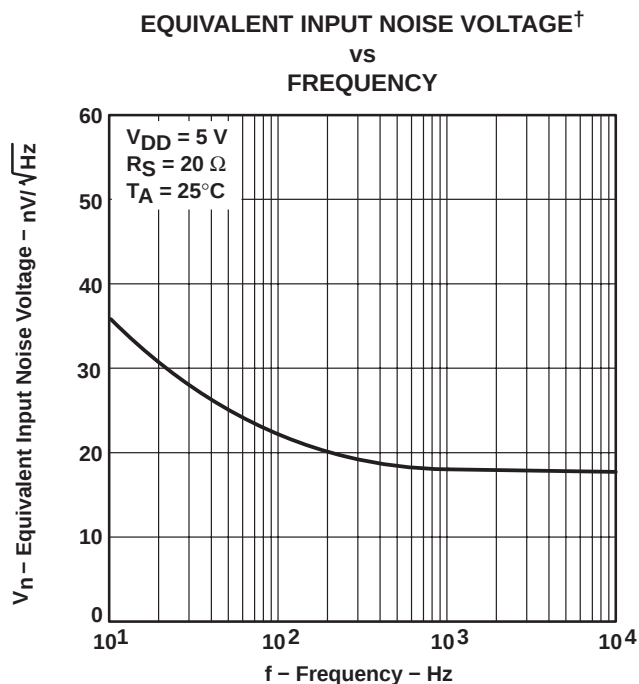


Figure 49

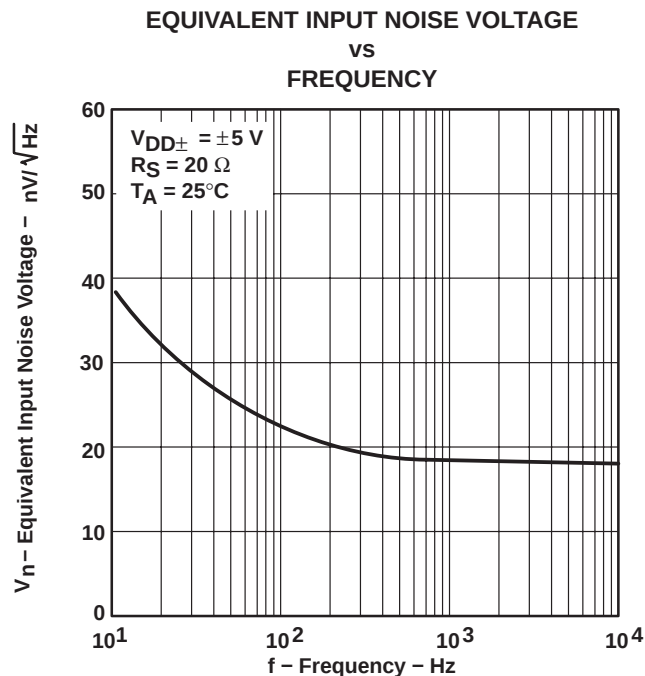


Figure 50

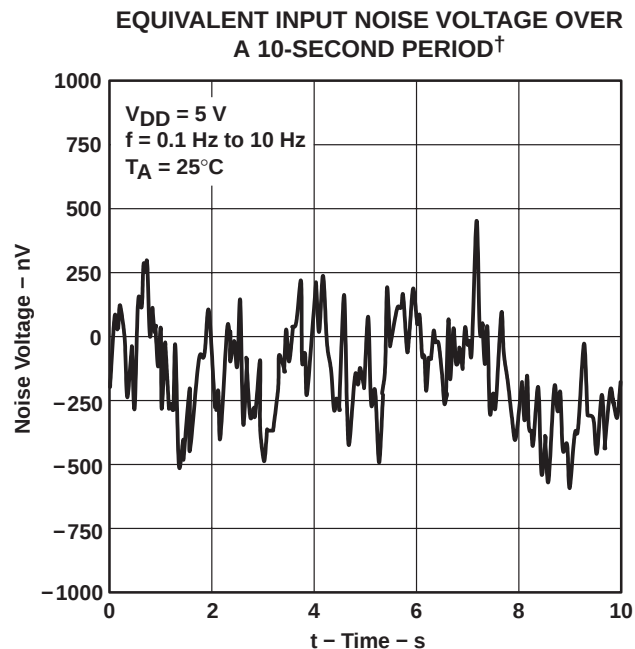
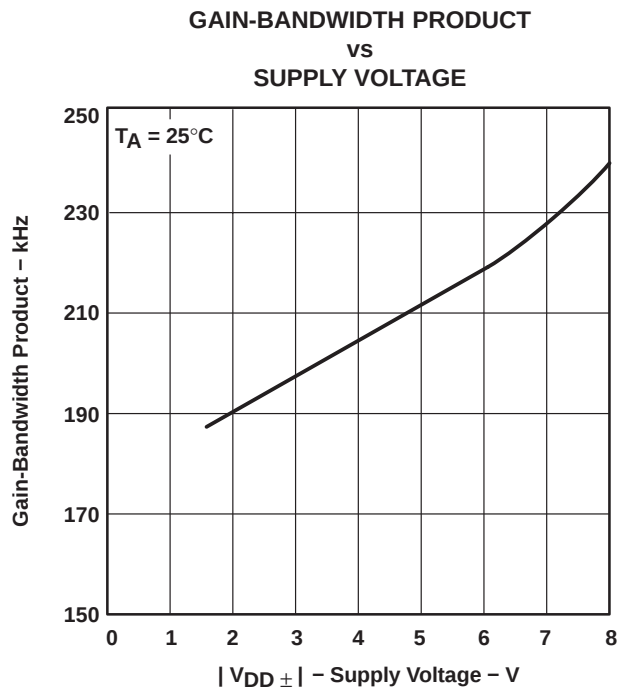
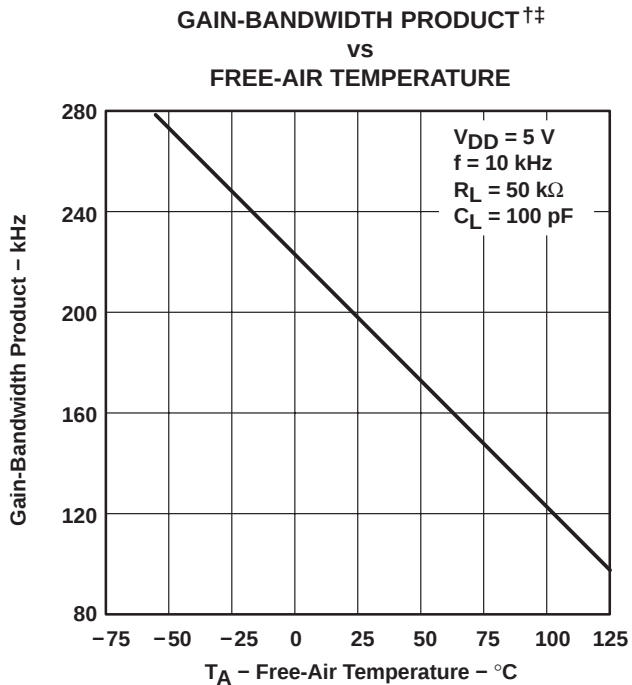
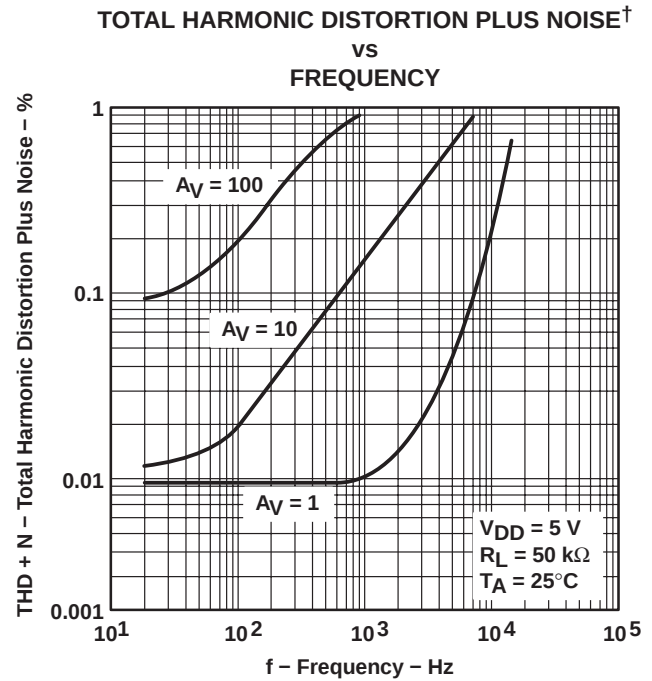
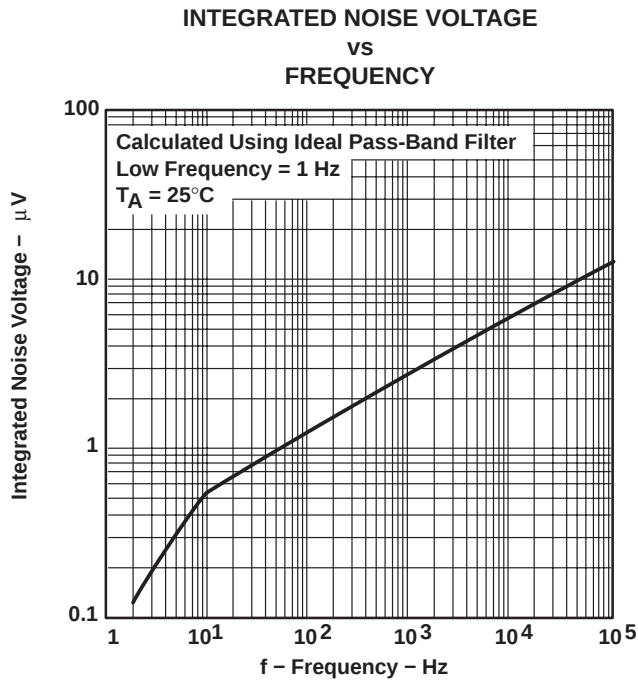


Figure 51

† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

TYPICAL CHARACTERISTICS



† For curves where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V .

†† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

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TYPICAL CHARACTERISTICS

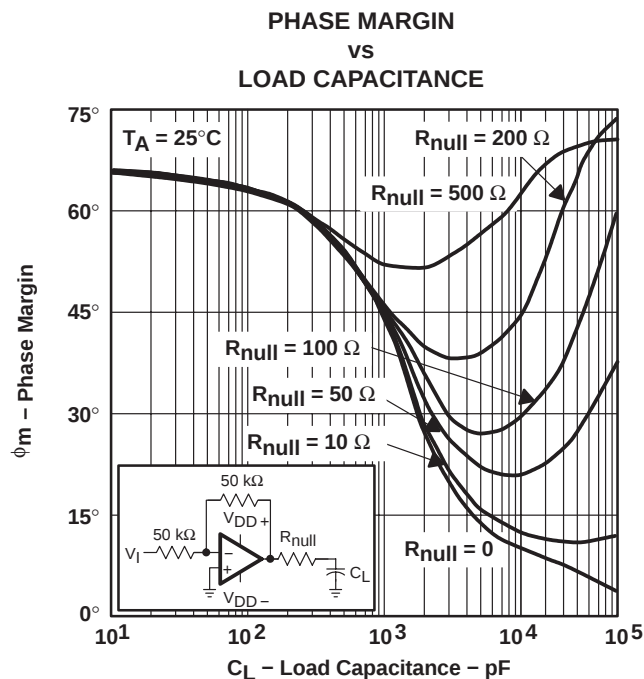


Figure 56

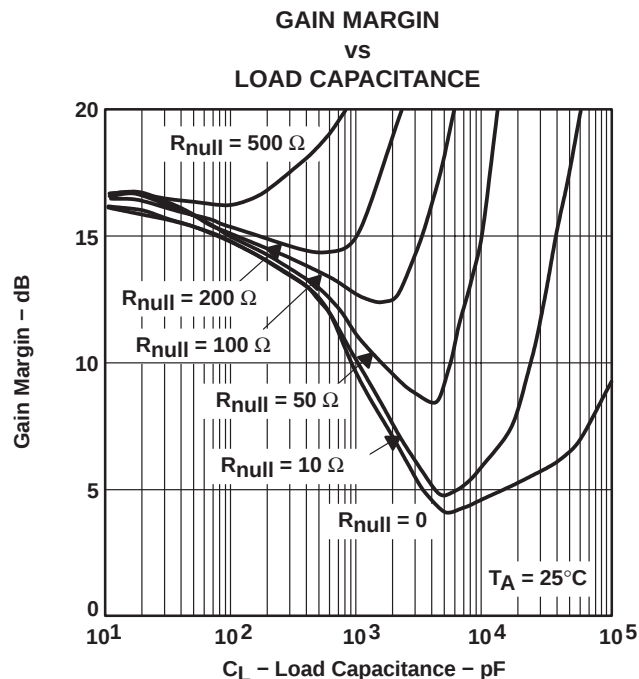


Figure 57

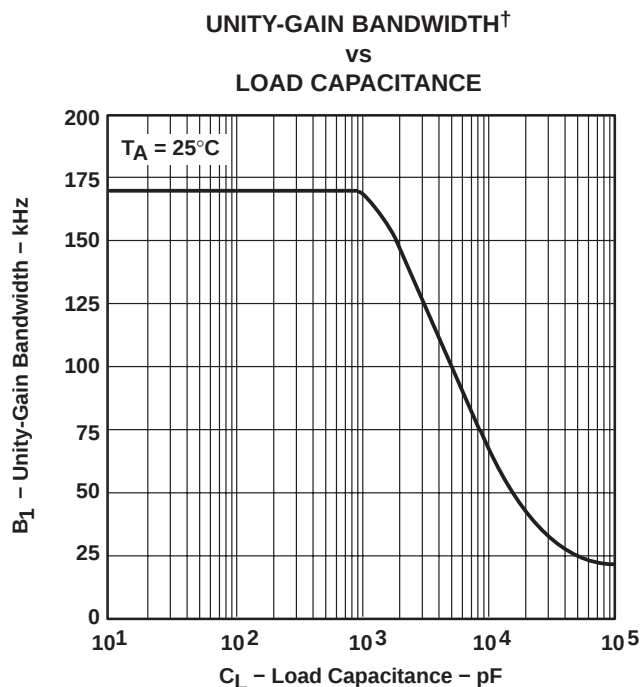


Figure 58

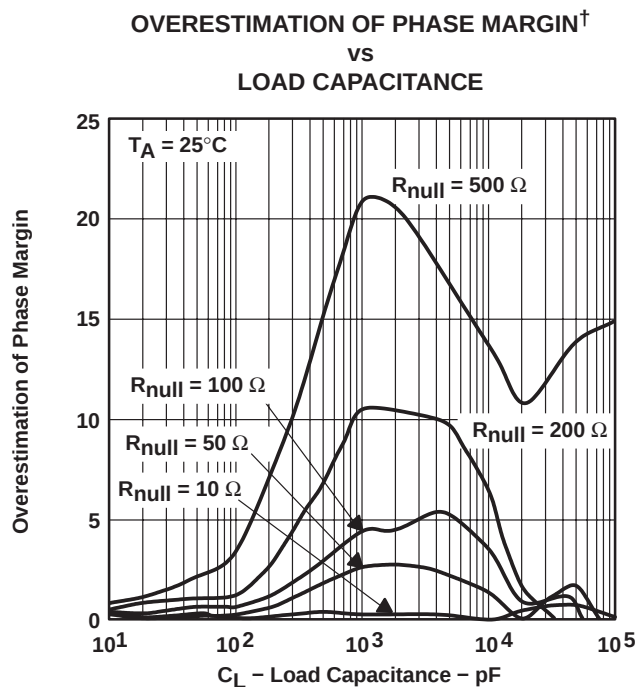


Figure 59

† See application information

APPLICATION INFORMATION

driving large capacitive loads

The TLC225x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 56 and Figure 57 illustrate its ability to drive loads up to 1000 pF while maintaining good gain and phase margins ($R_{null} = 0$).

A smaller series resistor (R_{null}) at the output of the device (see Figure 60) improves the gain and phase margins when driving large capacitive loads. Figure 56 and Figure 57 show the effects of adding series resistances of 10 Ω , 50 Ω , 100 Ω , 200 Ω , and 500 Ω . The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation 1 can be used.

$$\Delta\phi_{m1} = \tan^{-1} \left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L \right) \quad (1)$$

Where :

$\Delta\phi_{m1}$ = Improvement in phase margin

UGBW = Unity-gain bandwidth frequency

R_{null} = Output series resistance

C_L = Load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 58). To use equation 1, UGBW must be approximated from Figure 58.

Using equation 1 alone overestimates the improvement in phase margin, as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, thus providing additional phase shift and reducing the overall improvement in phase margin.

Using Figure 60, with equation 1 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitance loads.

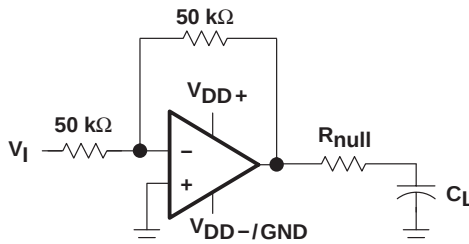


Figure 60. Series-Resistance Circuit

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APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using MicroSim *Parts*™, the model generation software used with MicroSim *PSPice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 61 are generated using the TLC225x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 4: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

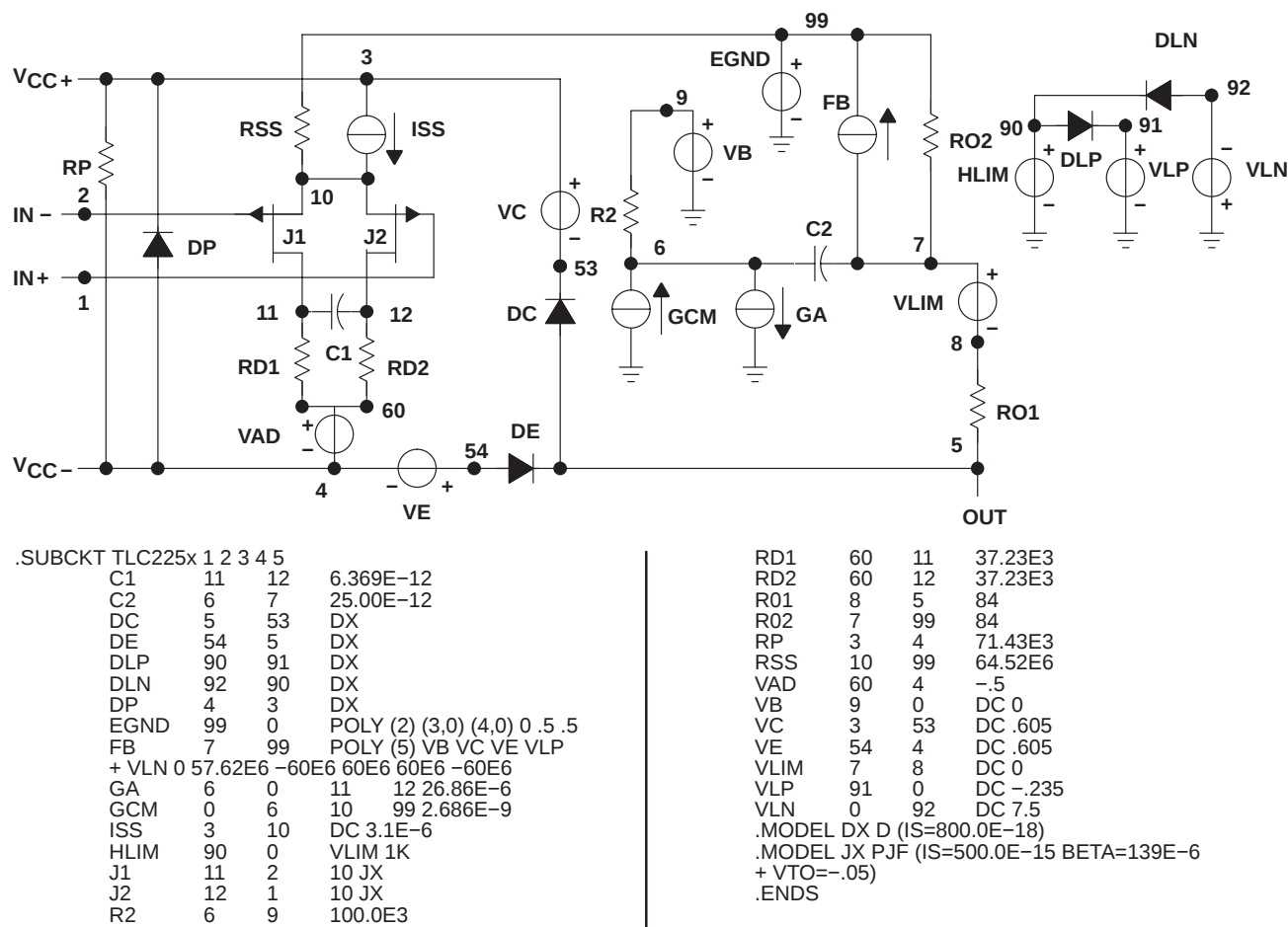


Figure 61. Boyle Macromodel and Subcircuit

PSPice and Parts are trademarks of MicroSim Corporation.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2252AQDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252AE	Samples
TLC2252QDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252EP	Samples
TLC2254AQDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2254AEP	Samples
TLC2254QDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2254EP	Samples
V62/04682-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252EP	Samples
V62/04682-02XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2252AE	Samples
V62/04682-03YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2254EP	Samples
V62/04682-04YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC2254AEP	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC2252-EP, TLC2252A-EP, TLC2254-EP, TLC2254A-EP :

- Catalog: [TLC2252](#), [TLC2252A](#), [TLC2254](#), [TLC2254A](#)
- Automotive: [TLC2252-Q1](#), [TLC2252A-Q1](#), [TLC2254-Q1](#), [TLC2254A-Q1](#)
- Military: [TLC2252M](#), [TLC2252AM](#), [TLC2254M](#), [TLC2254AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2252AQDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2252QDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2254AQDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2254QDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2252AQDREP	SOIC	D	8	2500	367.0	367.0	35.0
TLC2252QDREP	SOIC	D	8	2500	367.0	367.0	35.0
TLC2254AQDREP	SOIC	D	14	2500	333.2	345.9	28.6
TLC2254QDREP	SOIC	D	14	2500	333.2	345.9	28.6

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

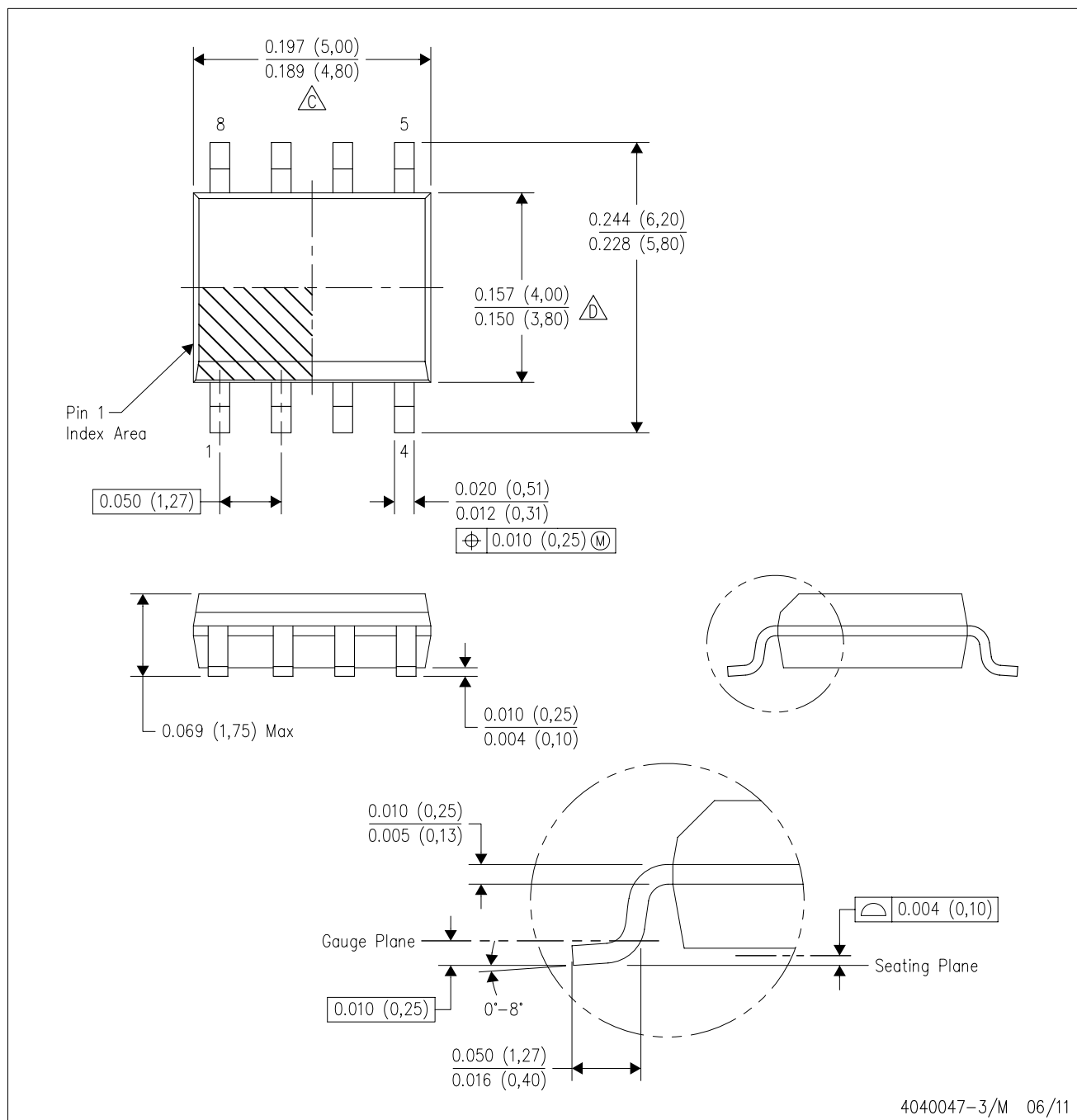
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

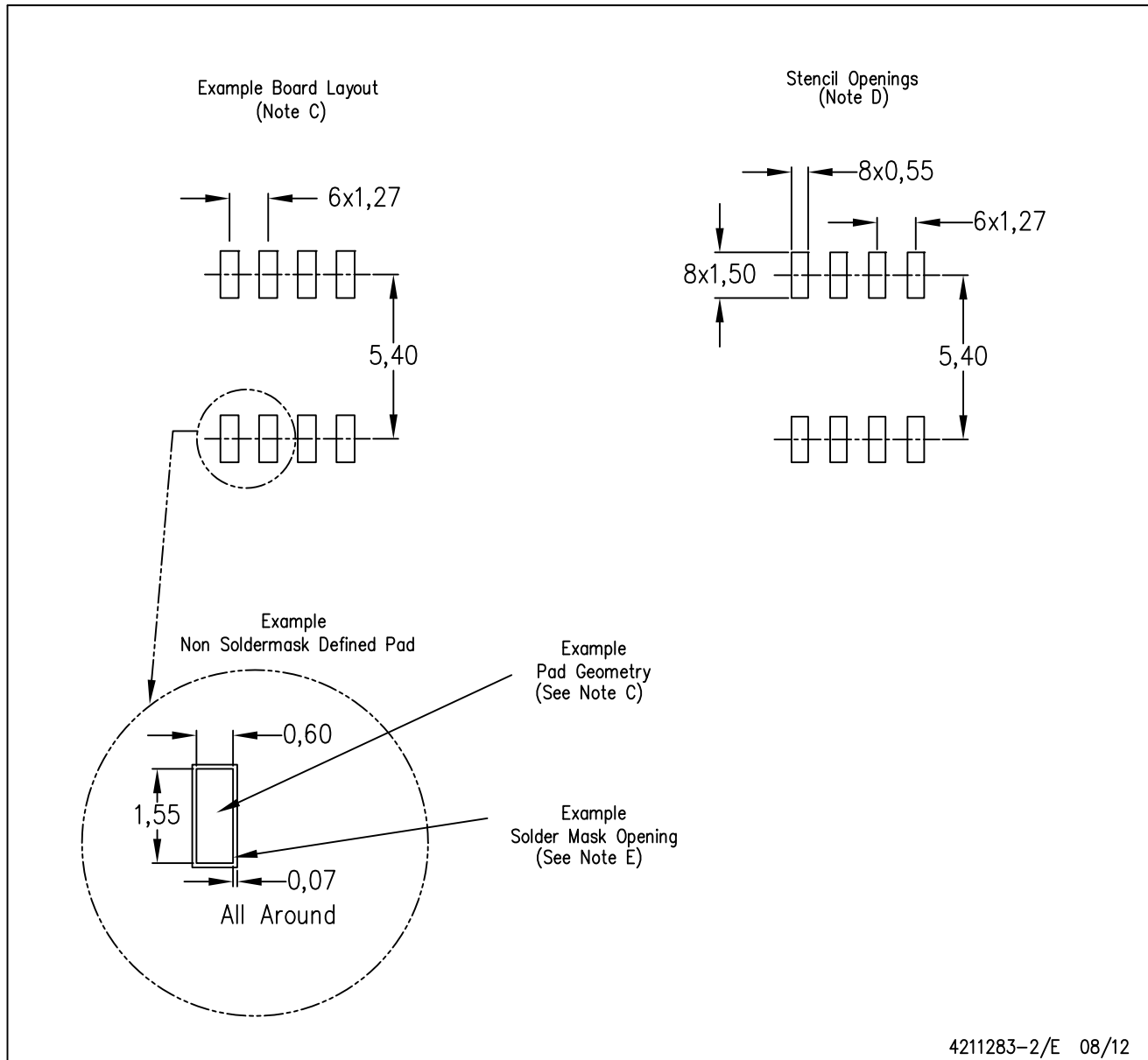
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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