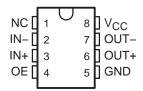
SLCS002D - JUNE 1983 - REVISED AUGUST 2003

- Operates From a Single 5-V Supply
- 0-V to 5.5-V Common-Mode Input Voltage Range
- Self-Biased Inputs
- Complementary 3-State Outputs
- Enable Capability
- Hysteresis . . . 5 mV Typ
- Response Times . . . 25 ns Typ

## D, P, PS, OR PW PACKAGE (TOP VIEW)



NC-No internal connection

#### description/ordering information

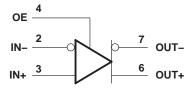
The TL712 is a high-speed comparator fabricated with bipolar Schottky process technology. The circuit has differential analog inputs and complementary 3-state TTL-compatible logic outputs with symmetrical switching characteristics. When the output enable (OE) is low, both outputs are in the high-impedance state. This device operates from a single 5-V supply and is useful as a disk memory read-chain data comparator.

#### ORDERING INFORMATION

TA	PACKAC	3E†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP (P)	Tube of 50	TL712CP	TL712CP
	COIC (D)	Tube of 75	TL712CD	TI 7400
000 to 7000	SOIC (D)	Reel of 2500	TL712CDR	TL712C
0°C to 70°C	SOP (PS)	Reel of 2000	TL712CPSR	T712
	TOCOD (DIA))	Tube of 150	TL712CPW	T740
	TSSOP (PW)	Reel of 2000	TL712CPWR	T712

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

#### symbol (positive logic)

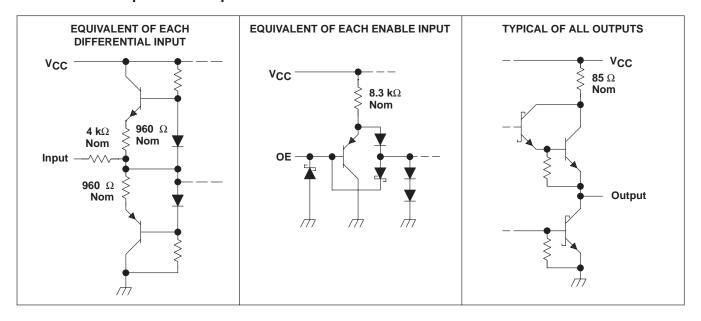




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#### schematics of inputs and outputs



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V <sub>CC</sub> (see Note 1)		7 V
Differential input voltage, V <sub>ID</sub> (see Note 2)		
Input voltage, V <sub>I</sub> , any differential input		±25 V
Output enable voltage		7 V
Low-level output current, I <sub>OL</sub>		50 mA
Package thermal impedance, θ <sub>JA</sub> (see Notes 3 and 4):	D package	97°C/W
	P package	85°C/W
	PS package	95°C/W
	PW package	
Operating virtual junction temperature, T <sub>J</sub>		150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10	seconds	260°C
Storage temperature range, T <sub>stg</sub>		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground.
  - 2. Differential voltage values are at IN+ with respect to IN -.
  - 3. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  - 4. The package thermal impedance is calculated in accordance with JESD 51-7.



#### recommended operating conditions

		MIN	NOM	MAX	UNIT
Vcc	Supply voltage	4.75	5	5.25	V
VIC	Common-mode input voltage	0		5.5	V
ІОН	High-level output current			-1	mA
lOL	Low-level output current			16	mA
TA	Operating free-air temperature	0		70	°C

## electrical characteristics at $V_{CC}$ = 5 V, $T_A$ = 25 $^{\circ}C$

	PARAMETER	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
VT	Threshold voltage (V <sub>T+</sub> and V <sub>T-</sub> )	V <sub>ICR</sub> = 0 to 5 V		-100†		100	mV
V <sub>hys</sub>	Hysteresis (V <sub>T+</sub> - V <sub>T-</sub> )				5	·	mV
Vон	High-level output voltage	$V_{ID} = 100 \text{ mV},$	$I_{OH} = -1 \text{ mA}$	2.7	3.5		V
VOL	Low-level output voltage	$V_{ID} = -100 \text{ mV},$	$I_{OL} = 16 \text{ mA}$		0.4	0.5	V
loz	Off-state output current	V <sub>O</sub> = 2.4 V				-20	μΑ
II	Enable current	V <sub>I</sub> = 5.5 V				100	μΑ
lн	High-level enable current	V <sub>IH</sub> = 2.7 V				20	μΑ
Ι <sub>Ι</sub> L	Low-level enable current	V <sub>IL</sub> = 0.4 V	•			-360	μΑ
rį	Differential input resistance		•	4		·	kΩ
r <sub>o</sub>	Output resistance		•			100	Ω
los	Short-circuit output current		•	-15		-85	mA
Icc	Supply current	$V_{ID} = 0$ ,	No load		17	20	mA

<sup>&</sup>lt;sup>†</sup> The algebraic convention, where the more-negative limit is designated as minimum, is used in this data sheet for input threshold voltage levels only.

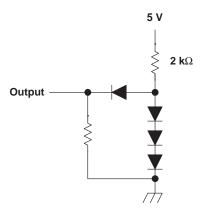
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

	PARAMETER	TE	TYP	UNIT	
tPLH	Propagation delay time, low-to-high-level output	TTL load.	See Note 5 and Figure 1	25	ns
tPHL	Propagation delay time, high-to-low-level output	i i L loau,	See Note 5 and Figure 1	25	ns

NOTE 5: The response time specified is for a 100-mV input step with 5-mV overdrive (105 mV total) and is the interval between the input step function and the instant when the output crosses 2.5 V.



#### PARAMETER MEASUREMENT INFORMATION



NOTE A: All diodes are 1N4148 or equivalent.

Figure 1. TTL Output Load Circuit

#### TYPICAL CHARACTERISTICS

# OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVE VOLTAGES

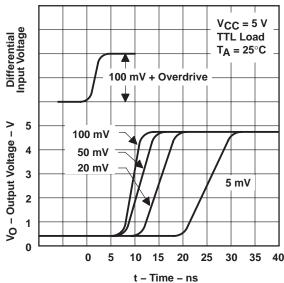


Figure 2

## OUTPUT RESPONSE FOR VARIOUS INPUT OVERDRIVE VOLTAGES

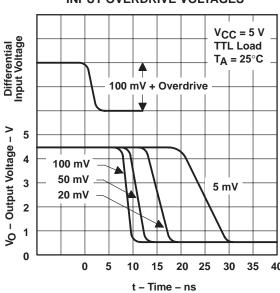


Figure 3

#### **TYPICAL CHARACTERISTICS**

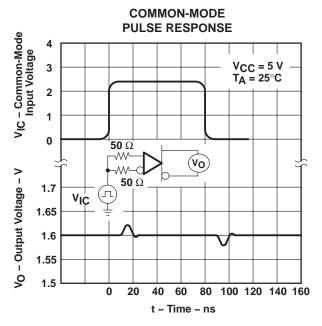


Figure 4





.com 4-Jun-2007

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp (3)
TL712CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CP	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL712CPE4	ACTIVE	PDIP	Р	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL712CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL712CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame



#### PACKAGE OPTION ADDENDUM

4-Jun-2007

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

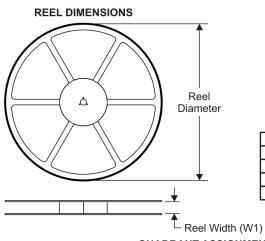
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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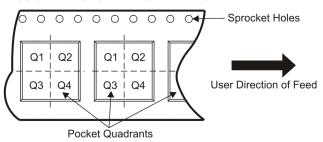
#### TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

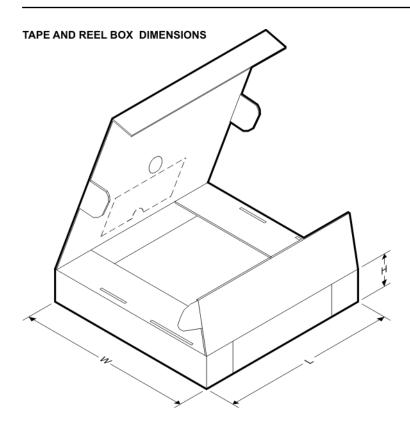
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL712CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL712CPSF	so so	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL712CPWF	R TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1



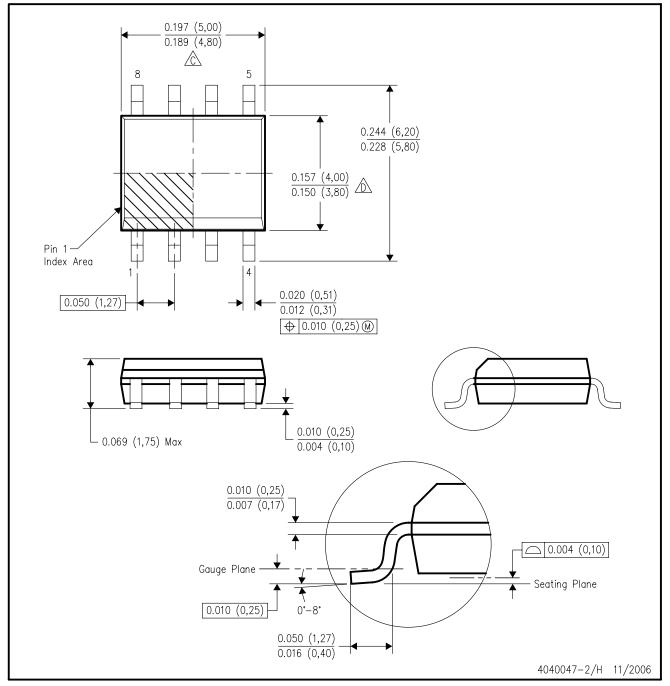


\*All dimensions are nominal

ı	7 III GIITTOTOTOTO GI O TTOTTITTGI							
	Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	TL712CDR	SOIC	D	8	2500	342.9	338.1	20.6
	TL712CPSR	SO	PS	8	2000	346.0	346.0	33.0
	TL712CPWR	TSSOP	PW	8	2000	346.0	346.0	29.0

## D (R-PDSO-G8)

### PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.



#### PW (R-PDSO-G\*\*)

#### 14 PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE

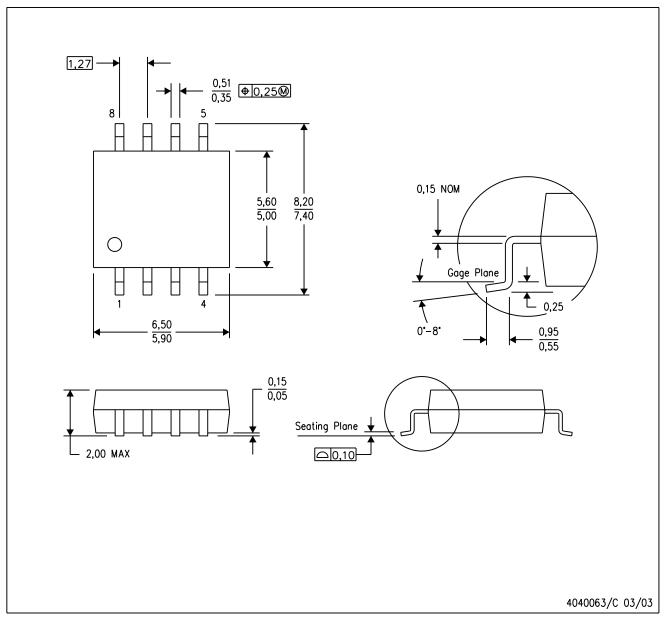


NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



NOTES: A. All linear dimensions are in millimeters.

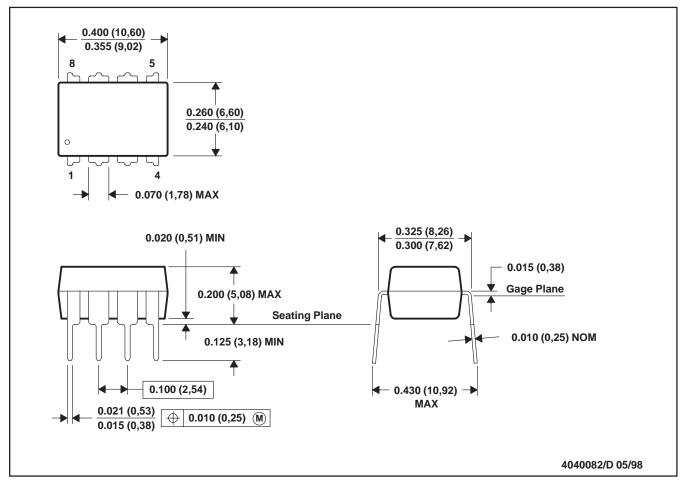
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



#### P (R-PDIP-T8)

#### PLASTIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001

For the latest package information, go to  $http://www.ti.com/sc/docs/package/pkg\_info.htm$ 

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