

SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

SDLS007

D2635. JANUARY 1981 - REVISED MARCH 1988

- 8-Bit Parallel Storage Register Inputs ('LS597)
- Parallel 3-State I/O, Storage Register Inputs, Shift Register Outputs ('LS598)
- Shift Register has Direct Overriding Load and Clear
- Accurate Shift-Frequency . . . DC to 20 MHz

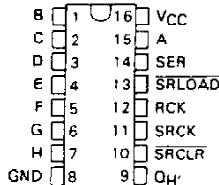
description

The 'LS597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

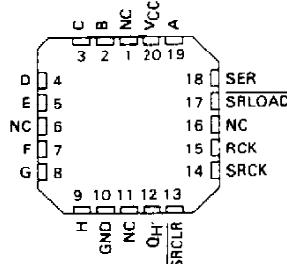
The 'LS598 comes in a 20-pin package and has all the features of the 'LS597 plus 3-state I/O ports that provide parallel shift register outputs and also has multiplexed serial data inputs.

SN54LS597 . . . J OR W PACKAGE
SN74LS597 . . . N PACKAGE

(TOP VIEW)

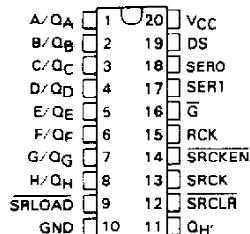


SN54LS597 . . . FK PACKAGE
(TOP VIEW)

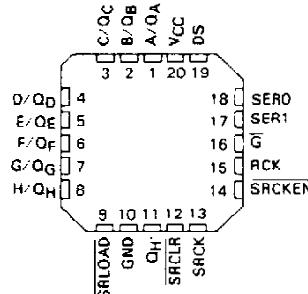


SN54LS598 . . . J OR W PACKAGE
LS598 . . . DW OR N PACKAGE

(TOP VIEW)



SN54LS598 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

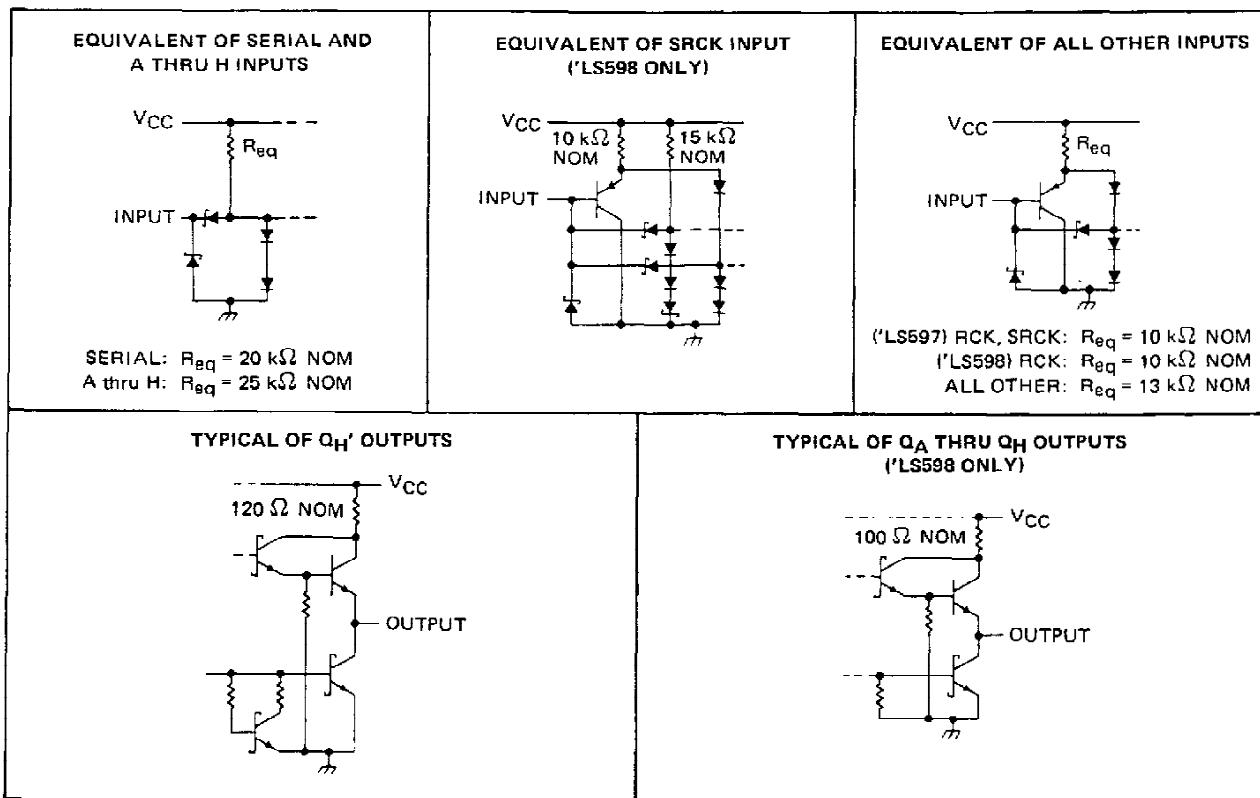
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

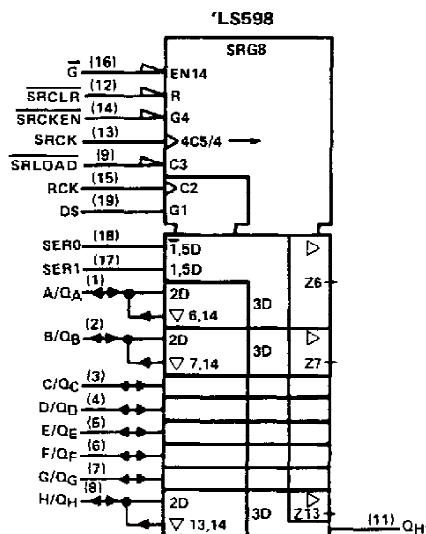
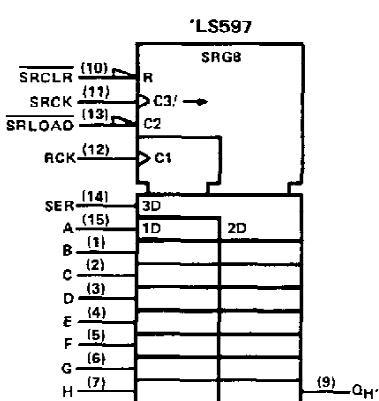
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SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

schematics of inputs and outputs



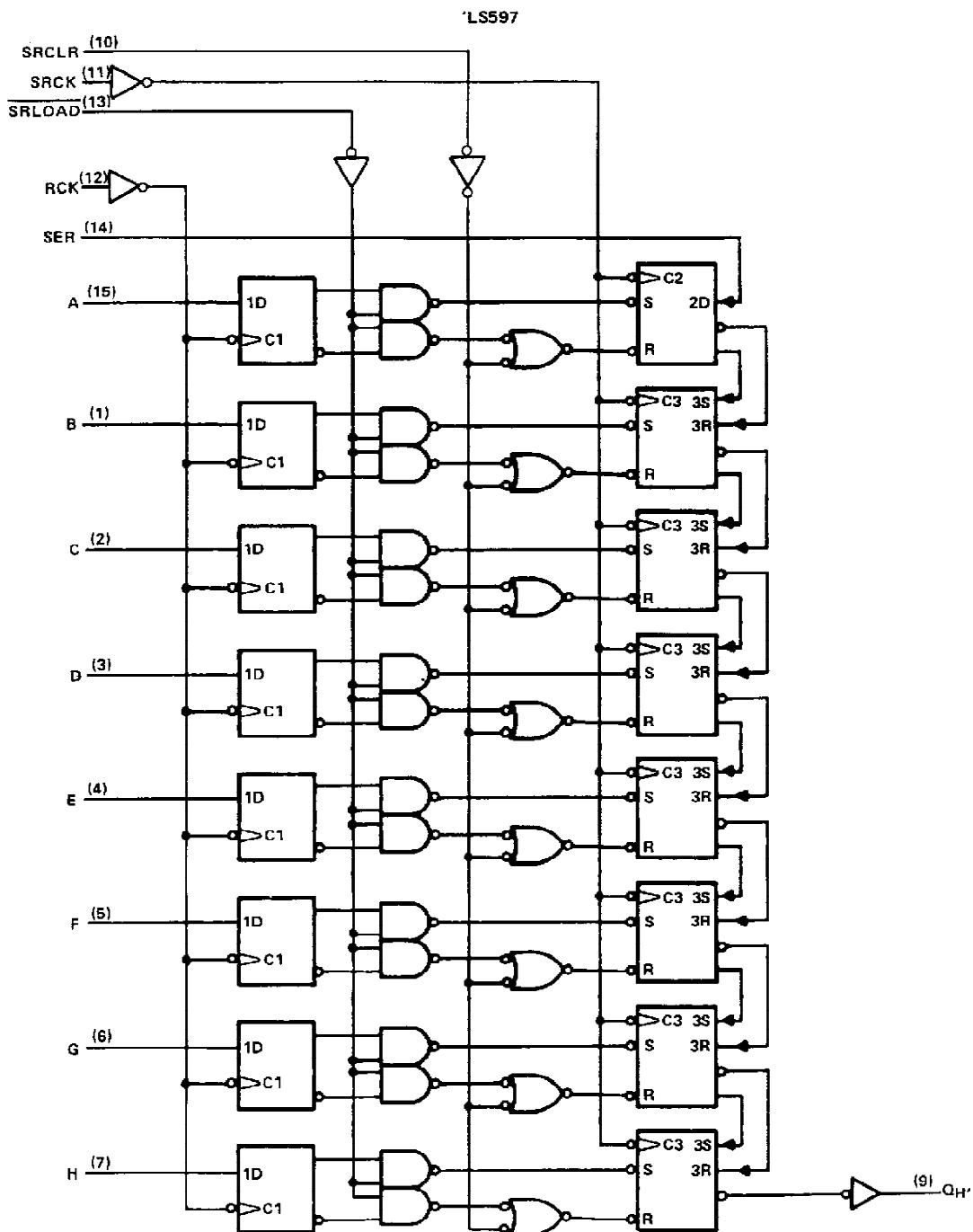
logic symbols[†]



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

SN54LS597, SN74LS597
8-BIT SHIFT REGISTERS WITH INPUT LATCHES

logic diagram (positive logic)



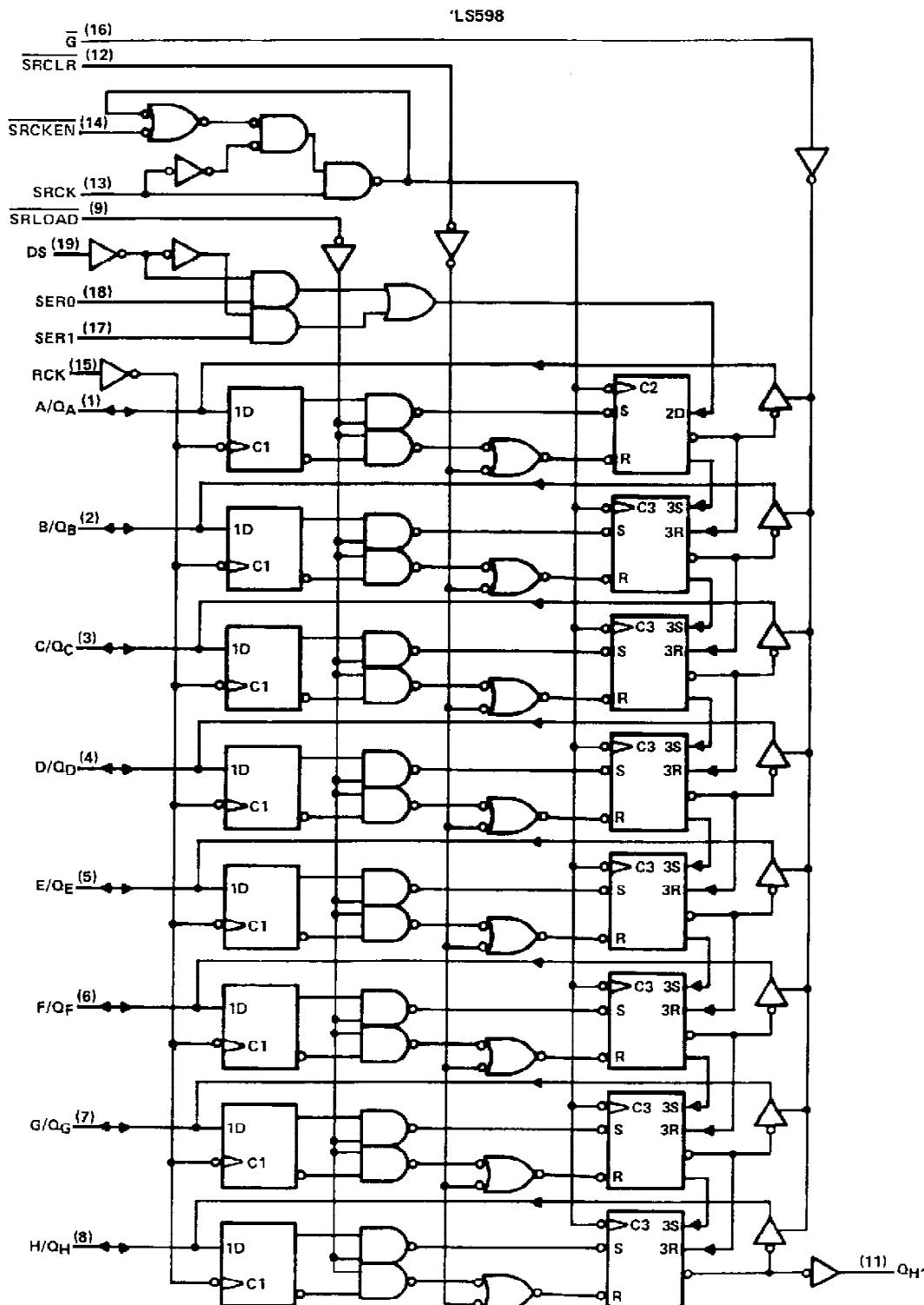
Pin numbers shown are for DW, J, N, and W packages.

TEXAS
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**SN54LS598, SN74LS598
8-BIT SHIFT REGISTERS WITH INPUT LATCHES**

logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

TEXAS
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SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

| | | | SN54LS' | | | SN74LS' | | | UNIT |
|------------------|--------------------------------|--|---------|-----|-----|---------|-----|------|------|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| V _{IH} | High-level input voltage | | 2 | | | 2 | | | V |
| V _{IL} | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| I _{OH} | High-level output current | Q _H ' | | | -1 | | | -1 | mA |
| | | Q _A thru Q _H , 'LS598 only | | | -1 | | | -2.6 | |
| I _{OL} | Low-level output current | Q _H ' | | | 8 | | | 16 | mA |
| | | Q _A thru Q _H , 'LS598 only | | | 12 | | | 24 | |
| f _{SCK} | Shift clock frequency | | 0 | | 20 | 0 | | 20 | MHz |
| t _w | Pulse duration | SRCK | high | | 15 | | | 15 | ns |
| | | | low | | 35 | | | 35 | |
| | | RCK | | | 20 | | | 20 | |
| | | SRCLR | | | 20 | | | 20 | |
| | | SRLOAD | | | 40 | | | 40 | |
| | | | | | | | | | |
| t _{su} | Setup time | Data before RCK↑ | | | 20 | | | 20 | ns |
| | | DS before SRCK↑ ('LS598 only) | | | 30 | | | 30 | |
| | | SRCKEN low before SRCK↑ ('LS598 only) | | | 20 | | | 20 | |
| | | SRCLR inactive before SRCK↑ | | | 25 | | | 25 | |
| | | SRLOAD inactive before SRCK↑ | | | 30 | | | 30 | |
| | | RCK↑ before SRLOAD↑ (see Note 2) | | | 40 | | | 40 | |
| | | SER before SRCK↑ | | | 20 | | | 20 | |
| t _h | Hold time | | 0 | | | 0 | | | ns |
| T _A | Operating free-air temperature | | -55 | | 125 | 0 | | 70 | °C |

NOTE 2: The RCK † before SRLOAD † setup time ensures the data saved by RCK † will also be loaded into the shift register.

SN54LS597, SN54LS598, SN74LS597, SN74LS598 8-BIT SHIFT REGISTERS WITH INPUT LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS [†] | | | SN54LS [*] | | | SN74LS [*] | | | UNIT |
|------------------------------|---|--|----|---------------------------|---------------------|------------------|------|---------------------|------------------|-----|------|
| | | | | | MIN | TYP [‡] | MAX | MIN | TYP [‡] | MAX | |
| V _{IK} | | V _{CC} = MIN, I _I = -18 mA | | | -1.5 | | | -1.5 | | | V |
| V _{OH} | 'LS598 Q | V _{CC} = MIN, V _{IH} = 2 V, | | I _{OH} = -1 mA | 2.4 | 3.2 | | | | | V |
| | | V _{IIL} = MAX | | I _{OH} = -2.6 mA | | | | 2.4 | 3.1 | | |
| | Q _H ' | | | I _{OH} = -1 mA | 2.4 | 3.2 | | 2.4 | 3.2 | | |
| V _{OL} | 'LS598 Q | V _{CC} = MIN, V _{IH} = 2 V, | | I _{OL} = 12 mA | 0.25 0.4 | | | 0.25 | 0.4 | | V |
| | | V _{IIL} = MAX | | I _{OL} = 24 mA | | | | 0.35 | 0.5 | | |
| | Q _H ' | | | I _{OL} = 8 mA | 0.25 0.4 | | | 0.25 | 0.4 | | |
| | | | | I _{OL} = 16 mA | | | | 0.35 | 0.5 | | |
| I _{OZH} | 'LS598 Q | V _{CC} = MAX, V _{IH} = 2 V, | | V _{IIL} = MAX, | 20 | | | 20 | 20 | | μA |
| I _{OZL} | 'LS598 Q | V _{CC} = MAX, V _{IH} = 2 V, | | V _{IIL} = MAX, | -0.4 | | | -0.4 | -0.4 | | mA |
| I _I | 'LS598 Q | V _{CC} = MAX | | V _I = 5.5 V | 0.1 | | | 0.1 | 0.1 | | mA |
| | Others | | | V _I = 7 V | 0.1 | | | 0.1 | 0.1 | | mA |
| I _{IH} | V _{CC} = MAX, V _I = 2.7 V | | 20 | | 20 | | | 20 | 20 | | μA |
| I _{IL} | 'LS598 SRCK | | | -0.8 | | | -0.8 | -0.8 | | | mA |
| | SER, A Thru H | V _{CC} = MAX, V _I = 0.4 V | | -0.4 | | | -0.4 | -0.4 | | | |
| | Others | | | -0.2 | | | -0.2 | -0.2 | | | |
| I _{OS} [§] | 'LS598 Q | V _{CC} = MAX, V _O = 0 V | | -30 | -130 | -30 | -130 | | | | mA |
| | Q _H ' | | | -20 | -100 | -20 | -100 | | | | |
| I _{CC} | 'LS597 | I _{CCH} | | | 35 | 53 | | 35 | 53 | | mA |
| | | I _{CCL} | | | 35 | 53 | | 35 | 53 | | |
| | | I _{CCH} | | | 45 | 68 | | 45 | 68 | | |
| | 'LS598 | I _{CCL} | | | 54 | 80 | | 54 | 80 | | |
| | | I _{CCZ} | | | 56 | 85 | | 56 | 85 | | |

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C

[§] Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

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switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$, (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS597 | | | 'LS598 | | | UNIT |
|-----------|----------------------------|----------------|---|--------|-----|-----|--------|-----|-----|------|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| f_{max} | SRCK | Q | $R_L = 667 \Omega$, $C_L = 45 \text{ pF}$ | 20 | 35 | | 20 | 35 | | MHz |
| f_{max} | SRCK | Q_H' | $R_L = 1 \text{ k}\Omega$, $C_L = 30 \text{ pF}$ | 20 | 35 | | | | | MHz |
| t_{PLH} | SRCK \dagger | Q_H' | $R_L = 1 \text{ k}\Omega$, $C_L = 30 \text{ pF}$ | | 15 | 23 | | 11 | 17 | ns |
| t_{PHL} | SPCK \dagger | Q_H' | | | 20 | 30 | | 15 | 23 | ns |
| t_{PLH} | <u>SRLOAD</u> \downarrow | Q_H' | | | 38 | 57 | | 28 | 42 | ns |
| t_{PHL} | <u>SRLOAD</u> \downarrow | Q_H' | | | 29 | 44 | | 20 | 30 | ns |
| t_{PHL} | SRCLR \dagger | Q_H' | | | 24 | 36 | | 18 | 27 | ns |
| t_{PLH} | RCK \dagger | Q_H' | | | 41 | 60 | | 32 | 48 | ns |
| t_{PHL} | RCK \dagger | Q_H' | | | 32 | 48 | | 24 | 36 | ns |
| t_{PLH} | SRCK \dagger | Q | | | | | | 12 | 18 | ns |
| t_{PHL} | SRCK \dagger | Q | | | | | | 19 | 28 | ns |
| t_{PLH} | <u>SRLOAD</u> \downarrow | Q | | | | | | 32 | 48 | ns |
| t_{PHL} | <u>SRLOAD</u> \downarrow | Q | $R_L = 667 \Omega$, $C_L = 45 \text{ pF}$ | | | | | 27 | 40 | ns |
| t_{PHL} | SRCLR \dagger | Q | | | | | | 25 | 38 | ns |
| t_{PZH} | G \downarrow | Q | | | | | | 26 | 31 | ns |
| t_{PZL} | G \downarrow | Q | | | | | | 29 | 43 | ns |
| t_{PHZ} | G \dagger | Q | | | | | | 25 | 38 | ns |
| t_{PLZ} | G \dagger | Q | | | | | | 20 | 30 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS

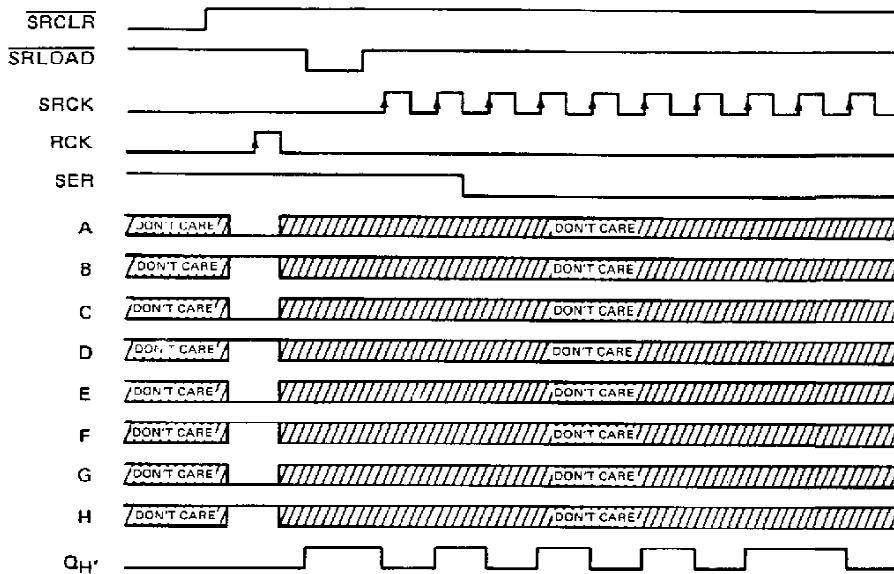
INSTRUMENTS

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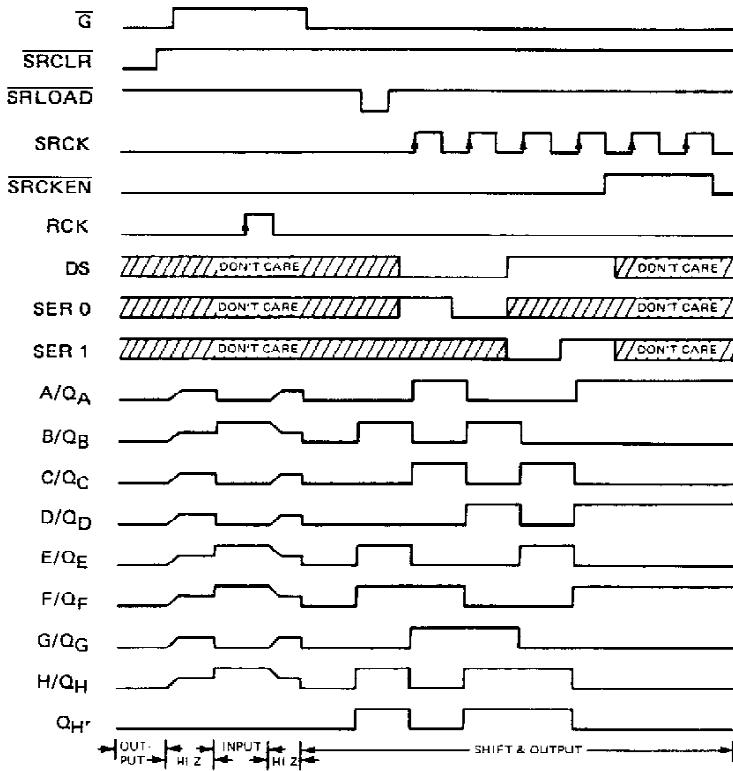
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typical operating sequences

'LS597



'LS598



TEXAS
INSTRUMENTS

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PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|--------------------------|
| 5962-89444012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | Call TI | Call TI | |
| 5962-8944401EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | |
| 5962-8944401EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | Call TI | |
| 5962-8944401FA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Call TI | |
| 5962-8944401FA | ACTIVE | CFP | W | 16 | 1 | TBD | Call TI | Call TI | |
| 5962-89756012A | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI | |
| 5962-89756012A | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI | |
| 5962-8975601SA | OBSOLETE | CFP | W | 20 | | TBD | Call TI | Call TI | |
| 5962-8975601SA | OBSOLETE | CFP | W | 20 | | TBD | Call TI | Call TI | |
| SN54LS597J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54LS597J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SN54LS598J | OBSOLETE | CDIP | J | 20 | | TBD | Call TI | Call TI | |
| SN54LS598J | OBSOLETE | CDIP | J | 20 | | TBD | Call TI | Call TI | |
| SN74LS597D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS597N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS597NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS597NE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS597NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |



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PACKAGE OPTION ADDENDUM

5-Sep-2011

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|--------------------------|
| SN74LS597NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597NSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS597NSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| SN74LS598N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS598N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS598NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SN74LS598NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | |
| SNJ54LS597FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54LS597FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | |
| SNJ54LS597J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54LS597J | ACTIVE | CDIP | J | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54LS597W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54LS597W | ACTIVE | CFP | W | 16 | 1 | TBD | A42 | N / A for Pkg Type | |
| SNJ54LS598FK | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI | |
| SNJ54LS598FK | OBSOLETE | LCCC | FK | 20 | | TBD | Call TI | Call TI | |
| SNJ54LS598J | OBSOLETE | CDIP | J | 20 | | TBD | Call TI | Call TI | |
| SNJ54LS598J | OBSOLETE | CDIP | J | 20 | | TBD | Call TI | Call TI | |
| SNJ54LS598W | OBSOLETE | | | 20 | | TBD | Call TI | Call TI | |
| SNJ54LS598W | OBSOLETE | | | 20 | | TBD | Call TI | Call TI | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN54LS597, SN54LS598, SN74LS597, SN74LS598 :

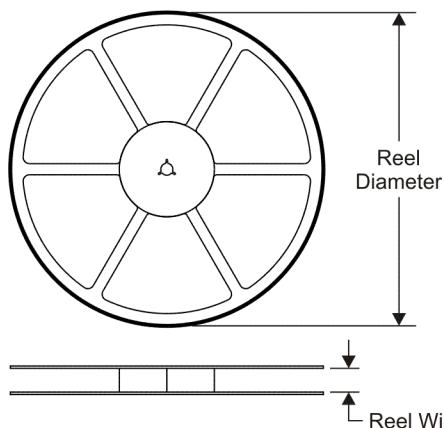
- Catalog: [SN74LS597](#), [SN74LS598](#)
- Military: [SN54LS597](#), [SN54LS598](#)

NOTE: Qualified Version Definitions:

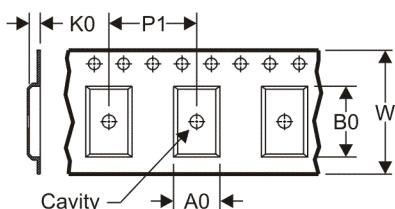
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

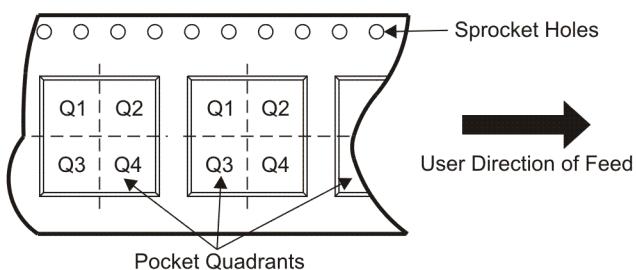


TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

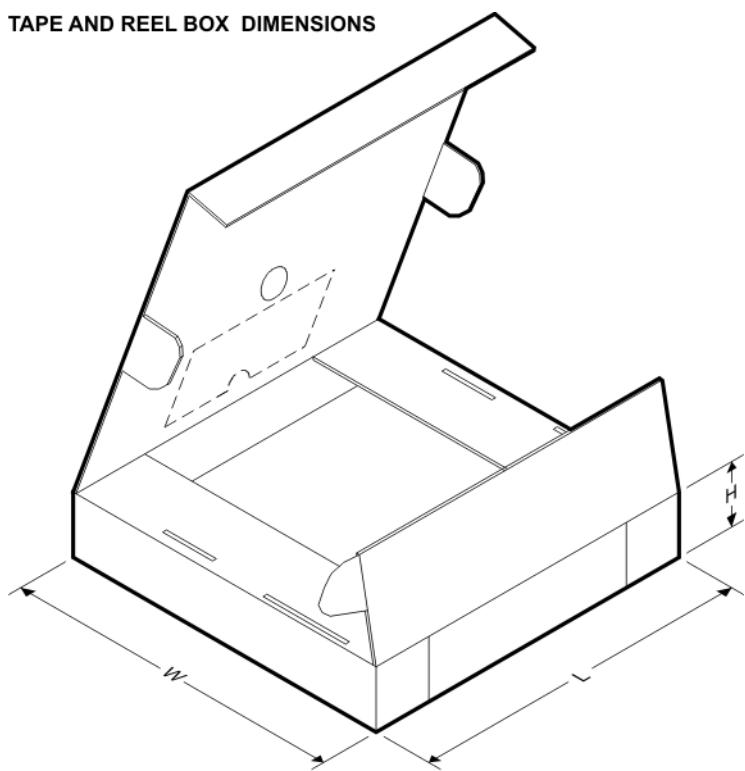
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LS597NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



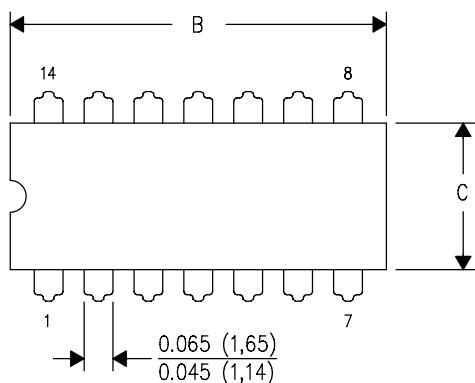
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LS597NSR | SO | NS | 16 | 2000 | 346.0 | 346.0 | 33.0 |

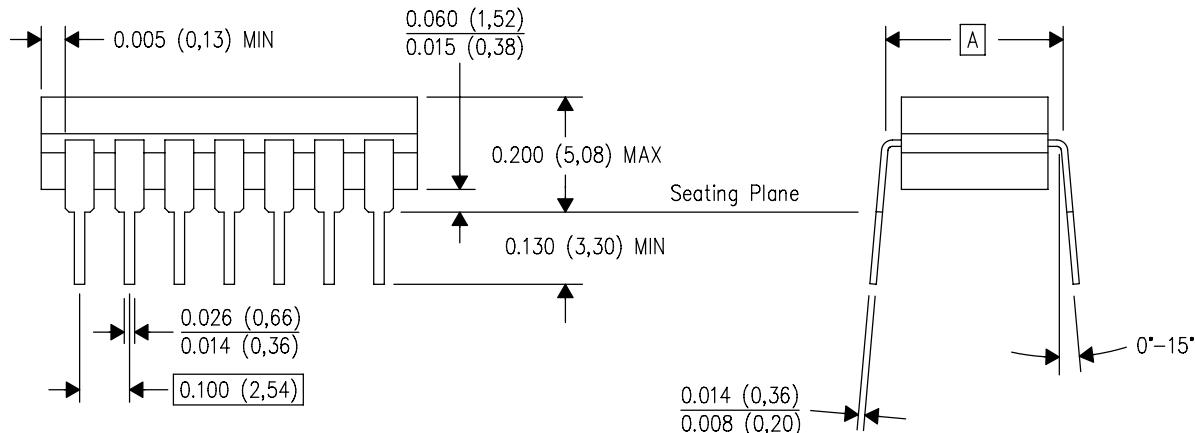
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS **\nDIM | 14 | 16 | 18 | 20 |
|--------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

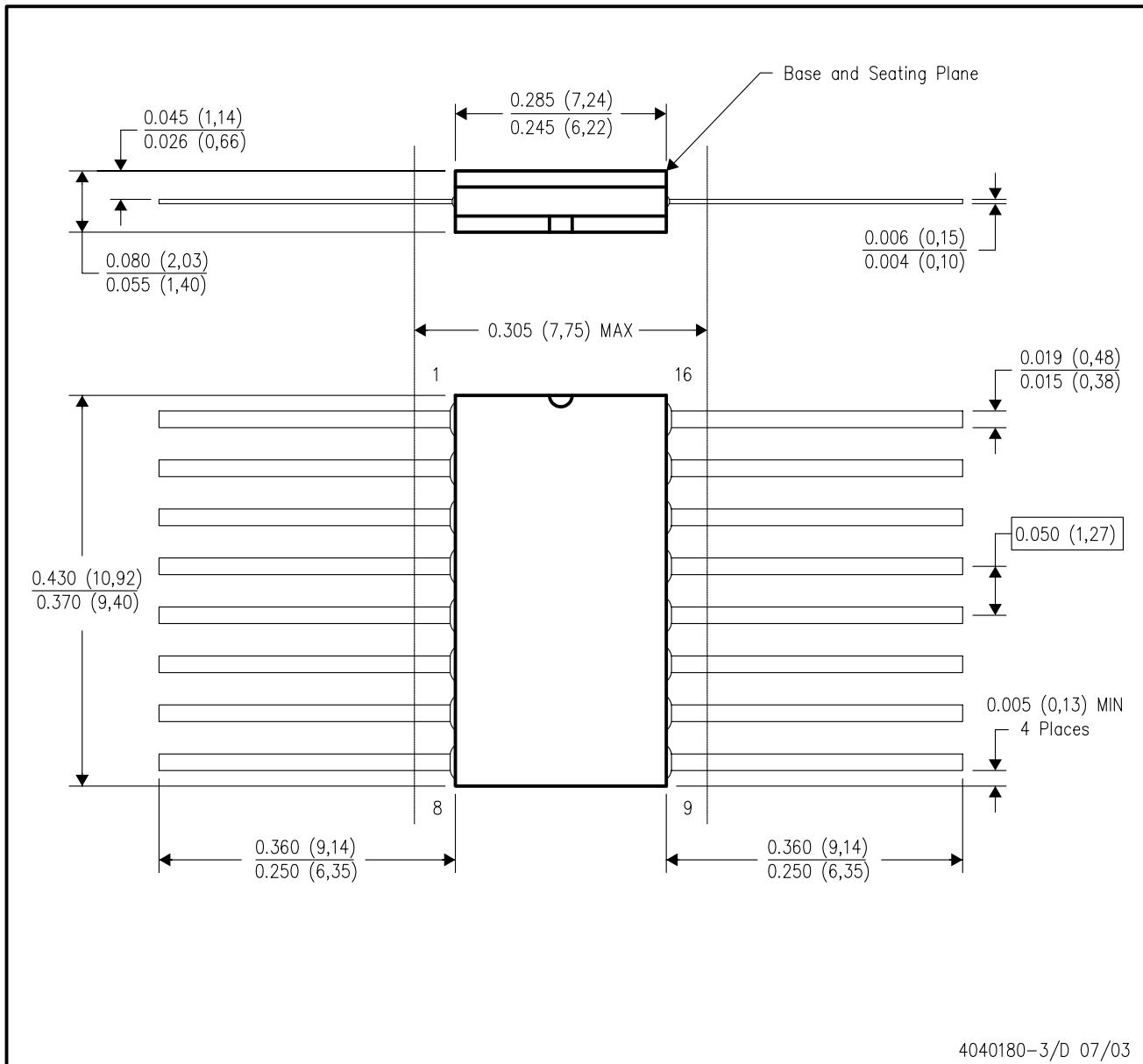


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

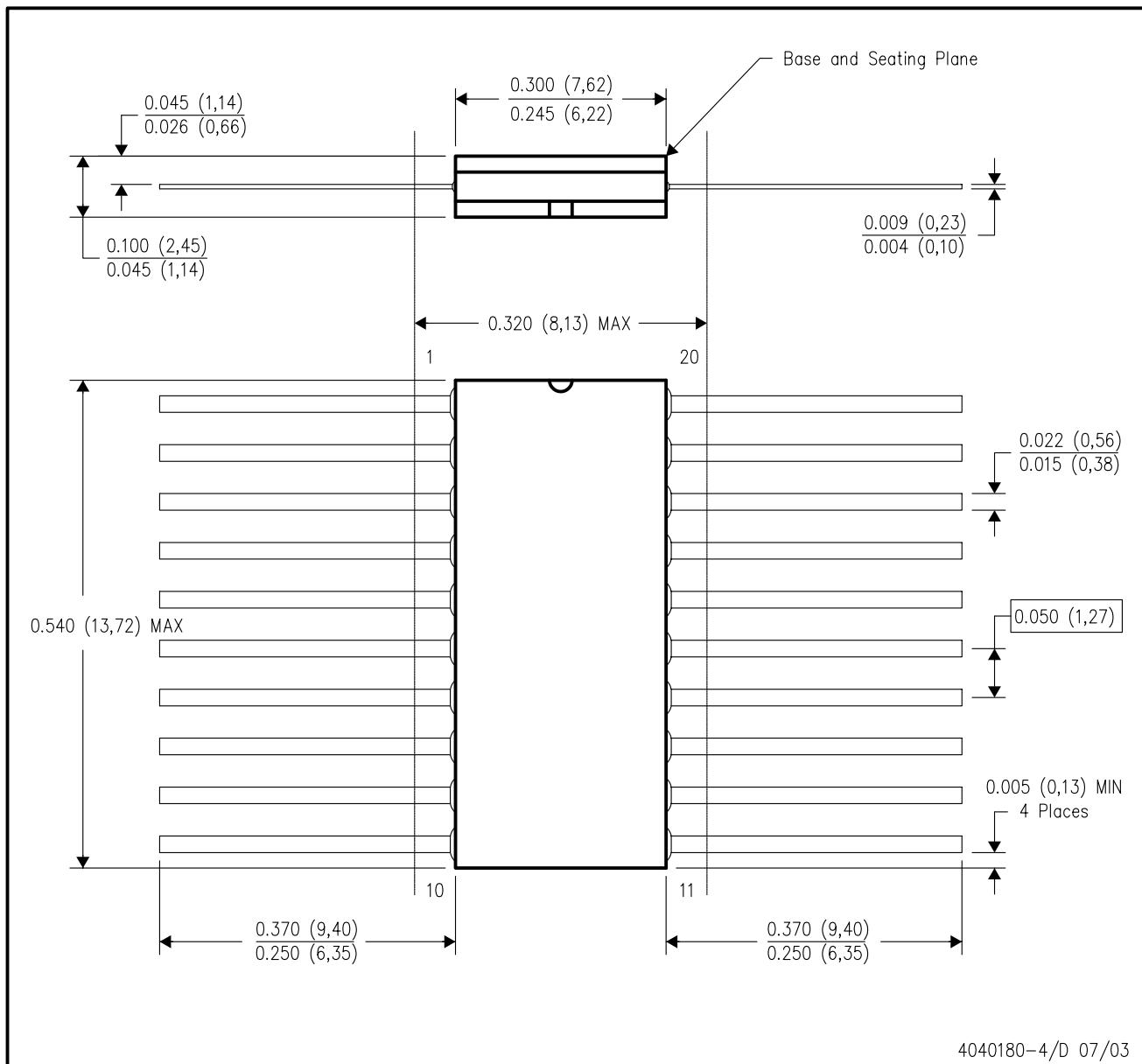


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK

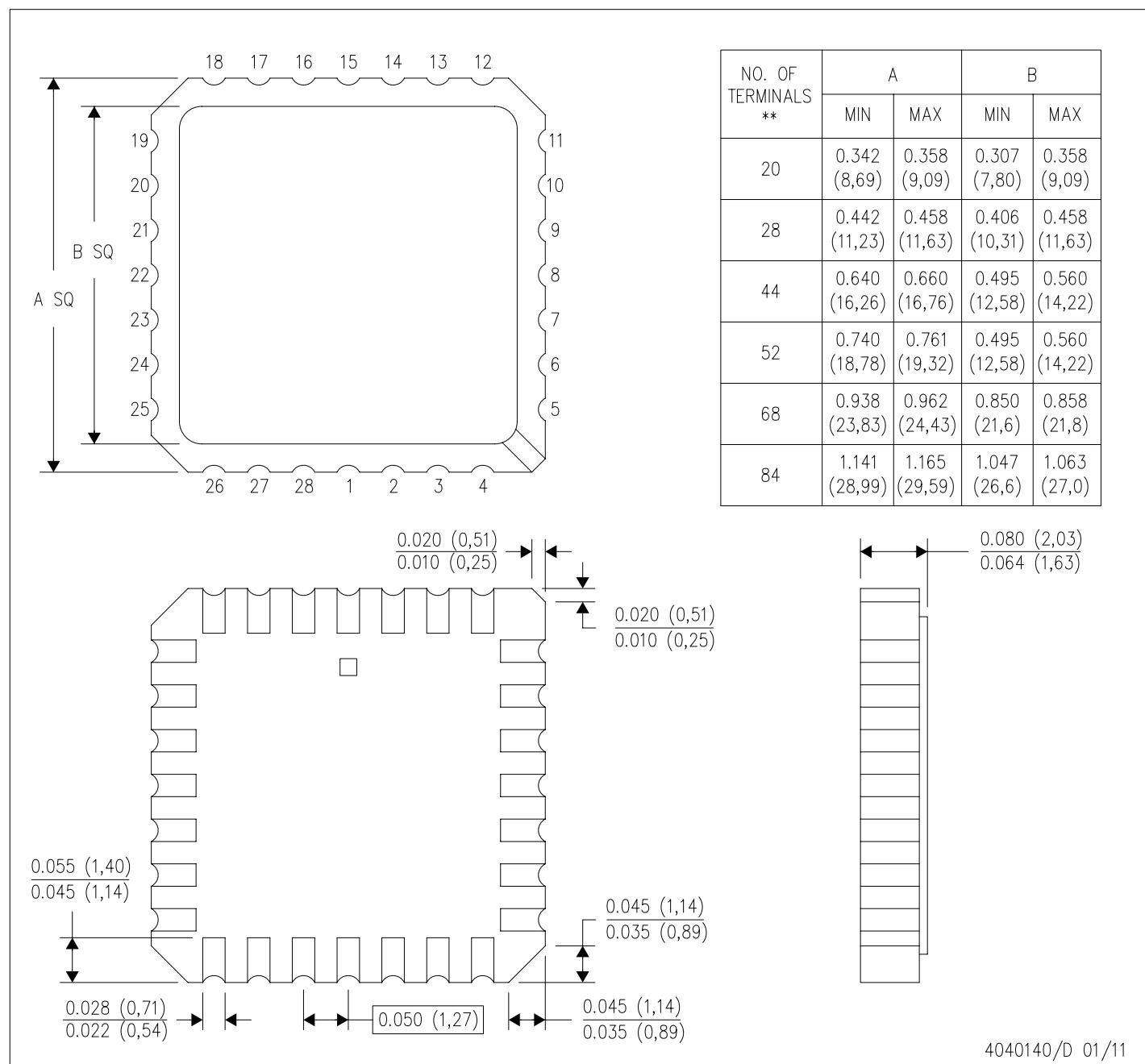


- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



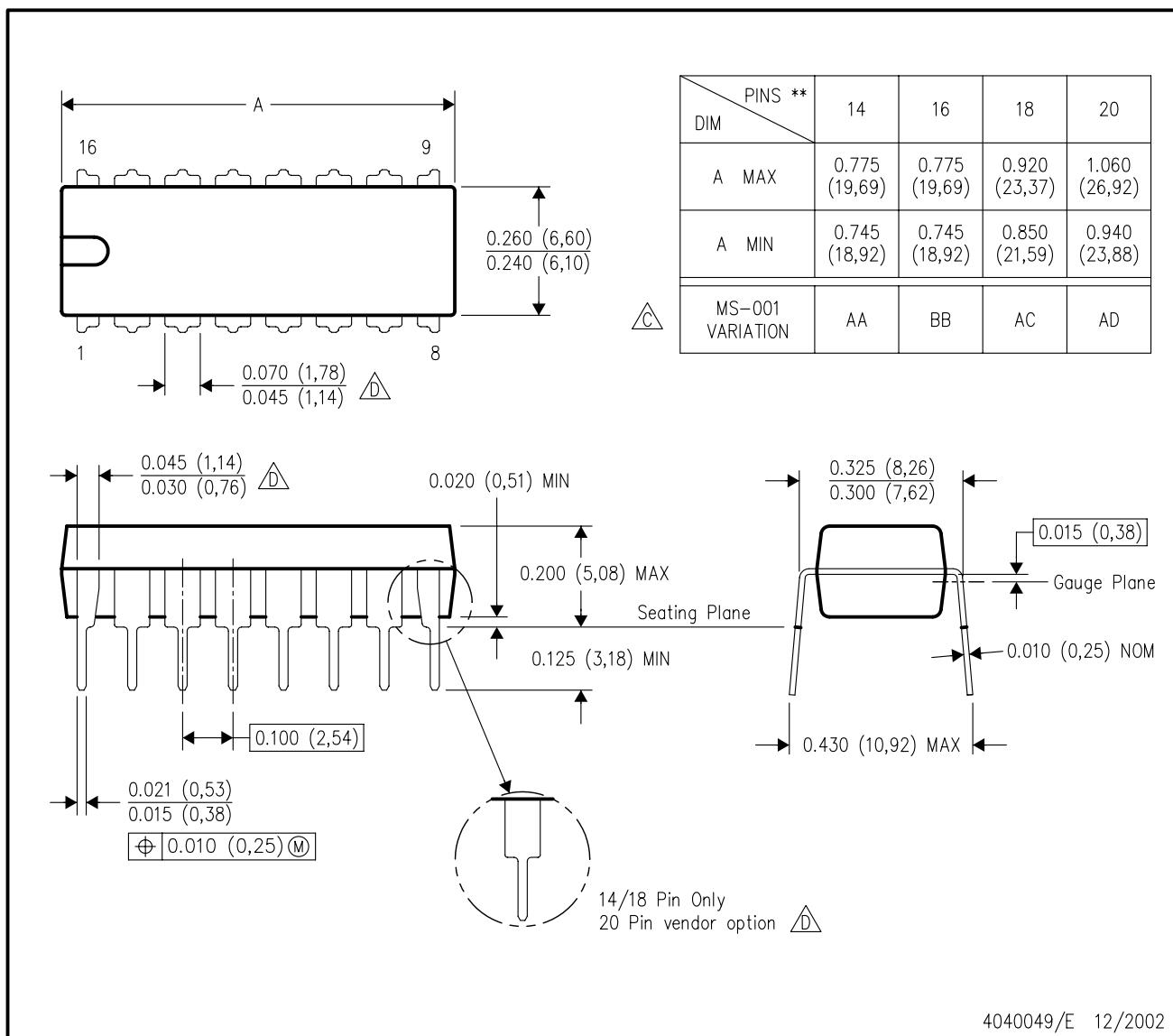
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

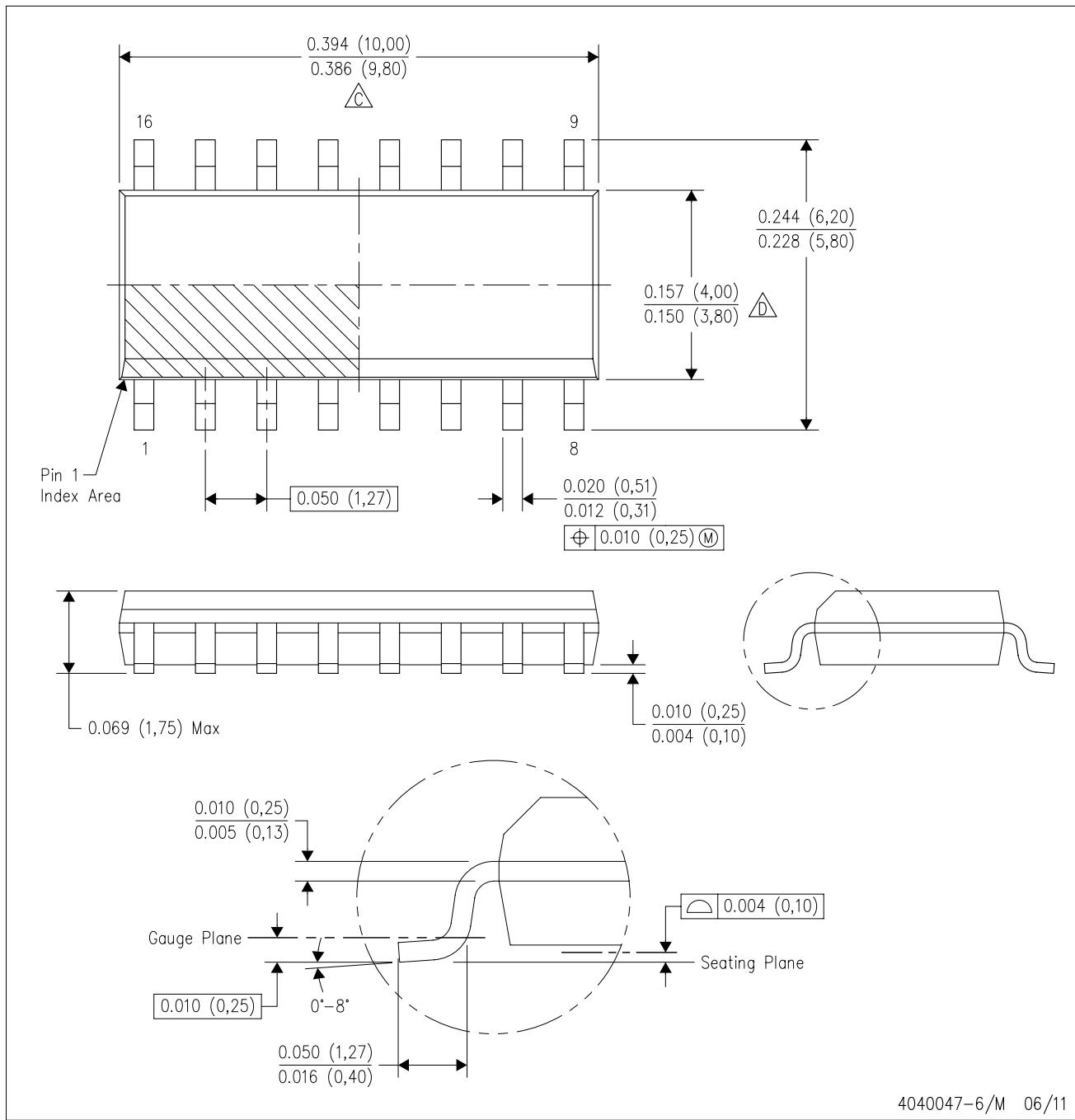
16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

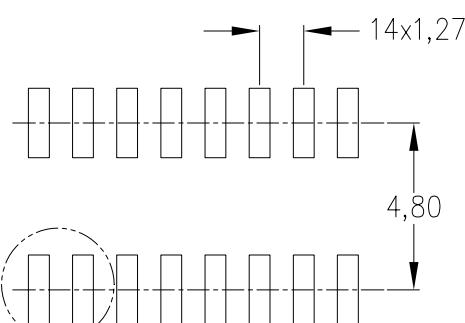
E. Reference JEDEC MS-012 variation AC.

LAND PATTERN DATA

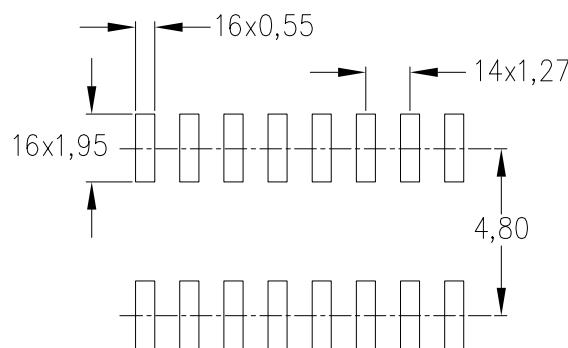
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

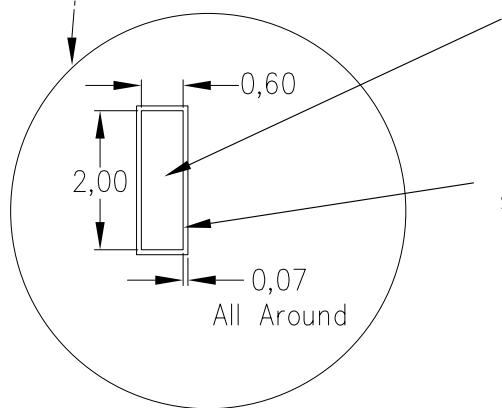
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

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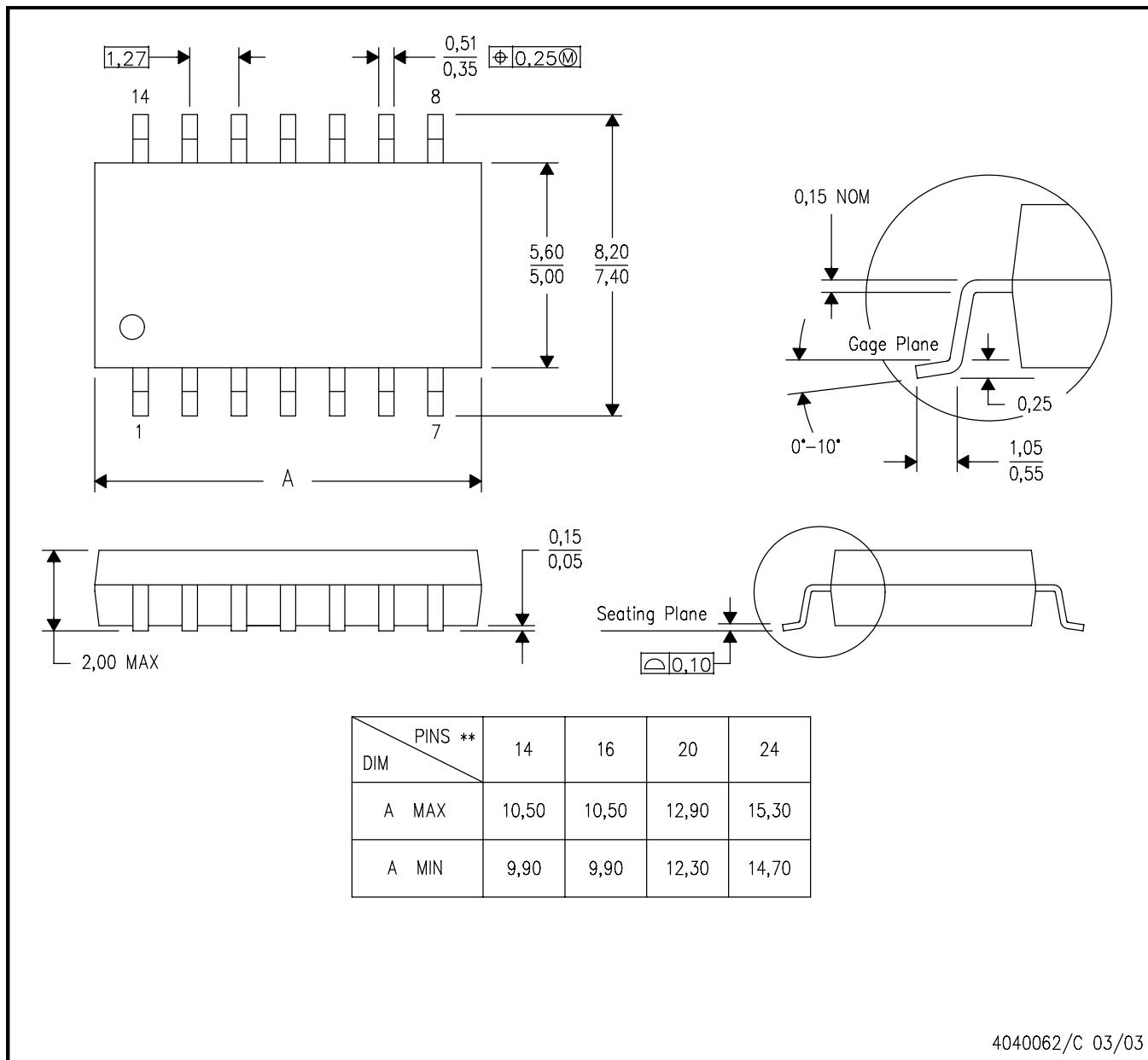
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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