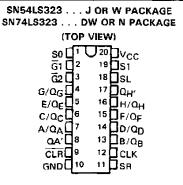
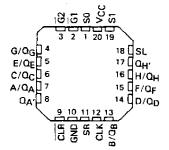
OCTOBER 1976 - REVISED MARCH 1988

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operation:
   Hold (Store) Shift Left
   Shift Right
   Load Data
- · Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Typical Power Dissipation . . . 175 mW
- Exceptionally Stable Shift (Clock)
   Frequency . . . 25 MHz
- Applications: Stacked or Push-Down Registers, Buffer Storage, and Accumulator Registers
- SN54LS299 and SN74LS299 Are Similar But Have Direct Overriding Clear



SN54LS323 . . . FK PACKAGE (TOP VIEW)



#### description

These Low-Power Schottky eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous, and a low-level at the clear input clears the register on the next low-to-high transition of the clock.

#### FUNCTION TABLE

MODE	ZTUPINI								INPUTS/OUTPUTS							OUTPUTS		
	CLR	FUNCTION SELECT		CONTROL		CLK	SERIAL		A/Q <sub>A</sub>	B/Qg	c/ac	o/Qp	E/Qr	F/Q <sub>E</sub>	G/Qc	H/Qu	Q <sub>A</sub> ,	<u>Ω</u> <sub>H</sub> ,
		S1	S0	Ğ1 <sup>†</sup>	G2†		SL	SR		_	Ť		-	•	•		^	
Clear	L	х	L	L.	7	Ť	×	Х		L,	Ļ		L	L	L	L.	L	L
	Ļ	L	×	L	L	†	×	×	L.	L	L	L	L	L	L	L	L	L
	L	Н	н	х	х	†	x	х	х	х	×	х	×	x	×	×	L	Ĺ
Hold	н	L	L	L	٦	×	X	х	QAO	QBQ	QC0	000	Q <sub>EO</sub>	Q <sub>FQ</sub>	$\alpha_{G0}$	Q <sub>H0</sub>	Q <sub>A0</sub>	ано
	н	×	X	L	L	L	×	x	QAO		aco	a <sub>D0</sub>	Œ0	GE0			QAO	QHO
Shift Right	Н	L	Н	L	Ļ	Ť	X	Ĥ	Н	QAn	OB n	Q <sub>Cn</sub>	Qpn	űe,	Q <sub>En</sub>	$Q_{G_0}$	Н	QGo
	Н	L	H	ĹĿ.	L	†	×	L	L	$a_{An}$	α <sub>Bπ</sub>	$a_{Cn}$	$a_{Dn}$	$\alpha_{En}$	$\mathbf{q}_{Fn}$	o <sub>G⊓</sub>	L	$\alpha_{Gn}$
Shift Left	н	Н	L	L	L	t	н	Х	QBn	аcп	αpn	QEn	Q <sub>En</sub>	QGn	QHn	Н	QBn	H
	Н	Н	L	L	L.	1	L	х	QBn	$a_{Cn}$	αpn	ι	$a_{Fn}$	$a_{Gn}$	Q <sub>Hn</sub>	L	QBn	L
Load	H	Н	Н	×	×	†	×	×	a	ь	C	d	e	_ <del></del>	9	ħ	a	h

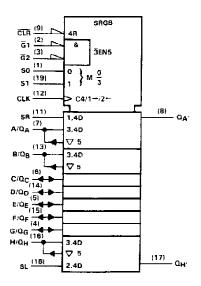
<sup>†</sup>When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.



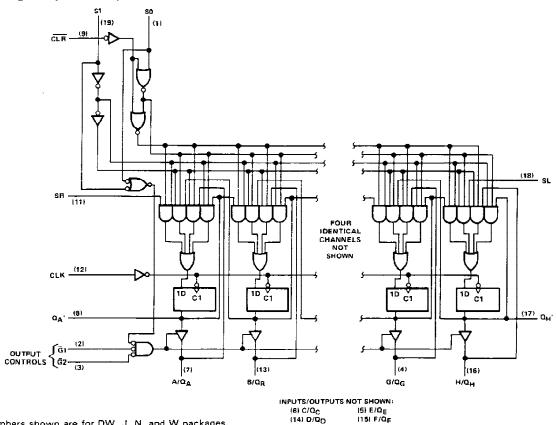
# SN54LS323, SN74LS323 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

#### logic symbol†



<sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

#### logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.



schematics of inputs and outputs, absolute maximum ratings, recommended operating conditions, and electrical characteristics

Same as SN54LS299 and SN74LS299, except  $t_{SU}$  (Clear Inactive) does not apply.

## switching characteristics, VCC = 5 V, $T_A = 25^{\circ}$ C

PARAMETER †	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN 25	TYP 35	MAX	UNIT
f <sub>max</sub>			See Note 1				
<sup>t</sup> PLH	CLK	QA' or QH'	C = 15 = 5		22	33	
<sup>‡</sup> PHL	CER	QA OI QH	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ		26	39	ns
<sup>t</sup> PLH	CLK	Q <sub>A</sub> thru Q <sub>H</sub>			17	25	
<sup>t</sup> PHL	GER	MA IIII CH	C -45 of D -605 O		25	39	ns
<sup>t</sup> PZH	<u>G</u> 1, <u>G</u> 2	Q <sub>A</sub> thru Q <sub>H</sub>	CL = 45 pF, R <sub>L</sub> = 665 Ω		14	21	
tPZL	41, 42	CA till CA			20	30	ns
<sup>t</sup> PHZ	Ğ1, Ğ2	Q <sub>A</sub> thru Q <sub>H</sub>	C E - B BE D		10	20	
tPLZ_		GA UIU CH	CL=5pF, RL=665Ω		10	15	ns

 $<sup>^{\</sup>dagger}$ t<sub>max</sub> = maximum clock frequency

tp\_H = Propagation delay time, low-to-high-level output

tpHL = Propagation delay time, high-to-low-level output

tpzH = Output enable time to high level

tpzL = Output enable time to low level

tpHZ = Output disable time from high level

tpLZ = Output disable time from low level

NOTE 1: For testing f<sub>max</sub>, all outputs are loaded simultaneously, each with C<sub>L</sub> and R<sub>L</sub> as specified for the propagation times. Load circuits and voltage waveforms are shown in Section 1.





ww.ti.com 7-Jun-2010

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN54LS323J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SN74LS323DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
SN74LS323DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
SN74LS323DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
SN74LS323DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	Samples Not Available
SN74LS323N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	Samples Not Available
SN74LS323N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS323FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
SNJ54LS323FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	Purchase Samples
SNJ54LS323J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54LS323J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	Purchase Samples
SNJ54LS323W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	Samples Not Available
SNJ54LS323W	OBSOLETE	CFP	W	20		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



### **PACKAGE OPTION ADDENDUM**

7-Jun-2010

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#### OTHER QUALIFIED VERSIONS OF SN54LS323, SN74LS323:

Military: SN54LS323

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

## 14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# W (R-GDFP-F20)

## CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20



# FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G20)

#### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



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