

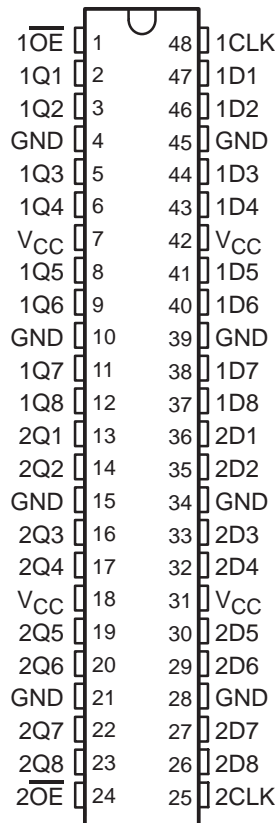
# SN54LVTH16374, SN74LVTH16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SCBS1450 – MAY 1992 – REVISED SEPTEMBER 2003

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH16374 . . . WD PACKAGE  
SN74LVTH16374 . . . DGG OR DL PACKAGE  
(TOP VIEW)



### description/ordering information

The 'LVTH16374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

### ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVTH16374DL	LVTH16374
		Tape and reel	SN74LVTH16374DLR	
	TSSOP – DGG	Tape and reel	SN74LVTH16374DGGR	LVTH16374
	VFBGA – GQL	Tape and reel	SN74LVTH16374GQLR	LL374
	VFBGA – ZQL (Pb-free)		SN74LVTH16374ZQLR	
–55°C to 125°C	CFP – WD	Tube	SNJ54LVTH16374WD	SNJ54LVTH16374WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# SN54LVTH16374, SN74LVTH16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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### description/ordering information (continued)

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

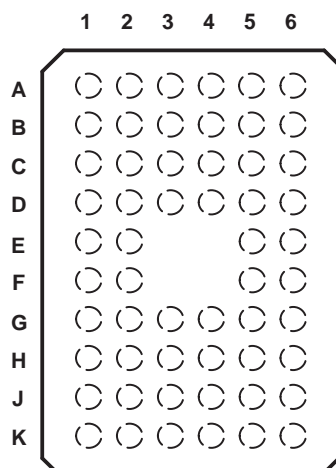
$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

#### GQL OR ZQL PACKAGE (TOP VIEW)

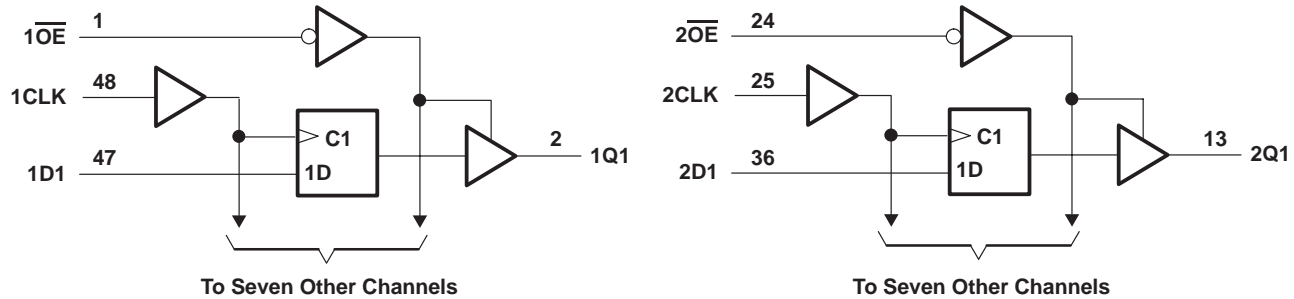


# SN54LVTH16374, SN74LVTH16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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### logic diagram (positive logic)



Pin numbers shown are for the DGG, DL, and WD packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$ : SN54LVTH16374	96 mA
SN74LVTH16374	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH16374	48 mA
SN74LVTH16374	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package	70°C/W
DL package	63°C/W
GQL/ZQL package	42°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

### recommended operating conditions (see Note 4)

		SN54LVTH16374		SN74LVTH16374		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16374			SN74LVTH16374			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = 2.7 V, I <sub>I</sub> = −18 mA		−1.2			−1.2			V
V <sub>OH</sub>		V <sub>CC</sub> = 2.7 V to 3.6 V, I <sub>OH</sub> = −100 μA		V <sub>CC</sub> −0.2			V <sub>CC</sub> −0.2			V
		V <sub>CC</sub> = 2.7 V, I <sub>OH</sub> = −8 mA		2.4			2.4			
		V <sub>CC</sub> = 3 V	I <sub>OH</sub> = −24 mA	2						
			I <sub>OH</sub> = −32 mA				2			
V <sub>OL</sub>		V <sub>CC</sub> = 2.7 V	I <sub>OL</sub> = 100 μA	0.2			0.2			V
			I <sub>OL</sub> = 24 mA	0.5			0.5			
		V <sub>CC</sub> = 3 V	I <sub>OL</sub> = 16 mA	0.4			0.4			
			I <sub>OL</sub> = 32 mA	0.5			0.5			
			I <sub>OL</sub> = 48 mA	0.55						
			I <sub>OL</sub> = 64 mA				0.55			
I <sub>I</sub>		V <sub>CC</sub> = 0 or 3.6 V, V <sub>I</sub> = 5.5 V		10			10			μA
	Control inputs	V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND		±1			±1			
	Data inputs	V <sub>CC</sub> = 3.6 V	V <sub>I</sub> = V <sub>CC</sub>	1			1			
			V <sub>I</sub> = 0	−5			−5			
I <sub>off</sub>		V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V					±100			μA
I <sub>I</sub> (hold)	Data inputs	V <sub>CC</sub> = 3 V	V <sub>I</sub> = 0.8 V	75			75			μA
			V <sub>I</sub> = 2 V	−75			−75			
		V <sub>CC</sub> = 3.6 V‡, V <sub>I</sub> = 0 to 3.6 V					±500			
I <sub>OZH</sub>		V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 3 V		5			5			μA
I <sub>OZL</sub>		V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0.5 V		−5			−5			μA
I <sub>OZPU</sub>		V <sub>CC</sub> = 0 to 1.5 V, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care		±100*			±100			μA
I <sub>OZPD</sub>		V <sub>CC</sub> = 1.5 V to 0, V <sub>O</sub> = 0.5 V to 3 V, OE = don't care		±100*			±100			μA
I <sub>CC</sub>		V <sub>CC</sub> = 3.6 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high	0.19			0.19			mA
			Outputs low	5			5			
			Outputs disabled	0.19			0.19			
ΔI <sub>CC</sub> §		V <sub>CC</sub> = 3 V to 3.6 V, One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>CC</sub> or GND		0.2			0.2			mA
C <sub>i</sub>		V <sub>I</sub> = 3 V or 0		3			3			pF
C <sub>O</sub>		V <sub>O</sub> = 3 V or 0		9			9			pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

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## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH16374				SN74LVTH16374				UNIT
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 ± 0.3 V		V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		160		160		160		160		MHz
t <sub>w</sub>	Pulse duration, CLK high or low		3		3		3		3		ns
t <sub>su</sub>	Setup time, data before CLK↑	High or low	2.9		3.3		1.8		2		ns
t <sub>h</sub>	Hold time, data after CLK↑	High or low	0.8		0.2		0.8		0.1		ns

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16374				SN74LVTH16374				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f <sub>max</sub>			160		160		160		160		MHz	
t <sub>PLH</sub>	CLK	Q	1.4	5.6	6.2		1.9	3	4.5	5.2		ns
t <sub>PHL</sub>			1.7	4.8	5		2.1	2.9	4	4.2		
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q	1	5.6	6.4		1.5	2.8	4.5	5.4		ns
t <sub>PZL</sub>			1.4	5.5	6.2		1.5	2.8	4.4	5		
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q	1	6.4	6.9		2.4	3.5	5	5.4		ns
t <sub>PLZ</sub>			1.7	5	5.2		2	3.2	4.6	4.8		
t <sub>sk(o)</sub>							0.5				ns	

$\dagger$  All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

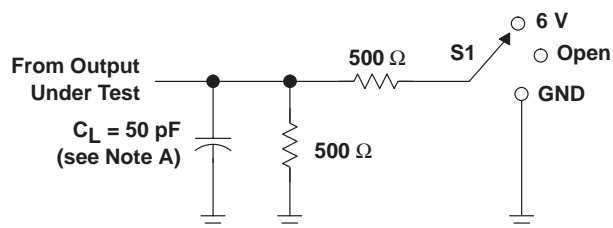
# SN54LVTH16374, SN74LVTH16374

## 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS

### WITH 3-STATE OUTPUTS

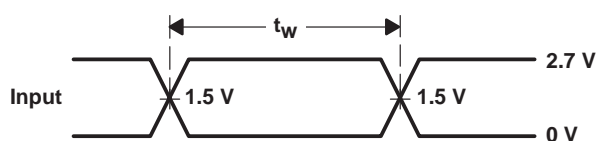
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#### PARAMETER MEASUREMENT INFORMATION

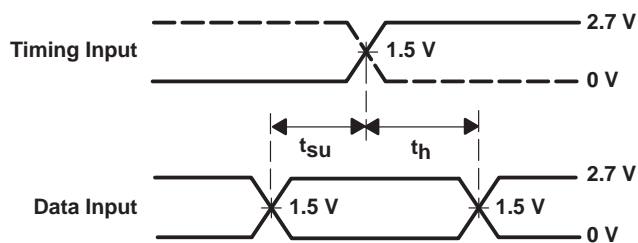


LOAD CIRCUIT

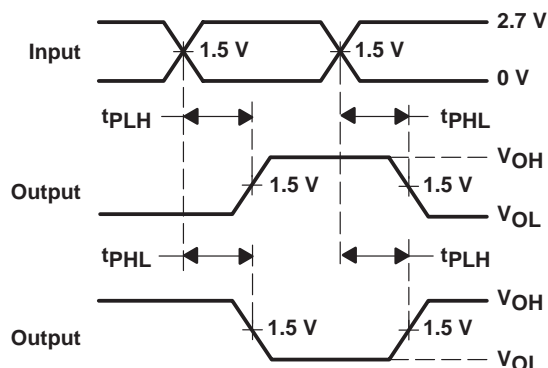
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



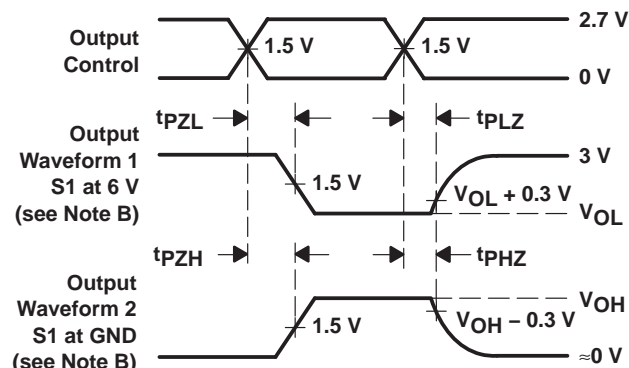
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

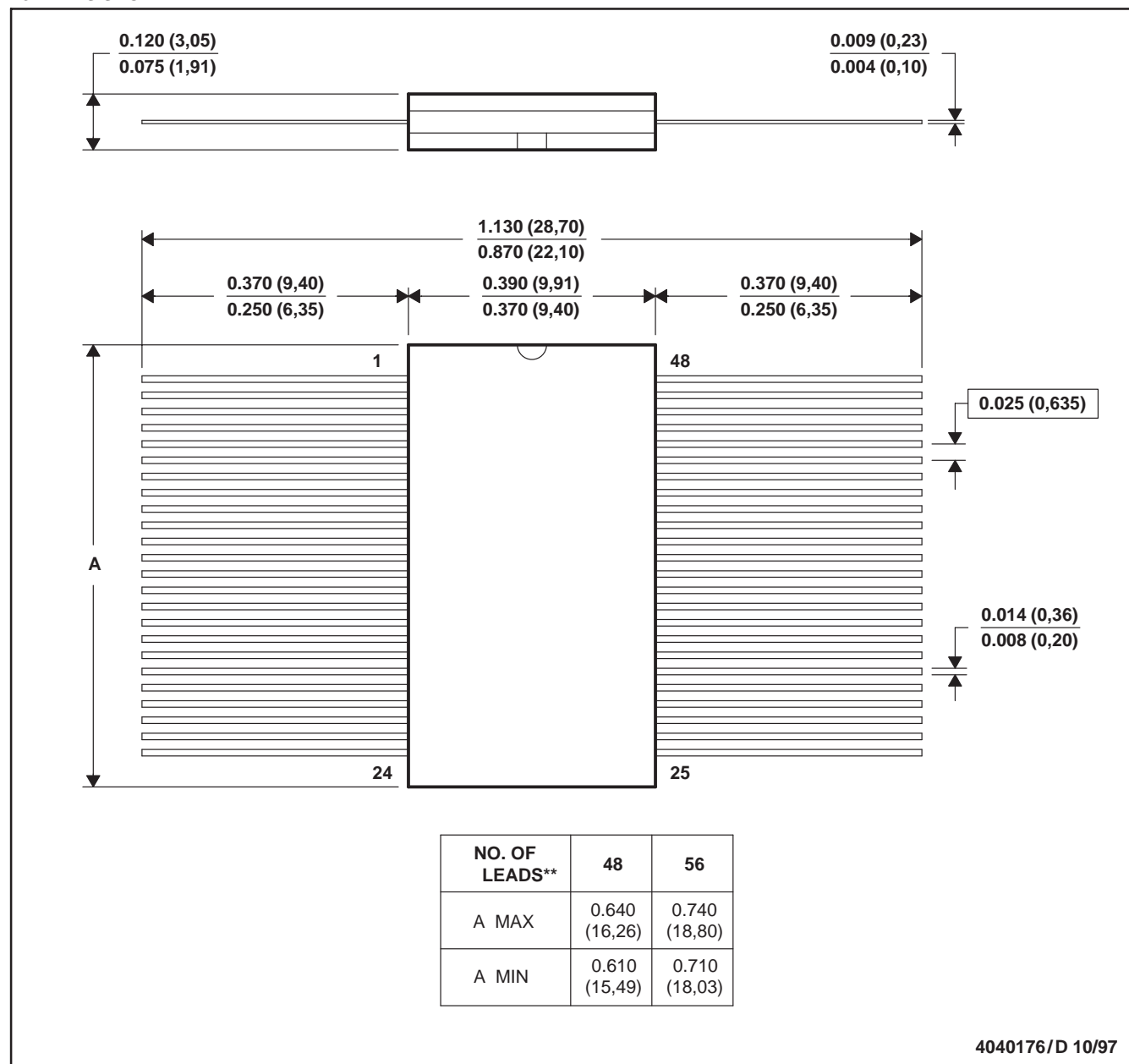
- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

## WD (R-GDFP-F\*\*)

## CERAMIC DUAL FLATPACK

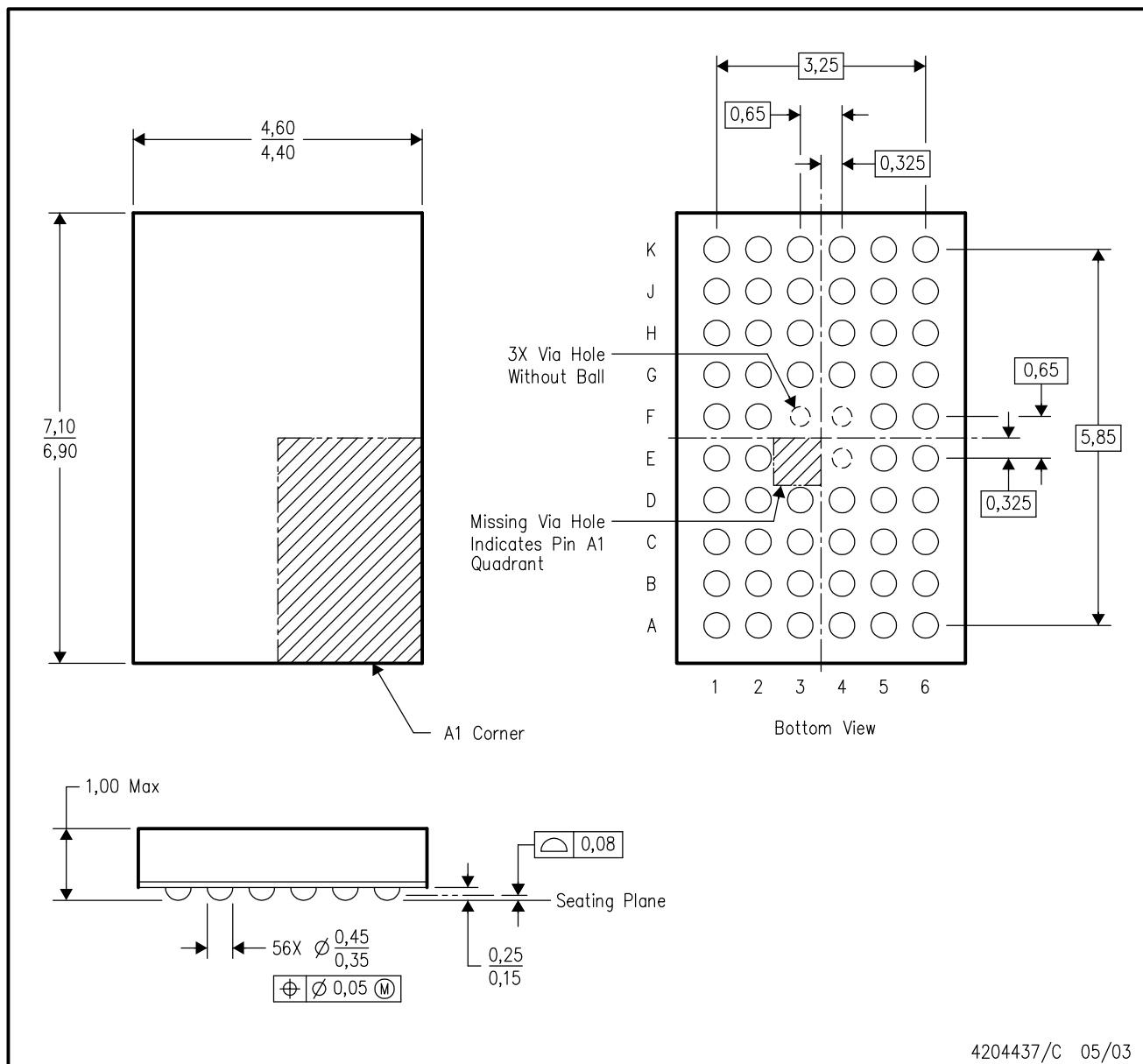
48 LEADS SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only
  - Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
GDFP1-F56 and JEDEC MO-146AB

## ZQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY

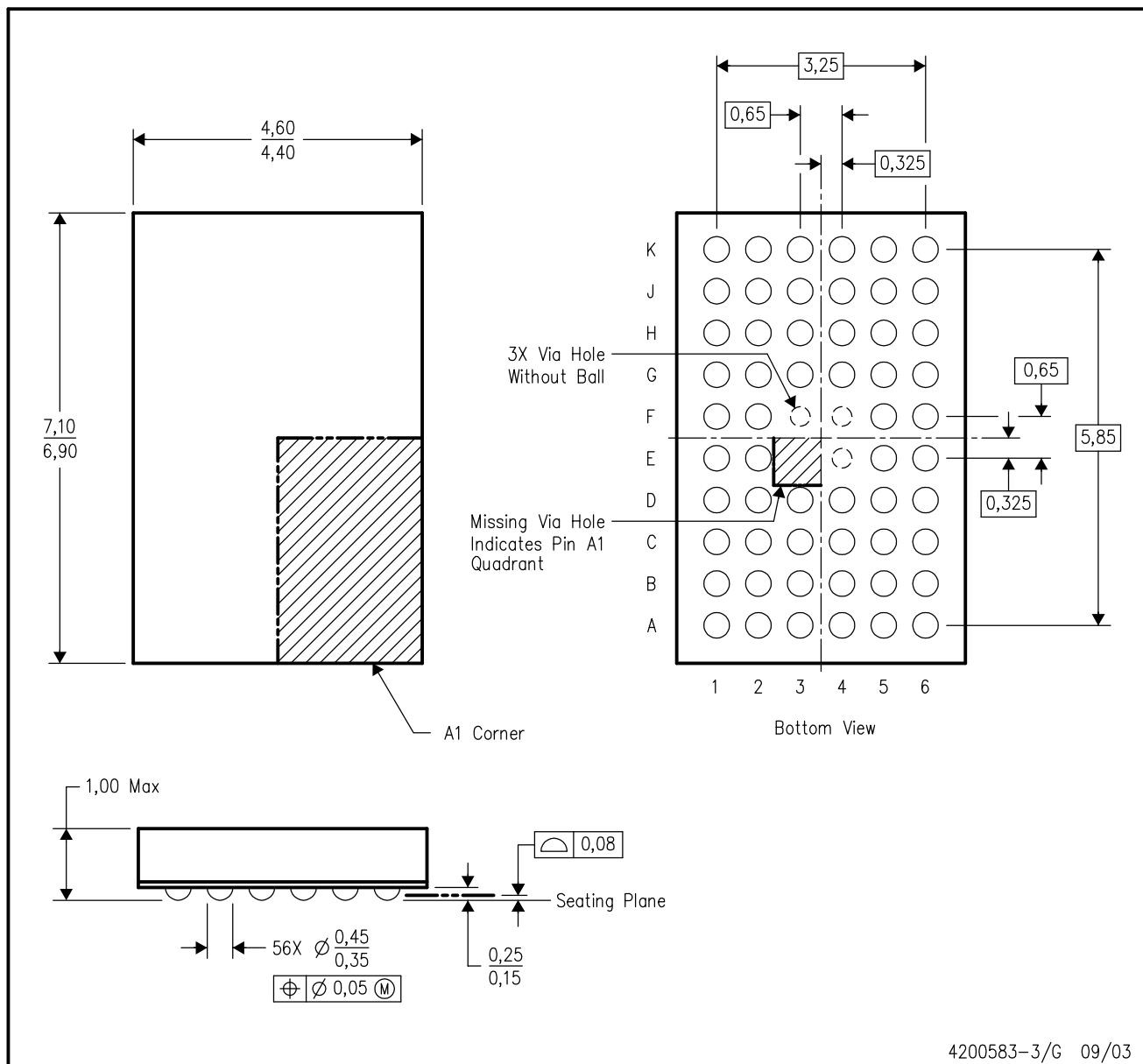


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - MicroStar Junior™ BGA configuration.
  - Falls within JEDEC MO-225 variation BA.
  - This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).



## GQL (R-PBGA-N56)

## PLASTIC BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - MicroStar Junior™ BGA configuration.
  - Falls within JEDEC MO-225 variation BA.
  - This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

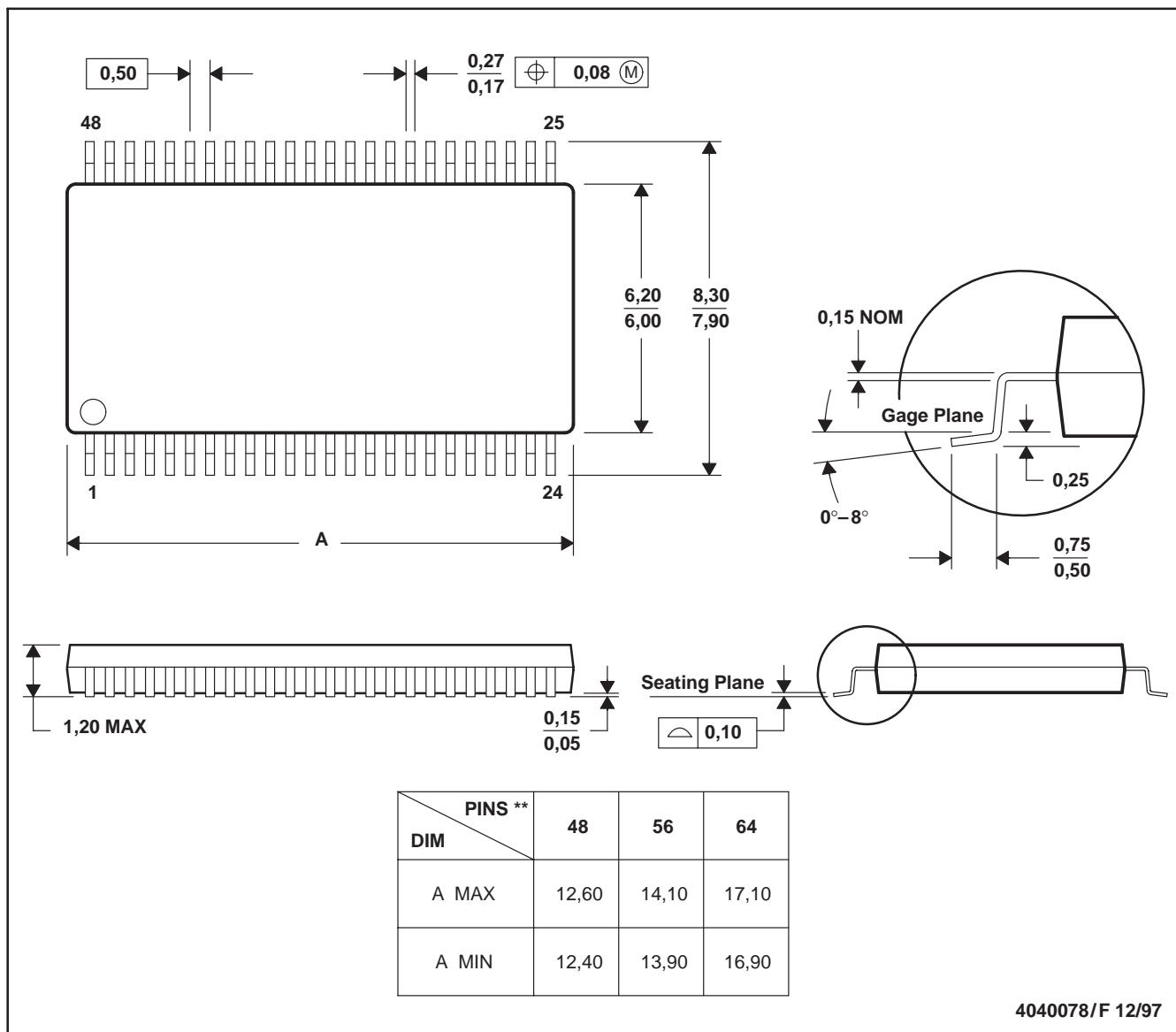


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

## DGG (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
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		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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