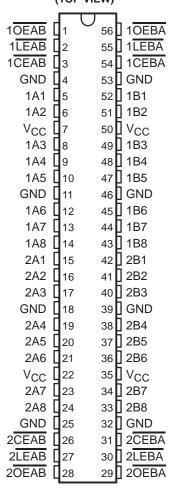
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- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation
- Members of the Texas Instruments Widebus™ Family
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
 < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors
- Support Live Insertion
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54LVT16543 . . . WD PACKAGE SN74LVT16543 . . . DGG OR DL PACKAGE (TOP VIEW)



description

The 'LVT16543 are 16-bit registered transceivers designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch-enable (\overline{LEAB} or \overline{LEAB}) and output-enable (\overline{OEAB} or \overline{OEBA}) inputs are provided for each register to permit independent control in either direction of data flow.

The A-to-B enable (CEAB) input must be low in order to enter data from A or to output data from B. If CEAB is low and LEAB is low, the A-to-B latches are transparent; a subsequent low-to-high transition of LEAB puts the A latches in the storage mode. With CEAB and OEAB both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the CEBA, LEBA, and OEBA inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.



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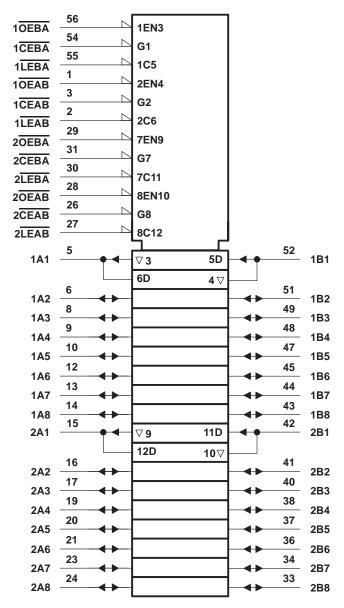
description (continued)

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT16543 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN54LVT16543 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVT16543 is characterized for operation from –40°C to 85°C.

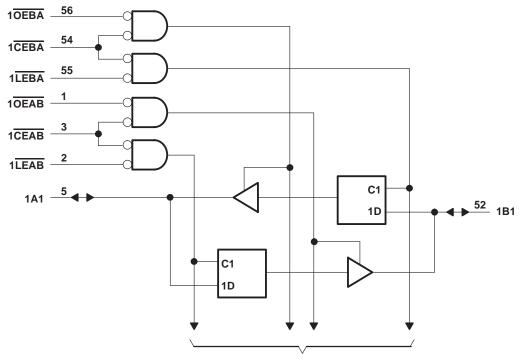
logic symbol†



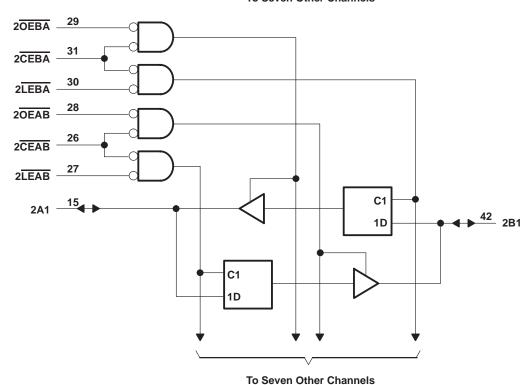
[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)



To Seven Other Channels



TEXAS INSTRUMENTS

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FUNCTION TABLE[†] (each 8-bit section)

	INPUTS								
CEAB	LEAB	OEAB	Α	В					
Н	Х	Χ	Χ	Z					
Х	Χ	Н	Χ	Z					
L	Н	L	Χ	в ₀ ‡					
L	L	L	L	L					
L	L	L	Н	Н					

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Supply voltage range, V _{CC} –0	5 \/ to 4 6 \/
Input voltage range, V _I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, VO (see Note 1)	-0.5 V to 7 V
Current into any output in the low state, IO: SN54LVT16543	96 mA
SN74LVT16543	128 mA
Current into any output in the high state, IO (see Note 2): SN54LVT16543	48 mA
SN74LVT16543	
Input clamp current, I_{IK} ($V_I < 0$)	50 mA
Output clamp current, I_{OK} ($V_O < 0$)	
Maximum power dissipation at T _A = 55°C (in still air) (see Note 3): DGG package	1 W
DL package	1.4 W
Storage temperature range, T _{stq} –65	

[§] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
 - 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions (see Note 4)

			SN54LV	T16543	SN74LV	T16543	
			MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage		2.7	3.6	2.7	3.6	V
VIH	High-level input voltage		2	FIN	2		V
VIL	Low-level input voltage			0.8		0.8	V
VI	Input voltage			5.5		5.5	V
IOH	High-level output current		Ç	-24		-32	mA
l _{OL}	Low-level output current		200	48		64	mA
Δt/Δν	Input transition rise or fall rate	Outputs enabled	BA	10		10	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: Unused control inputs must be held high or low to prevent them from floating.



[‡] Output level before the indicated steady-state input conditions were established

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	_	SN5	4LVT16	543	SN7	'4LVT16	543				
PARAMETER	"	EST CONDITIONS		MIN	TYP [†]	MAX	MIN	TYP [†]	MAX	UNIT	
VIK	$V_{CC} = 2.7 \text{ V},$	I _I = -18 mA				-1.2			-1.2	V	
	$V_{CC} = MIN \text{ to } MAX^{\ddagger},$	I _{OH} = -100 μA		VCC-C).2		VCC-0	.2			
.,	$V_{CC} = 2.7 \text{ V},$	I _{OH} = – 8 mA		2.4			2.4			V	
VOH		I _{OH} = - 24 mA	2						V		
	V _{CC} = 3 V	$I_{OH} = -32 \text{ mA}$				2					
	V 07V	I _{OL} = 100 μA				0.2			0.2		
	V _{CC} = 2.7 V	I _{OL} = 24 mA			0.5			0.5			
ļ ,,		I _{OL} = 16 mA				0.4			0.4		
V _{OL}	2.7	I _{OL} = 32 mA				0.5			0.5	V	
	V _{CC} = 3 V	I _{OL} = 48 mA	0.55]			
		I _{OL} = 64 mA				4			0.55		
	$V_{CC} = 3.6 \text{ V},$	$V_I = V_{CC}$ or GND	Octobel in sector		1	±1			±1		
	$V_{CC} = 0$ or MAX ‡ ,	V _I = 5.5 V	Control inputs		07.	10			10		
l _l	V _{CC} = 3.6 V	V _I = 5.5 V			6	20			20	μΑ	
		VI = VCC	A or B ports§		30	5			5		
		V _I = 0		0		-10			-10		
l _{off}	$V_{CC} = 0$,	V_{I} or $V_{O} = 0$ to 4.5	V	- V					±100	μΑ	
1	V 2 V	V _I = 0.8 V	A = D = = = = =	75			75			^	
l(hold)	VCC = 3 V	V _I = 2 V	A or B ports	-75			-75			μΑ	
lozh	$V_{CC} = 3.6 \text{ V},$	V _O = 3 V				1			1	μΑ	
lozL	$V_{CC} = 3.6 \text{ V},$	$V_0 = 0.5 V$				-1			-1	μΑ	
			Outputs high			0.12			0.12		
ICC	$V_{CC} = 3.6 \text{ V},$ $V_{I} = V_{CC} \text{ or GND}$	$I_O = 0$,	Outputs low			5			5	mA	
	V1 = VCC 01 014B	Outputs disabled			0.12			0.12	<u>. </u>		
ΔI _{CC} ¶	$V_{CC} = 3 \text{ V to } 3.6 \text{ V},$ Other inputs at V_{CC} or		– 0.6 V,			0.2			0.2	mA	
C _i	V _I = 3 V or 0				4			4		pF	
C _{io}	$V_O = 3 \text{ V or } 0$				13			13		pF	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C. ‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[§] Unused pins at V_{CC} or GND

This is the increase in supply current for each input that is at the specified TTL voltage level rather than VCC or GND.

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

					SN54LV	T16543		;	SN74LV	T16543			
				V _{CC} =		V _{CC} =	2.7 V	V _{CC} =		V _{CC} =	2.7 V	UNIT	
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_W	t _W Pulse duration, LEAB or LEBA low			3.3		3.3		3.3		3.3		ns	
		A or B before LEAB↑ or	Data high	0.8		0.5	,	0.8		0.5			
	Catua tima	LEBA↑	Data low	1.5		1.9		1.5		1.9		ns	
t _{su}	Setup time	A or B before CEAB↑ or CEBA↑	Data high	0.7		0.4		0.7		0.4			
			Data low	1.6		1.9		1.6		1.9		ns	
		A or B after LEAB↑ or	Data high	0.8	2/,	0		0.8		0			
4.	Hald Care	LEBA†	Data low	1.2	000	1.3		1.2		1.3		ns	
t _h Ho	Hoia time	Hold time A or B after CEAB↑ or	Data high	0.8	Q.	0		0.8		0			
		CEBA↑	Data low	1.3		1.4		1.3		1.4		ns	

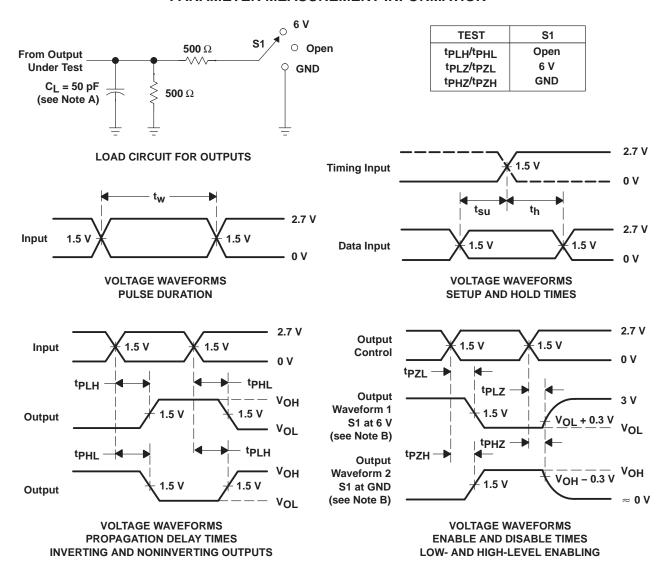
switching characteristics over recommended operating free-air temperature range, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

				SN54LV	T16543			SN7	4LVT16	543			
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V_{CC} = 3.3 V \pm 0.3 V		V	V _{CC} = 2.7 V		UNIT	
			MIN	MAX	MIN	MAX	MIN	TYP [†]	MAX	MIN	MAX		
t _{PLH}	A or D	D or A	1.4	5		5.8	1.4	2.7	4.6		5.5	20	
t _{PHL}	A or B	B or A	1.3	4.7		5.9	1.3	2.9	4.6		5.8	ns	
^t PLH	<u>LE</u>	A D	1.3	6.8	Mi	8.5	1.7	3.7	6.3		8.1		
t _{PHL}	LE	A or B	1.5	6.5	1/2	8.3	1.9	3.7	6		7.8	ns	
t _{PZH}	ŌĒ	A or B	1.4	6	<i>V</i> 0	7.7	1.5	3.3	5.8		7.6	ns	
t _{PZL}	OE		1.6	6.3		8.4	1.6	3.3	6.2		8.2		
t _{PHZ}	ŌĒ	A D	2	6.7		7.3	2	4.1	6.5		7.1		
t _{PLZ}	OE	A or B	2.7	6		6.2	2.7	3.9	5.8		5.9	ns	
^t PZH	CE	A D	1.4	6.2		7.7	1.5	3.3	6		7.6	ns	
t _{PZL}	CE	A or B	1.6	6.6		8.5	1.7	3.3	6.4		8.3		
t _{PHZ}	CE	A or P	2	6.6		7.2	2	4.1	6.4		7.1		
tPLZ	CE	A or B	2.6	5.6		5.9	2.6	4	5.4		5.6	ns	

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_Q = 50 \Omega$, $t_f \leq 2.5$ ns. $t_f \leq 2.5$ ns.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



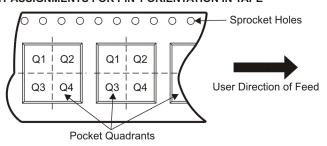
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

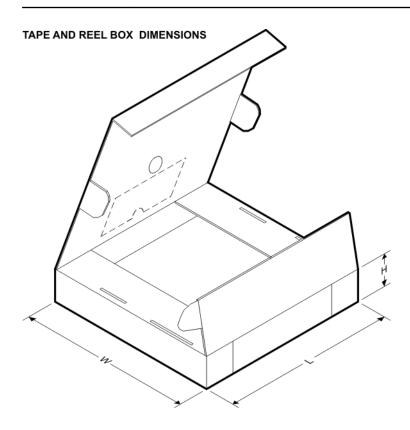
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

	Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ĺ	SN74LVT16543DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
	SN74LVT16543DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVT16543DGGR	TSSOP	DGG	56	2000	346.0	346.0	41.0
SN74LVT16543DLR	SSOP	DL	56	1000	346.0	346.0	49.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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