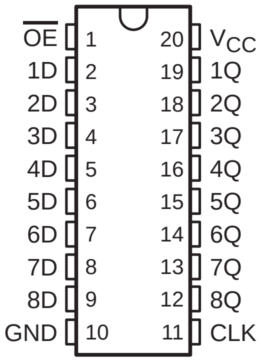
SN54LVC574A, SN74LVC574A
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

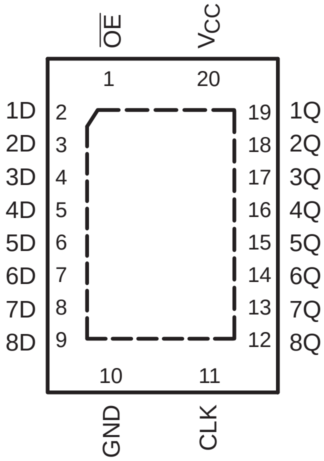
SCAS301Q − JANUARY 1993 − REVISED AUGUST 2003

- **Operate From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 7 ns at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

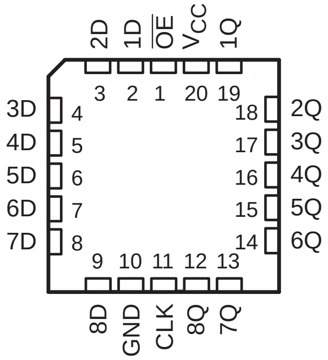
SN54LVC574A . . . J OR W PACKAGE
SN74LVC574A . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN74LVC574A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC574A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The SN54LVC574A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC574A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

description/ordering information (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

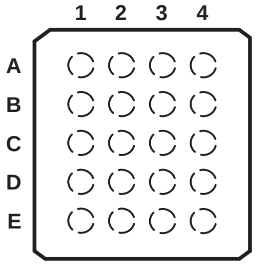
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP − N	Tube of 20	SN74LVC574AN	SN74LVC574AN
	QFN − RGY	Reel of 1000	SN74LVC574ARGYR	LC574A
	SOIC − DW	Tube of 25	SN74LVC574ADW	LVC574A
		Reel of 2000	SN74LVC574ADWR	
	SOP − NS	Reel of 2000	SN74LVC574ANSR	LVC574A
	SSOP − DB	Reel of 2000	SN74LVC574ADBR	LC574A
	TSSOP − PW	Tube of 70	SN74LVC574APW	LC574A
		Reel of 2000	SN74LVC574APWR	
		Reel of 250	SN74LVC574APWT	
	TVSOP − DGV	Reel of 2000	SN74LVC574ADGVR	LC574A
	VFBGA − GQN	Reel of 1000	SN74LVC574AGQNR	LC574A
	VFBGA − ZQN (Pb-free)		SN74LVC574AZQNR	
−55°C to 125°C	CDIP − J	Tube of 20	SNJ54LVC574AJ	SNJ54LVC574AJ
	CFP − W	Tube of 85	SNJ54LVC574AW	SNJ54LVC574AW
	LCCC − FK	Tube of 55	SNJ54LVC574AFK	SNJ54LVC574AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GQN OR ZQN PACKAGE
(TOP VIEW)



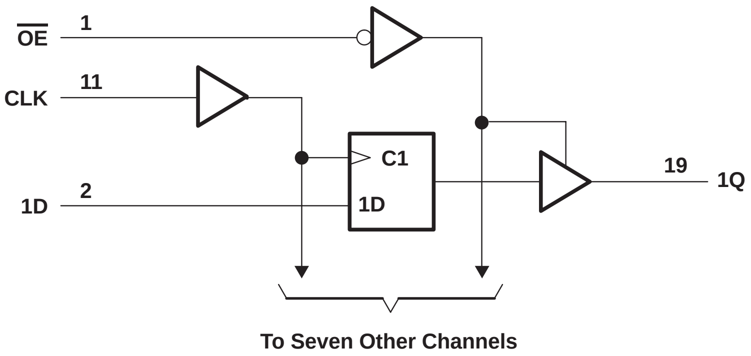
terminal assignments

	1	2	3	4
A	1D	$\overline{OE}$	V_{CC}	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	CLK	8Q

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Output clamp current, I_{OK} ($V_O < 0$)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DGV package	92°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN/ZQN package	78°C/W
(see Note 3): N package	69°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LVC574A		SN74LVC574A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V			0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V			1.7		
		V_{CC} = 2.7 V to 3.6 V	2		2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V				0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V				0.7	
		V_{CC} = 2.7 V to 3.6 V		0.8		0.8	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V				−4	mA
		V_{CC} = 2.3 V				−8	
		V_{CC} = 2.7 V		−12		−12	
		V_{CC} = 3 V		−24		−24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V				4	mA
		V_{CC} = 2.3 V				8	
		V_{CC} = 2.7 V		12		12	
		V_{CC} = 3 V		24		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			6		6	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	SN54LVC574A MIN	SN54LVC574A TYP†	SN54LVC574A MAX	SN74LVC574A MIN	SN74LVC574A TYP†	SN74LVC574A MAX	UNIT
V_{OH}	I_{OH} = −100 μA		1.65 V to 3.6 V				V_{CC}−0.2			V
			2.7 V to 3.6 V	V_{CC}−0.2						
	I_{OH} = −4 mA		1.65 V				1.2			
	I_{OH} = −8 mA		2.3 V				1.7			
	I_{OH} = −12 mA		2.7 V	2.2			2.2			
			3 V	2.4			2.4			
	I_{OH} = −24 mA		3 V	2.2			2.2			
V_{OL}	I_{OL} = 100 μA		1.65 V to 3.6 V						0.2	V
			2.7 V to 3.6 V			0.2				
	I_{OL} = 4 mA		1.65 V						0.45	
	I_{OL} = 8 mA		2.3 V						0.7	
	I_{OL} = 12 mA		2.7 V			0.4			0.4	
	I_{OL} = 24 mA		3 V			0.55			0.55	
I_I	V_I = 0 to 5.5 V		3.6 V			±5			±5	μA
I_{off}	V_I or V_O = 5.5 V		0						±10	μA
I_{OZ}	V_O = 0 to 5.5 V		3.6 V			±15			±10	μA
I_{CC}	$V_I = V_{CC}$ or GND	I_O = 0	3.6 V			10			10	μA
	$3.6 \text{ V} \le V_I \le 5.5 \text{ V}$‡					10			10	
ΔI_{CC}	One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND		2.7 V to 3.6 V			500			500	μA
C_i	$V_I = V_{CC}$ or GND		3.3 V		4			4		pF
C_o	$V_O = V_{CC}$ or GND		3.3 V		5.5			5.5		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This applies in the disabled state only.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVC574A V_{CC} = 2.7 V MIN	SN54LVC574A V_{CC} = 2.7 V MAX	SN54LVC574A V_{CC} = 3.3 V ± 0.3 V MIN	SN54LVC574A V_{CC} = 3.3 V ± 0.3 V MAX	UNIT
f_{clock}	Clock frequency		150		150	MHz
t_w	Pulse duration, CLK high or low	3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	2		2		ns
t_h	Hold time, data after CLK↑	2		2		ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN74LVC574A								UNIT
		V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		55		95		150		150	MHz
t_w	Pulse duration, CLK high or low	9		4		3.3		3.3		ns
t_{su}	Setup time, data before CLK↑	6		4		2		2		ns
t_h	Hold time, data after CLK↑	4		2		1.5		1.5		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC574A				UNIT
			V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{pd}	CLK	Q		8	1	7	ns
t_{en}	$\overline{OE}$	Q		9	1	7.5	ns
t_{dis}	$\overline{OE}$	Q		7	0.5	6.4	ns

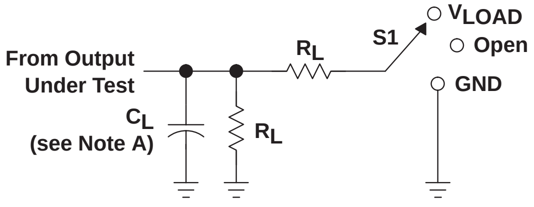
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC574A								UNIT
			V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			55		95		150		150		MHz
t_{pd}	CLK	Q	1	21.6	1	10.5	1	8	2.2	7	ns
t_{en}	$\overline{OE}$	Q	1	19.5	1	10.5	1	8.5	1.5	7.5	ns
t_{dis}	$\overline{OE}$	Q	1	18.8	1	7.8	1	7	1.7	6.4	ns
$t_{sk(o)}$										1	ns

operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	f = 10 MHz	67	60	43	pF
		Outputs disabled		9	9	15	

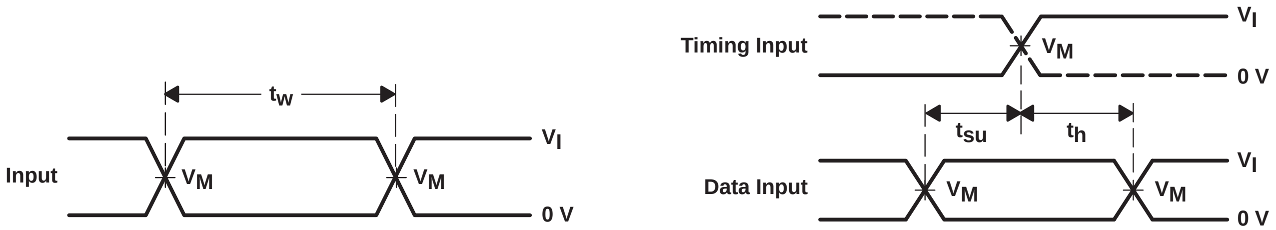
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

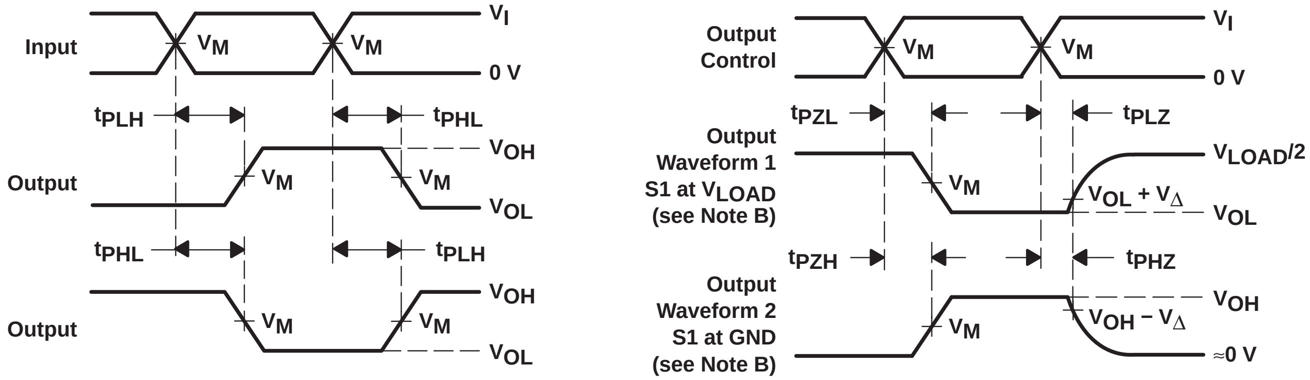
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

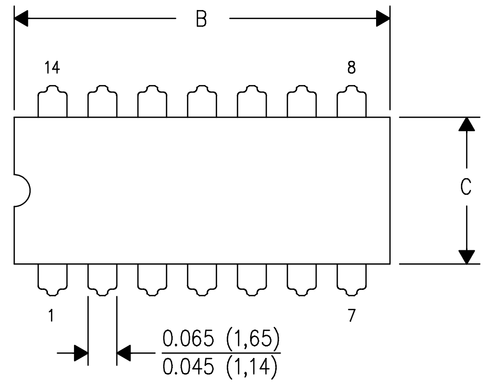
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

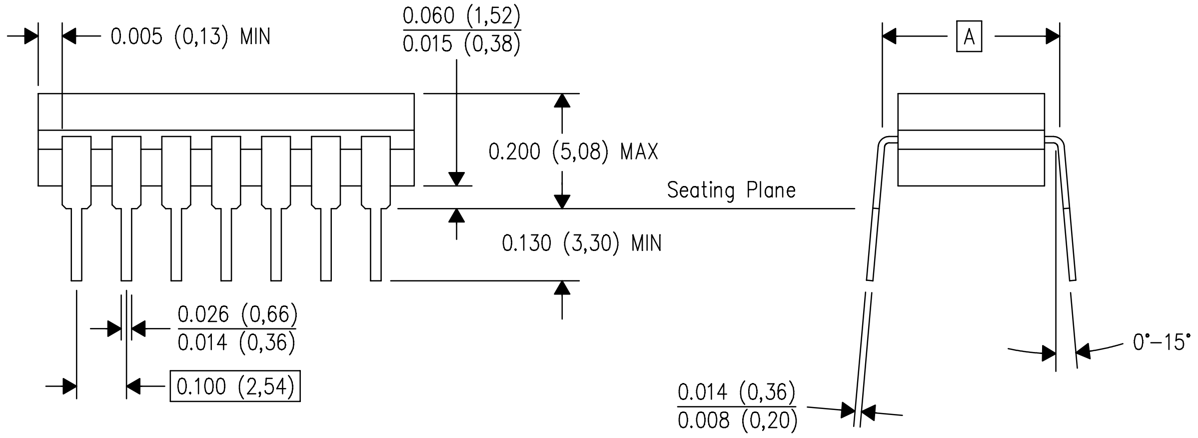
Figure 1. Load Circuit and Voltage Waveforms

J (R–GDIP–T**) CERAMIC DUAL IN–LINE PACKAGE

14 LEADS SHOWN



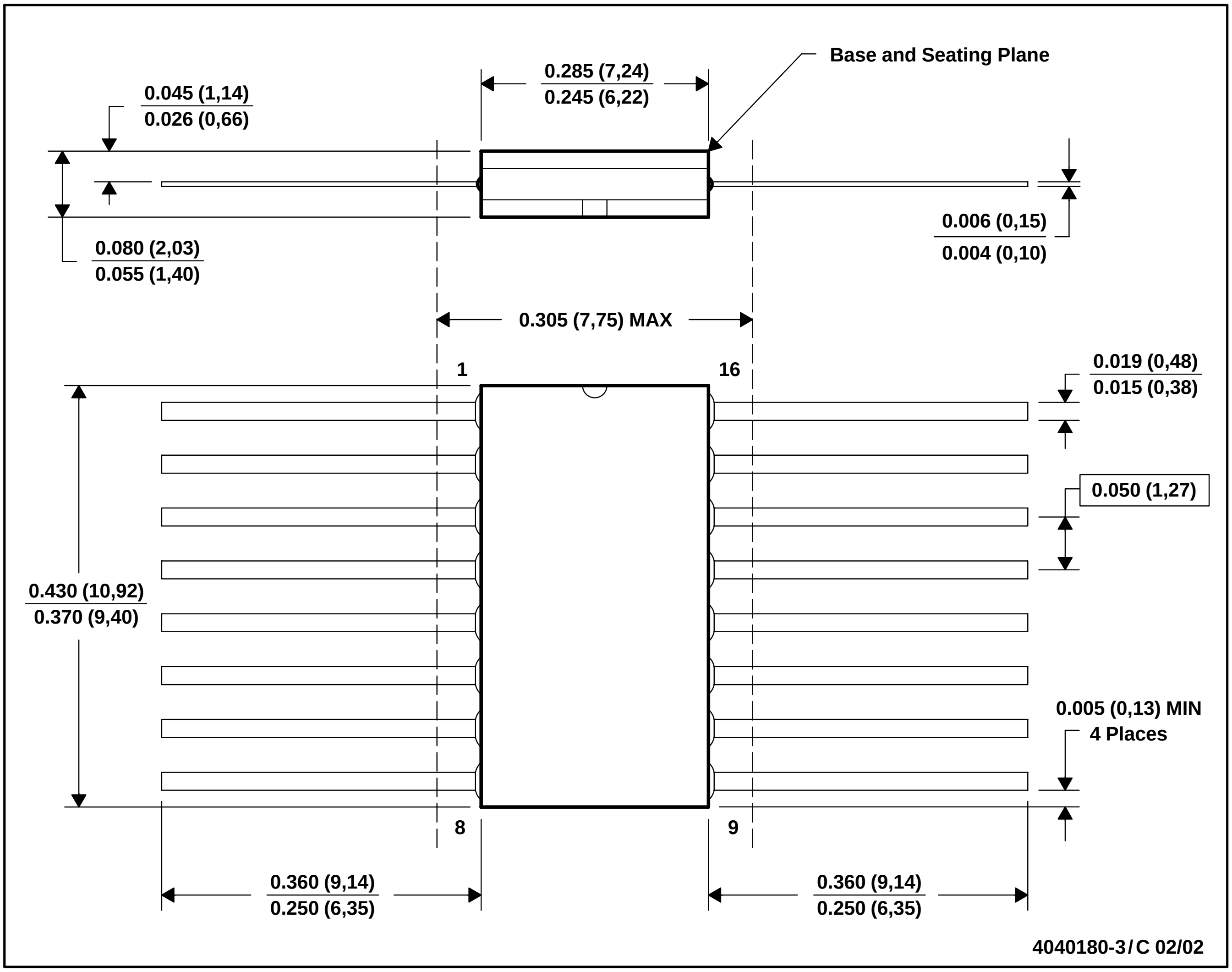
PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

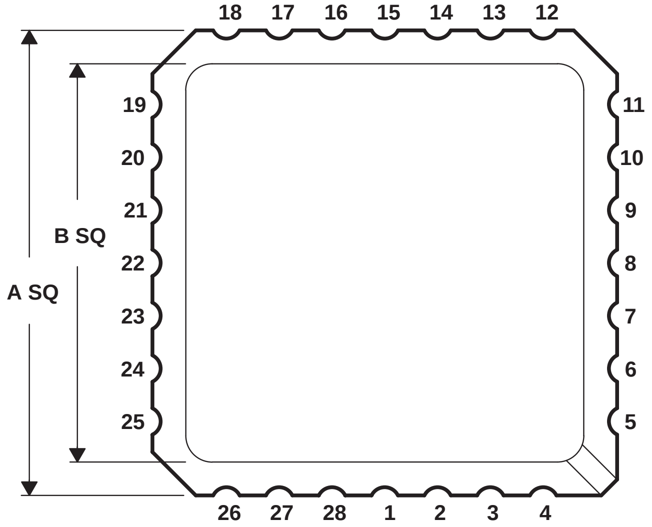
W (R-GDFP-F16) **CERAMIC DUAL FLATPACK**



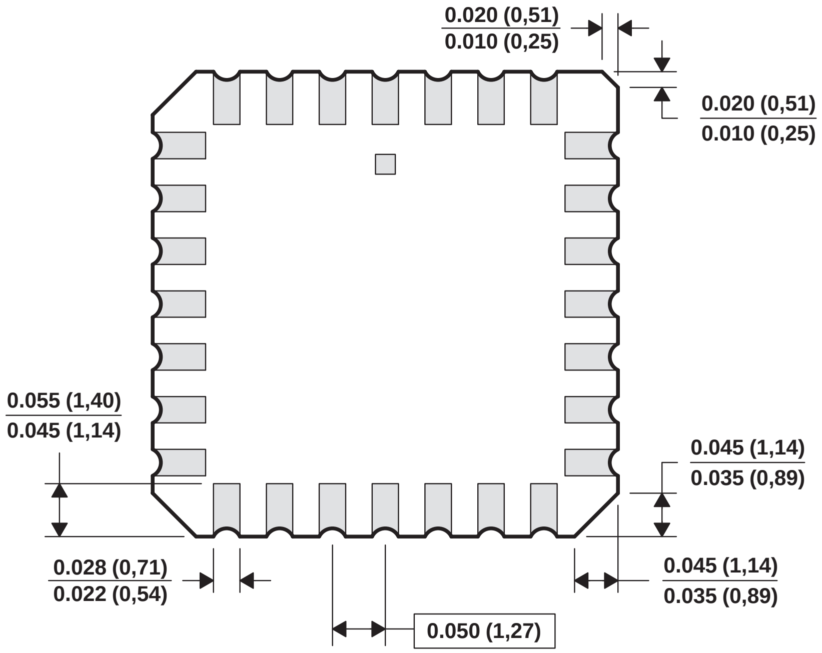
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP-1F16 and JEDEC MO-092AC

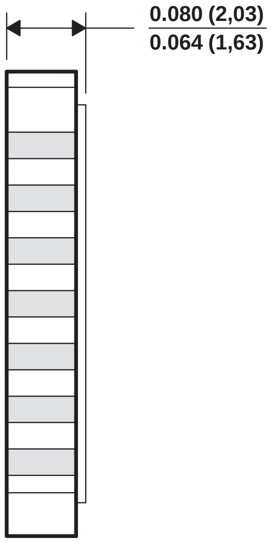
FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

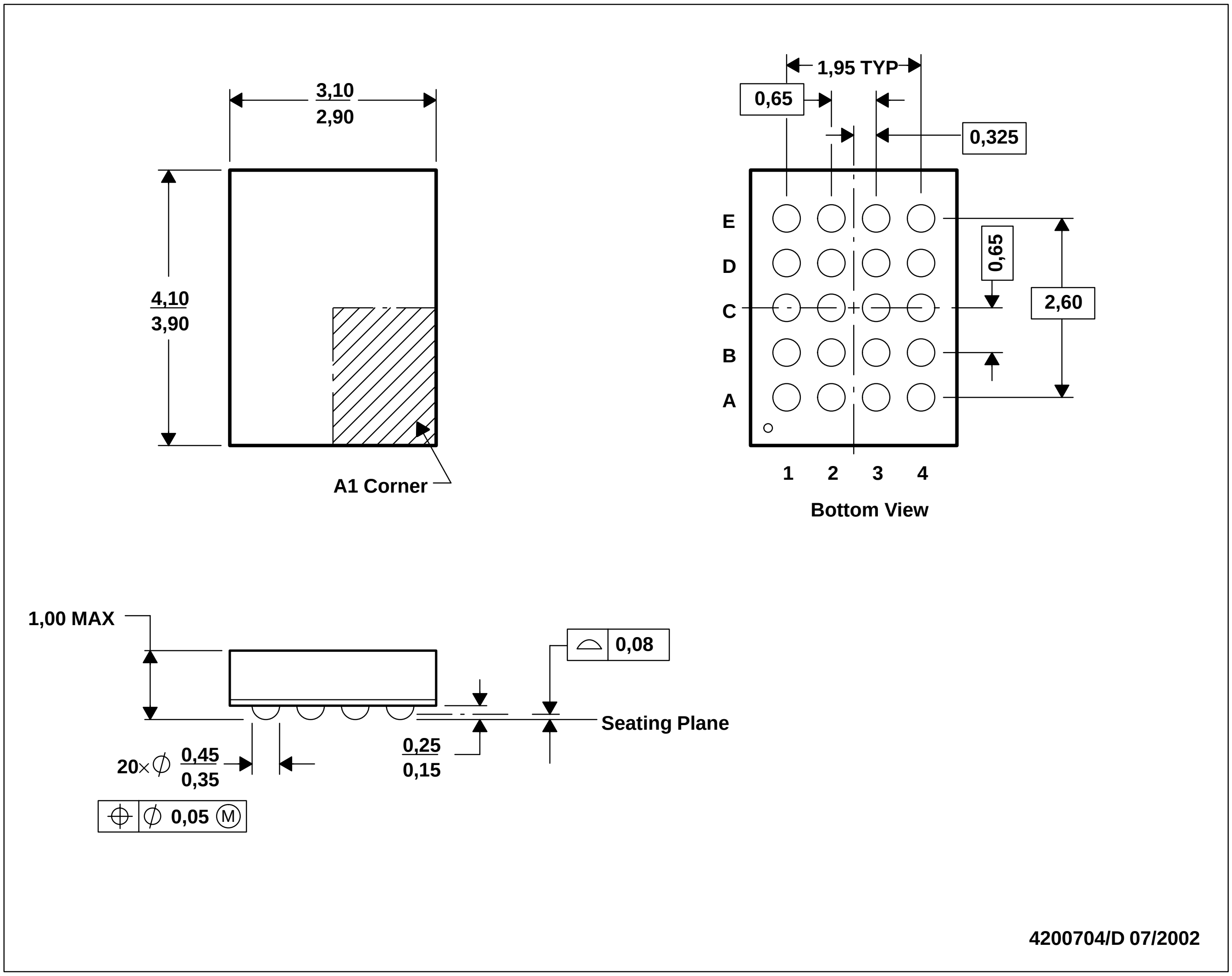




4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

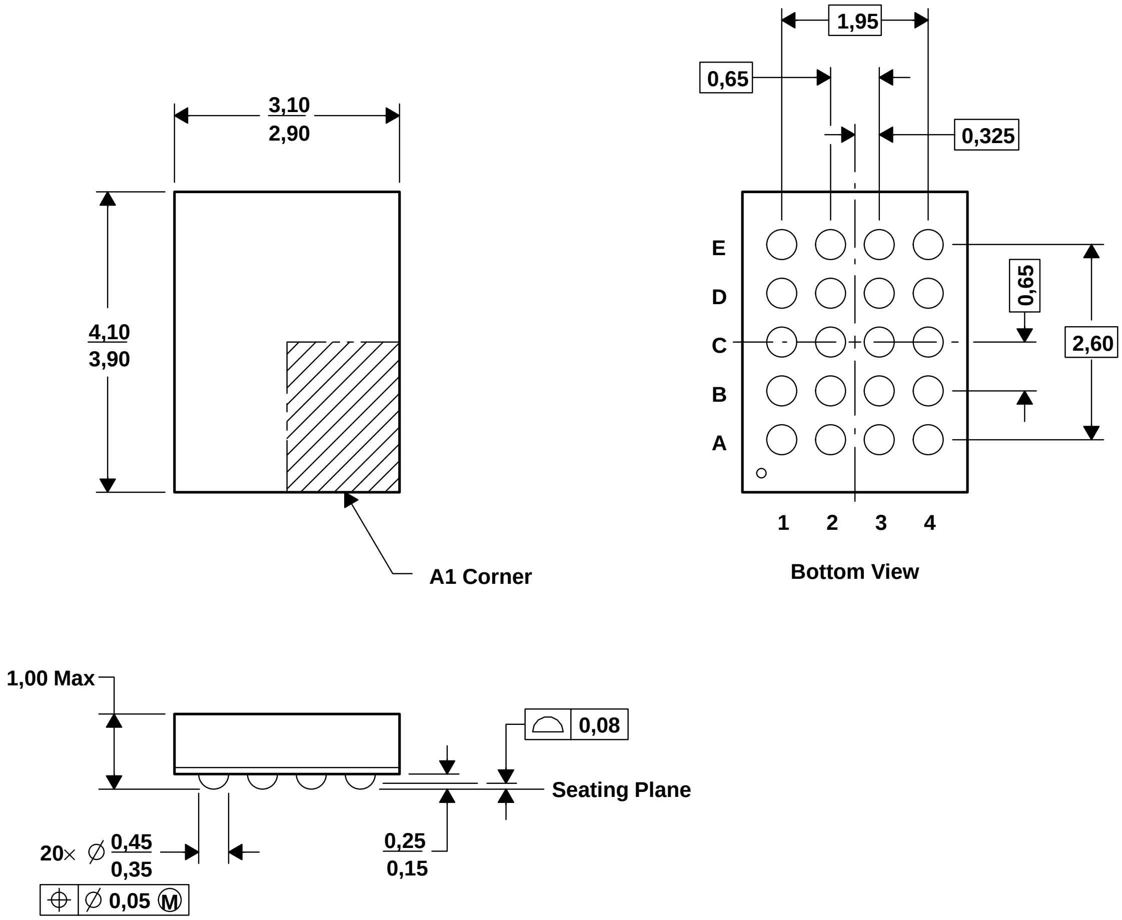
GQN (R-PBGA-N20) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ configuration
- D. Falls within JEDEC MO-225 variation BC.
- E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

MicroStar Junior is a trademark of Texas Instruments.

ZQN (R-PBGA-N20) **PLASTIC BALL GRID ARRAY**



4204492/A 06/2002

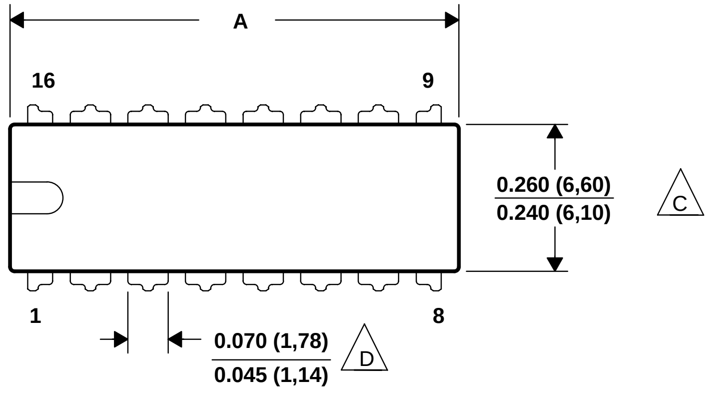
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. MicroStar Junior™ configuration.
- D. Fall within JEDEC MO-225 variation BC.
- E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead)SnPb).

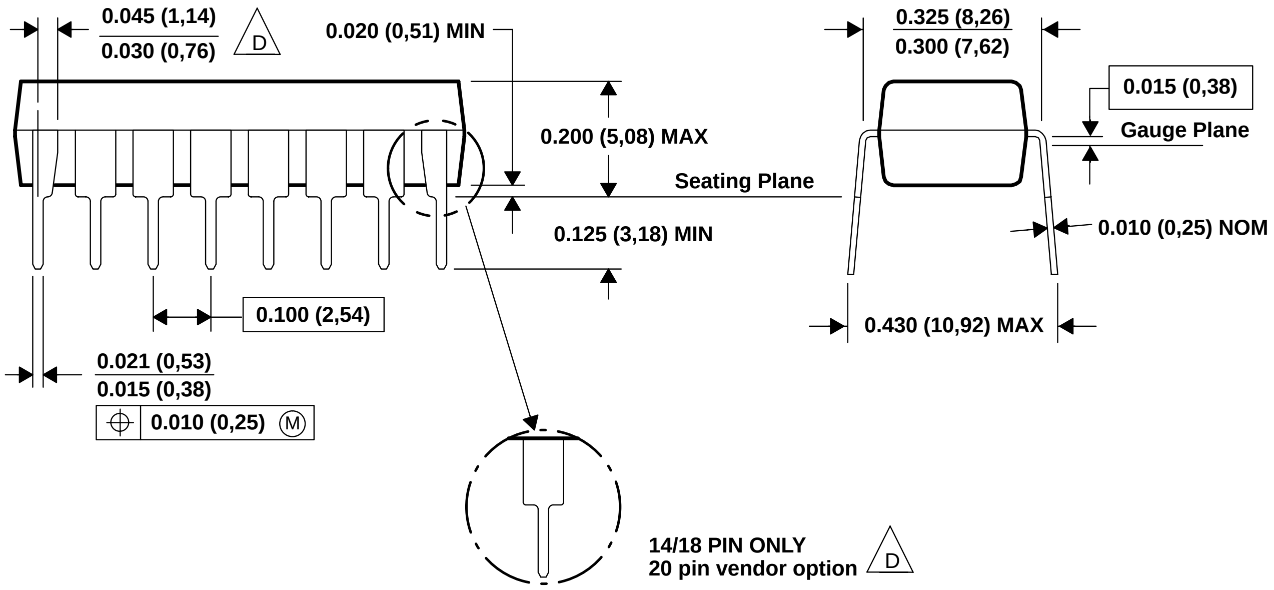
MicroStar Junior is a trademark of Texas Instruments.

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD



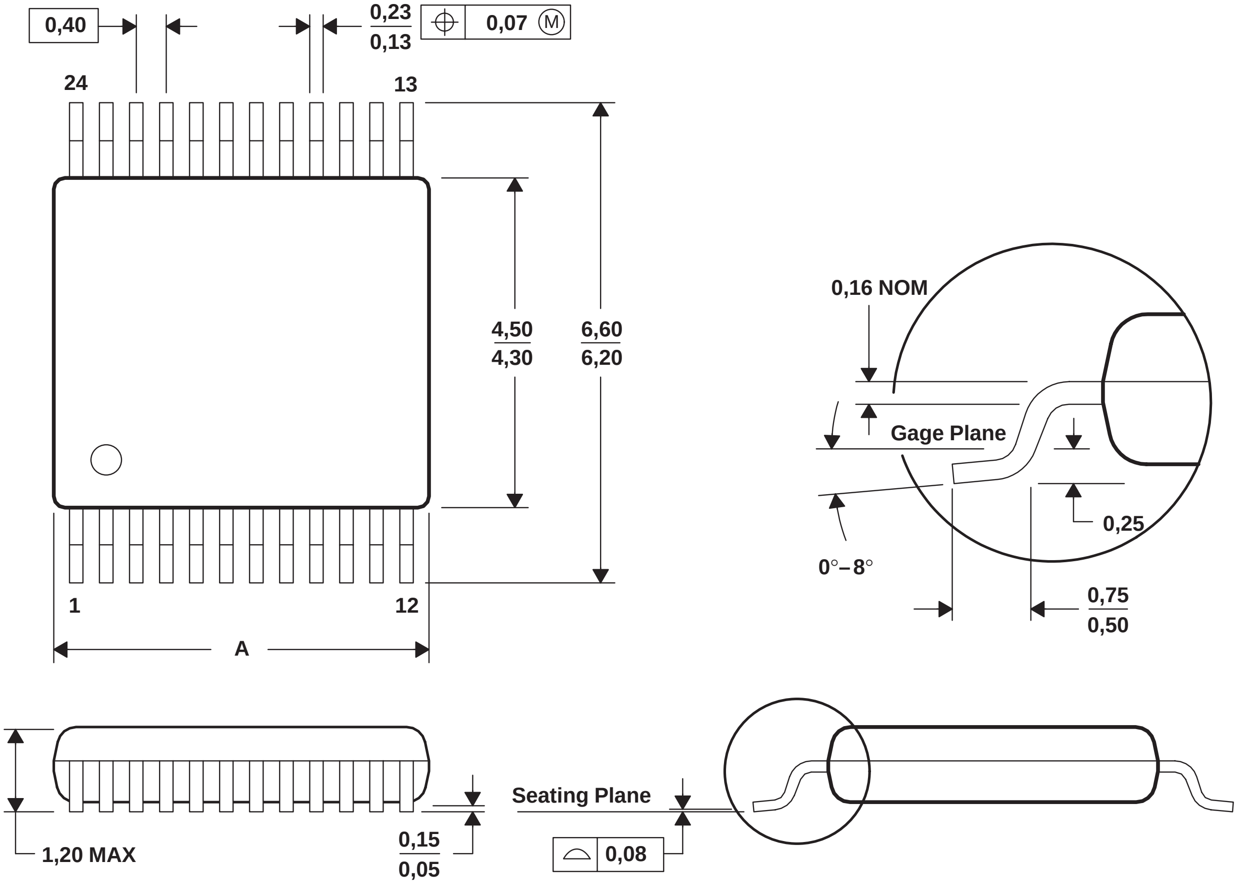


4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE

24 PINS SHOWN

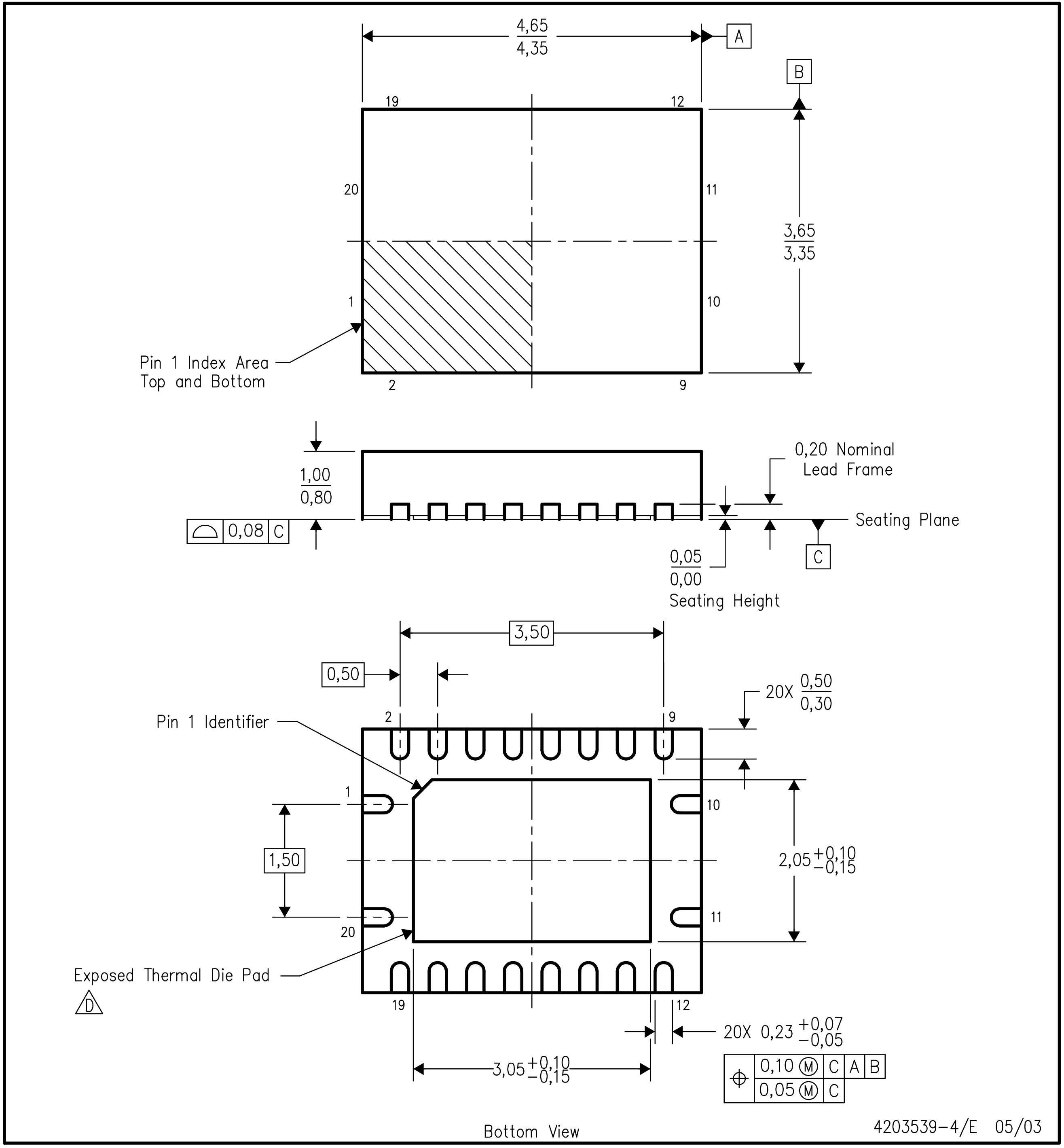


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK

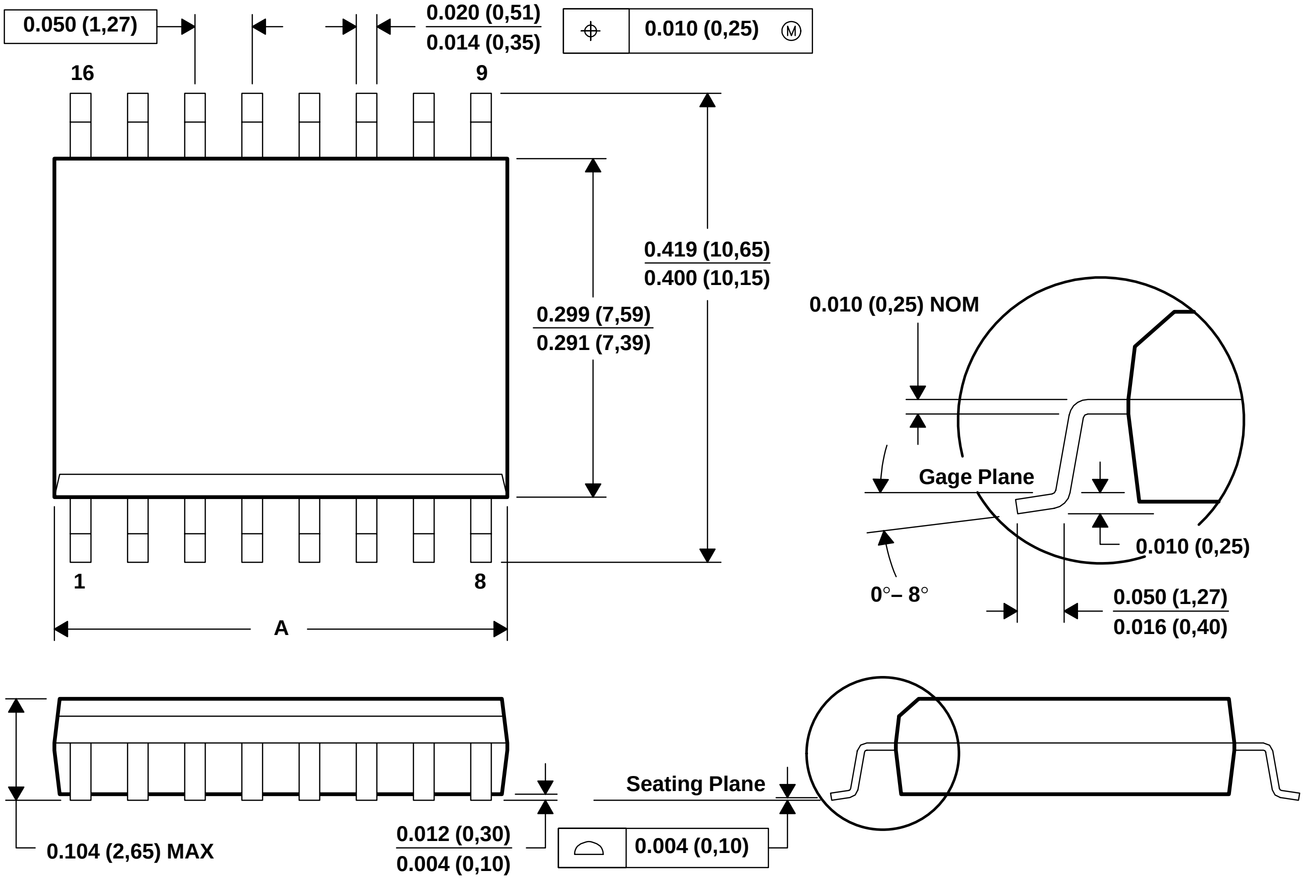


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- △D The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
- E. Package complies to JEDEC MO–241 variation BC.

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



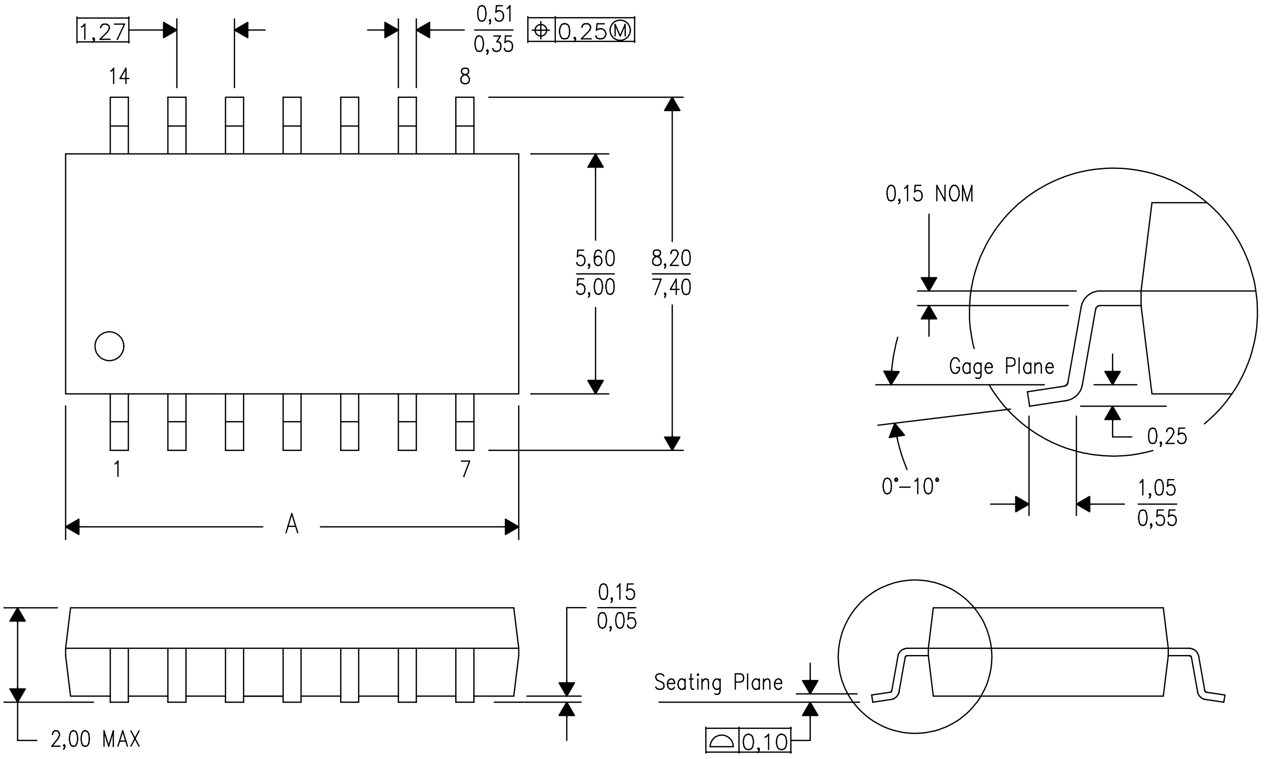
PINS ** DIM	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013

NS (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



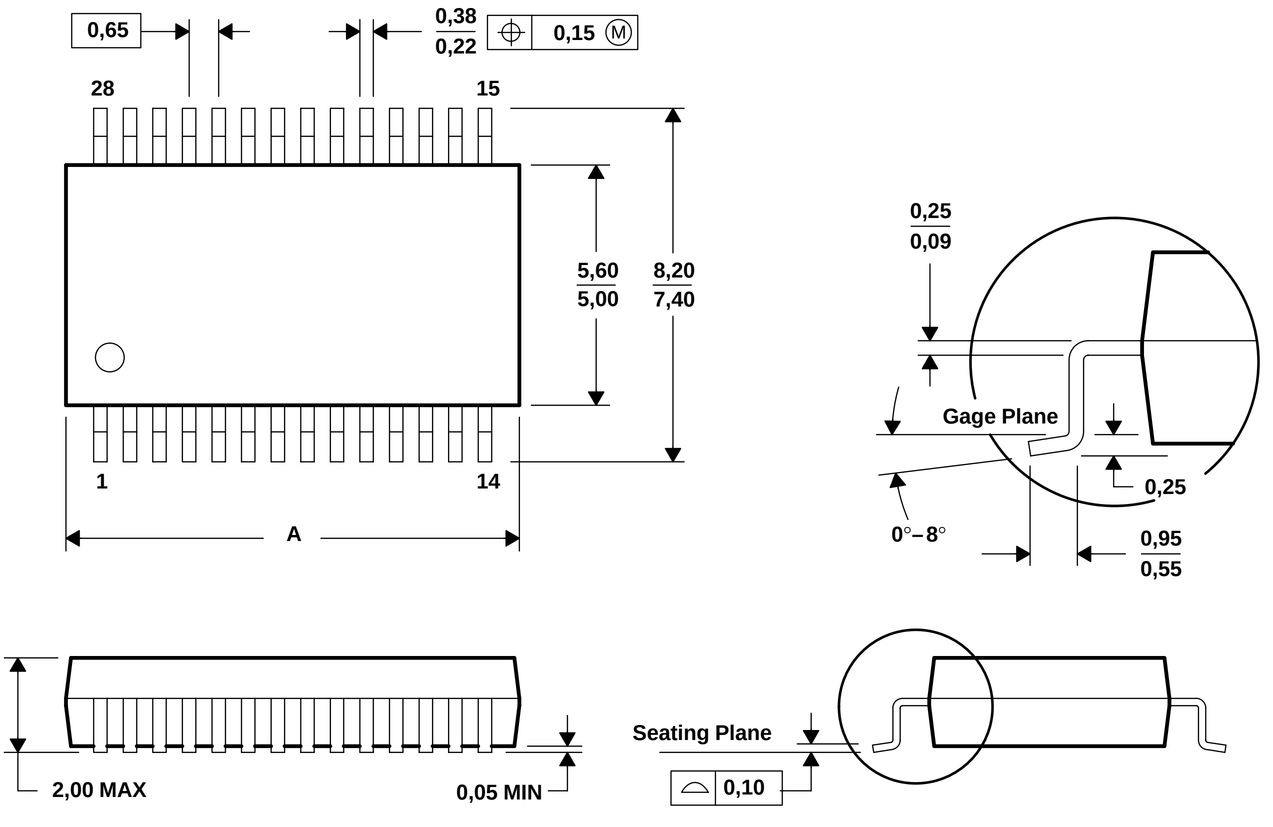
PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



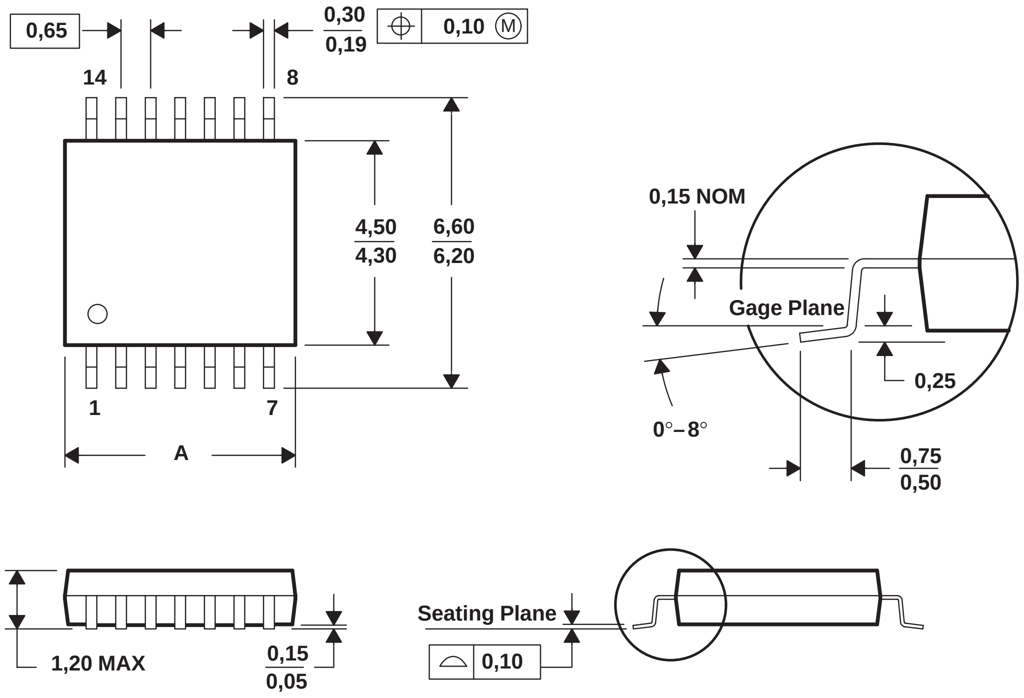
PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

PW (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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