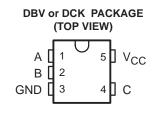
SCES499D - OCTOBER 2003 - REVISED JANUARY 2008

- Qualified for Automotive Applications
- 1.65-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns (V_{CC} = 3 V, C_L = 50 pF)
- Low On-State Resistance, Typically \approx 5.5 Ω (V_{CC} = 4.5 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78. Class II



description/ordering information

This single analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G66 can handle both analog and digital signals. The device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction.

Applications include signal gating, chopping, modulation or demodulation (modem), and signal multiplexing for analog-to-digital and digital-to-analog conversion systems.

ORDERING INFORMATION†

TA	PACKAGE‡	PACKAGE [‡]		TOP-SIDE MARKING§
-40°C to 125°C	SOT (SOT-23) – DBV	Reel of 3000	1P1G66QDBVRQ1	C66_
-40 C to 125°C	SOT (SOT-70) - DCK	Reel of 3000	1P1G66QDCKRQ1	C6_

[†] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

FUNCTION TABLE

CONTROL INPUT (C)	SWITCH
L	OFF
Н	ON



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



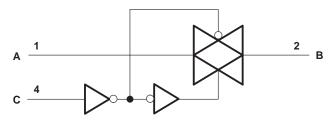
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[‡] Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

[§] The actual top-side marking has one additional character that designates the wafer fab/assembly site.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC} (see Note 1)	
Switch I/O voltage range, V _{I/O} (see Notes 1, 2, and 3)	
Control input clamp current, I_{IK} ($V_I < 0$)	
I/O port diode current, I_{IOK} ($V_{I/O}$ < 0)	–50 mA
On-state switch current, $I_T (V_{I/O} = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V _{CC} or GND	
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	
ESD rating, HBM (see Note 5)	2 (H2) kV
ESD rating, CDM (see Note 5)	1 (C5) kV
ESD rating, MM (see Note 5)	200 (M3) V
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
 - 2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 - 3. This value is limited to 5.5 V maximum.
 - 4. The package thermal impedance is calculated in accordance with JESD 51-7.
 - 5. ESD Protection Level per AEC Q100 classification.



recommended operating conditions (see Note 5)

			MIN	MAX	UNIT	
Vcc	Supply voltage		1.65	5.5	V	
V _{I/O}	I/O port voltage		0	Vcc	V	
		V _{CC} = 1.65 V to 1.95 V	V _{CC} × 0.65			
, ,	LPak basel Sanat sellana sanatal Sanat	V _{CC} = 2.3 V to 2.7 V	V _{CC} ×0.7		.,	
V _{IH} High-level input voltage, control input	V _{CC} = 3 V to 3.6 V	V _{CC} ×0.7		V		
		V _{CC} = 4.5 V to 5.5 V	V _{CC} ×0.7			
	Low-level input voltage, control input	V _{CC} = 1.65 V to 1.95 V		V _{CC} × 0.35		
1		V _{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		
VIL		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		$V_{CC} \times 0.3$		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$		
٧ _I	Control input voltage		0	5.5	V	
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		20		
44/4	han at the position via a Mall time	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		20		
Δt/Δv	Input transition rise/fall time	V _{CC} = 3 V to 3.6 V		10	ns/V	
		V _{CC} = 4.5 V to 5.5 V		10		
TA	Operating free-air temperature		-40	125	°C	

NOTE 6: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		VCC	MIN TYPT	MAX	UNIT
			$I_S = 4 \text{ mA}$	1.65 V	12	35	
_	On atota assistata and	$V_I = V_{CC}$ or GND,	$I_S = 8 \text{ mA}$	2.3 V	9	30	
r _{on}	On-state switch resistance	V _C = V _{IH} (see Figure 1)	I _S = 16 mA	3 V	9	30	Ω
		, (I _S = 16 mA	4.5 V	5.5	25	
			$I_S = 4 \text{ mA}$	1.65 V	74.5	165	
<u>.</u>	Dealt or resistance	$V_I = V_{CC}$ to GND,	$I_S = 8 \text{ mA}$	2.3 V	20	60	0
ron(p)	Peak on resistance	VC = VIH (see Figure 1)	I _S = 16 mA	3 V	12.5	35	Ω
		(, , , , , , , , , , , , , , , , , , ,	I _S = 16 mA	4.5 V	7.5	25	
	2 ″	$V_I = V_{CC}$ and $V_O = 0$		5.5 V		±1	
IS(off)	Off-state switch leakage current		$V_I = GND$ and $V_O = V_{CC}$, $V_C = V_{IL}$ (see Figure 2)			±0.1 [†]	μΑ
I _{S(on)}	On-state switch leakage current	V _I = V _{CC} or GND, V ₀ (see Figure 3)	$V_I = V_{CC}$ or GND, $V_C = V_{IH}$, $V_O = Open$ (see Figure 3)			±1 ±0.1†	μΑ
1 ₁	Control input current	V _C = V _{CC} or GND		5.5 V		±1 ±0.1†	μΑ
lcc	Supply current	V _C = V _{CC} or GND		5.5 V		10 1†	μА
Δlcc	Supply current change	$V_C = V_{CC} - 0.6 V$		5.5 V		500	μΑ
C _{ic}	Control input capacitance			5 V	2		pF
C _{io(off)}	Switch input/output capacitance			5 V	6		pF
C _{io(on)}	Switch input/output capacitance			5 V	13		pF

 $^{^{\}dagger}T_{A} = 25^{\circ}C$



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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = ± 0.1		V _{CC} =		V _{CC} =		± 0.5		UNIT
	(INFOT)	(0011-01)	MIN	MIN MAX		MAX	MIN	MAX	MIN	MAX	
t _{pd} †	A or B	B or A		5.5		3.2		2.8		2.6	ns
t _{en} ‡	С	A or B	2.5	14	1.9	9.5	1.8	8	1.5	7.2	ns
t _{dis} §	С	A or B	2.2	12	1.4	8.9	2	8.4	1.4	6.9	ns

[†] tPLH and tPHL are the same as tpd. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

analog switch characteristics, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	v _{CC}	TYP	UNIT
				1.65 V	35	
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	120	
			f _{in} = sine wave (see Figure 5)	3 V	175	
Frequency response¶	A D	D A	(SSS Figure S)	4.5 V	195	NALI-
(switch ON)	A or B	B or A		1.65 V	>300	MHz
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	2.3 V	>300	
			f _{in} = sine wave (see Figure 5)	3 V	>300	
			(ecc : .ga.c c)	4.5 V	>300	
				1.65 V	35	
Crosstalk	0	A == D	$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	50	/
(control input to signal output)	С	A or B	f _{in} = 1 MHz (square wave) (see Figure 6)	3 V	70	mV
			(SSS Figure S)	4.5 V	100	
	A or B	B or A		1.65 V	-58	dB
			$C_L = 50 \text{ pF}, R_L = 600 \Omega,$	2.3 V	-58	
			f _{in} = 1 MHz (sine wave) (see Figure 7)	3 V	-58	
Feedthrough attenuation#			, , , , , , , , , , , , , , , , , , ,	4.5 V	-58	
(switch OFF)	AUID	DUIA		1.65 V	-42	
			$C_L = 5 \text{ pF}, R_L = 50 \Omega,$	2.3 V	-42	
			f _{in} = 1 MHz (sine wave) (see Figure 7)	3 V	-42	
			(cos go s)	4.5 V	-42	
				1.65 V	0.1	
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$ $f_{\text{in}} = 1 \text{ kHz (sine wave)}$	2.3 V	0.025	
Sine-wave distortion			(see Figure 8)	3 V	0.015	%
	A or B	B or A		4.5 V	0.01	
	AUID	DUIA		1.65 V	0.15	
			$C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega,$	2.3 V	0.025	
			f _{in} = 10 kHz (sine wave) (see Figure 8)	3 V	0.015	
			3 ,	4.5 V	0.01	

Adjust fin voltage to obtain 0 dBm at output. Increase fin frequency until dB meter reads –3 dB.



 $[\]ddagger$ tp_ZL and tpZH are the same as ten. \$ tpLZ and tpHZ are the same as tdis.

[#] Adjust fin voltage to obtain 0 dBm at input.

SN74LVC1G66-Q1 SINGLE BILATERAL ANALOG SWITCH

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operating characteristics, $T_A = 25^{\circ}C$

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	LINUT	
	FARAMETER	TEST CONDITIONS	TYP	TYP	TYP	TYP	UNIT	
C _{pd}	Power dissipation capacitance	f = 10 MHz	8	9	9	11	pF	

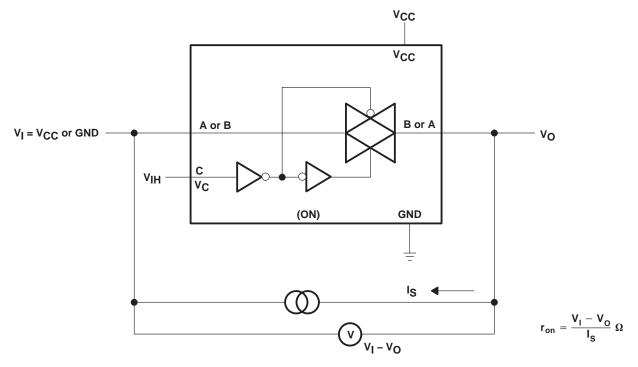


Figure 1. On-State Resistance Test Circuit

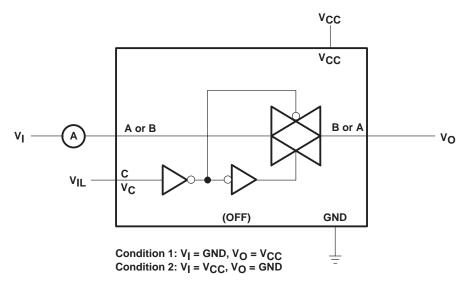


Figure 2. Off-State Switch Leakage-Current Test Circuit

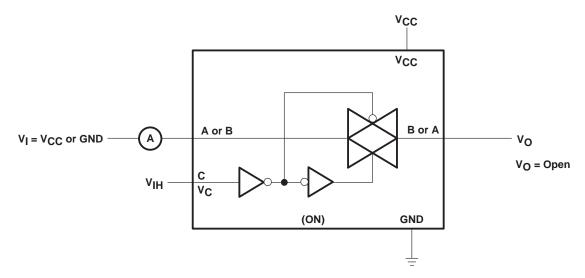
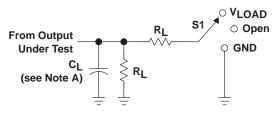


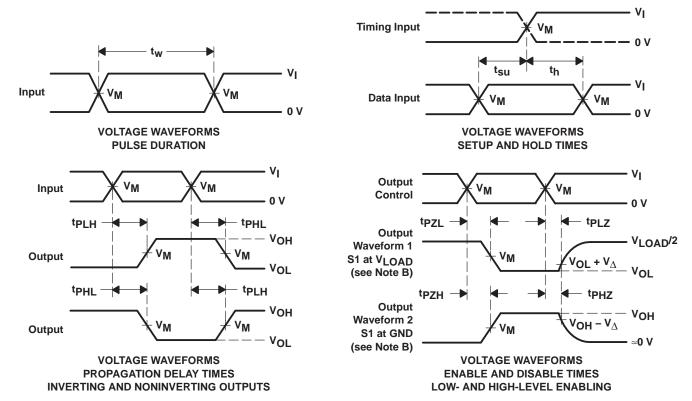
Figure 3. On-State Leakage-Current Test Circuit



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	V _{LOAD}
tPHZ/tPZH	GND

LOAD CIRCUIT

.,	INF	PUTS	.,	V	•	_	.,
VCC	٧ _I	t _r /t _f	VM	VLOAD	CL	RL	$v_{\!\scriptscriptstyle\Delta}$
1.8 V \pm 0.15 V	VCC	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	VCC	≤ 2 ns	V _{CC} /2	2×VCC	30 pF	500 Ω	0.15 V
3.3 V \pm 0.3 V	VCC	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V
5 V \pm 0.5 V	VCC	≤2.5 ns	V _{CC} /2	2×V _{CC}	50 pF	500 Ω	0.3 V



NOTES: A. C_I includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_Ω = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms



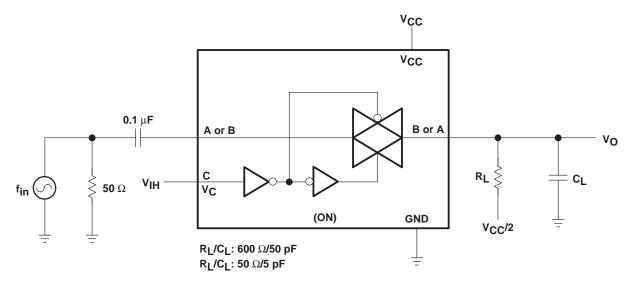


Figure 5. Frequency Response (Switch ON)

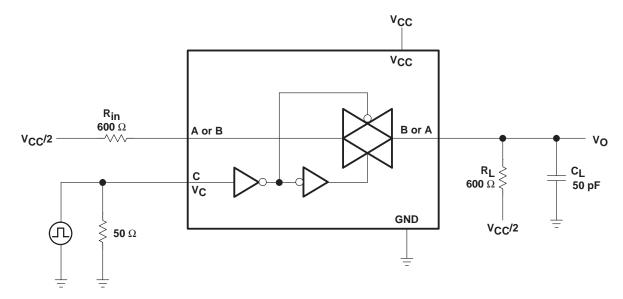


Figure 6. Crosstalk (Control Input – Switch Output)

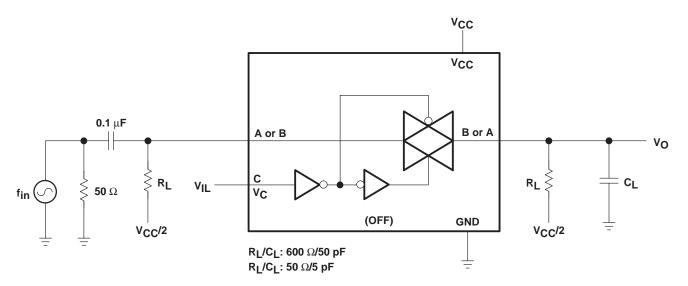


Figure 7. Feed Through (Switch OFF)

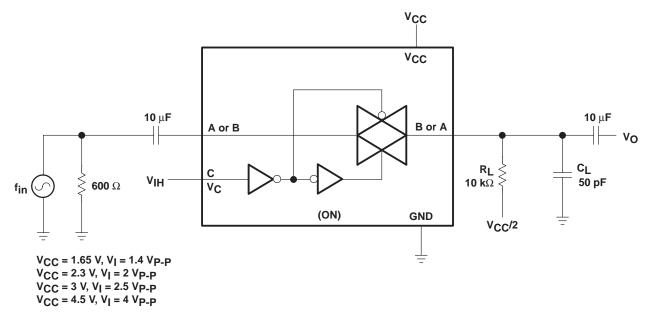


Figure 8. Sine-Wave Distortion

27-Aug-2011

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
1P1G66QDBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
1P1G66QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LVC1G66QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G66-Q1:

Catalog: SN74LVC1G66





27-Aug-2011

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.



DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



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