



SN74LVC07A Hex Buffer/Driver With Open-Drain Outputs

1 Features

- Operates From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages Up to 5.5 V
- Max t_{pd} of 2.6 ns at 5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- MP3 Player or Recorder
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD, Digital, and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

4 Simplified Schematic



3 Description

This hex buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC07A	SOIC (14)	8.65 mm × 3.91 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TVSOP (14)	3.60 mm × 4.40 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	VQFN (14)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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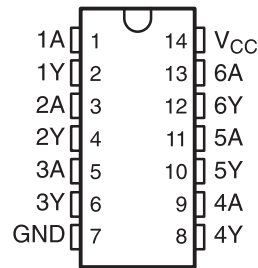
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

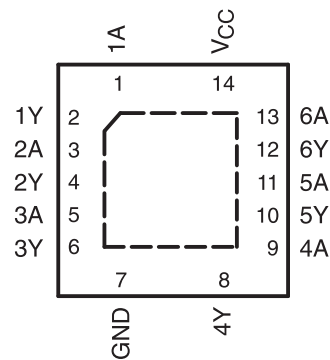
Changes from Revision T (February 2011) to Revision U	Page
• Updated document to new TI data sheet format	1
• Removed Ordering Information table.	1
• Added I _{off} Feature bullet	1
• Added Applications.	1
• Added Device Information table.	1
• Added Handling Ratings table.	4
• Changed MAX operating free-air temperature from 85°C to 125°C	5
• Updated Thermal Information table.	5
• Added –40°C TO 125°C temperature range to Electrical Characteristics table	6
• Added Switching Characteristics table for –40°C TO 125°C temperature range	6
• Added Typical Characteristics.	7

6 Pin Configuration and Functions

**D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)**



**RGY PACKAGE
(TOP VIEW)**



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I	Input 1
2	1Y	O	Output 1
3	A2	I	Input 1
4	Y2	O	Output 2
5	A3	I	Input 3
6	Y3	O	Output 3
7	GND	—	Ground pin
8	Y4	O	Output 4
9	A4	I	Input 4
10	Y5	O	Output 5
11	A5	I	Input 5
12	Y6	O	Output 6
13	A7	I	Input 6
14	VCC	—	Power pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6.5	V
V_I	Input voltage range ⁽²⁾		–0.5	6.5	V
V_O	Output voltage range		–0.5	6.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	0	1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 2.7 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I	Input voltage		0	5.5	V
V _O	Output voltage		0	5.5	V
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		12	
		V _{CC} = 2.7 V		12	
		V _{CC} = 3 V		24	
		V _{CC} = 4.5 V		24	
T _A	Operating free-air temperature		–40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC ⁽¹⁾		D	DB	DGV	NS	PW	RGY	UNIT
		14 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	177.4	135.1	157.7	120.3	160.3	80.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	75.4	86.7	78.3	76.3	84.4	97.0	
R _{θJB}	Junction-to-board thermal resistance	70.6	82.4	90.8	79.0	102.1	56.7	
ψ _{JT}	Junction-to-top characterization parameter	34.7	43.7	21.0	36.2	24.3	16.7	
ψ _{JB}	Junction-to-board characterization parameter	70.4	81.9	90.1	78.7	101.4	56.8	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	35.8	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, literature number [SPRA953](#).

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7.5 Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40°C TO 85°C			–40°C TO 125°C			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{OL}	I _{OL} = 100 µA	1.65 V to 5.5 V			0.2			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45			0.45	
	I _{OL} = 12 mA	2.3 V			0.7			0.7	
		2.7 V			0.4			0.4	
	I _{OL} = 24 mA	3 V			0.55			0.55	
I _I	V _I = 5.5 V or GND	3.6 V			±5			±5	µA
I _{off}	V _I or V _O = 5.5 V	0 V			±10			±10	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10			10	µA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500			500	µA
C _i	V _I = V _{CC} or GND	3.3 V			5.0			5.0	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

7.6 Switching Characteristics –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) through [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 85°C										UNIT
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1	5.6	1	3.4	1	3.3	1	3.6	1	2.6	ns

7.7 Switching Characteristics –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#) through [Figure 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	–40°C TO 125°C								UNIT		
			V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 5 V ± 0.5 V	
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX
t _{pd}	A	Y	1	6.1	1	3.9	1	3.8	1	4.1	1	3.1	ns

7.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C _{pd}	Power dissipation capacitance per buffer/driver	f = 10 MHz	1.8	2	2.5	3.78	pF

7.9 Typical Characteristics

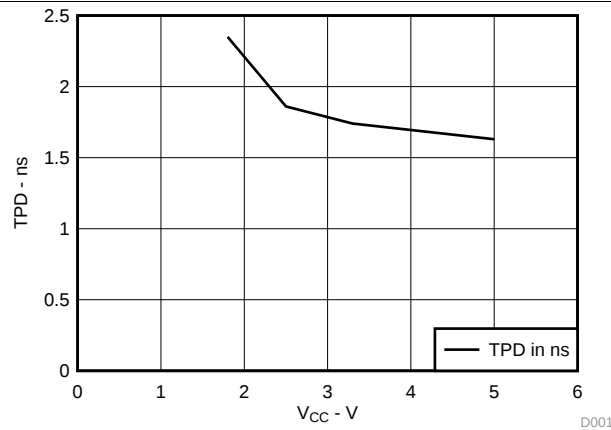


Figure 1. TPD vs V_{CC}

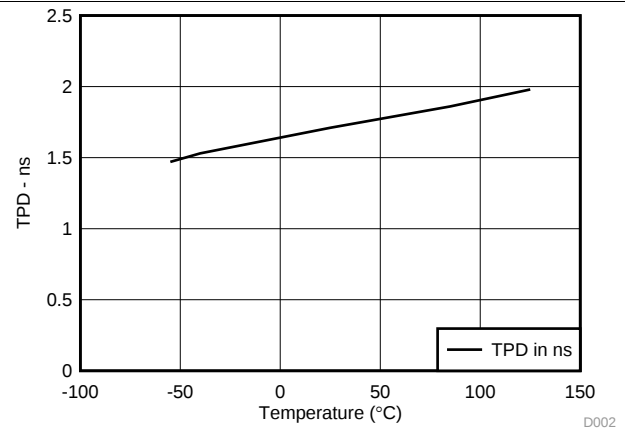
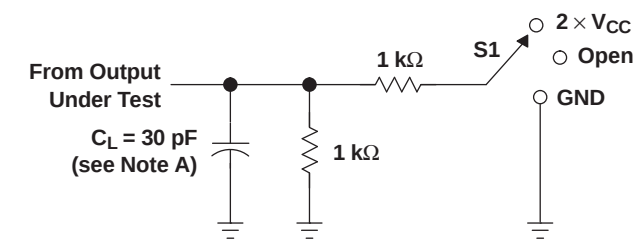


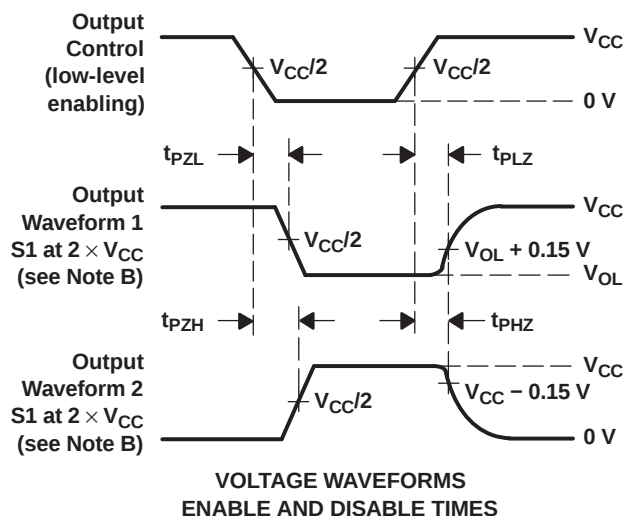
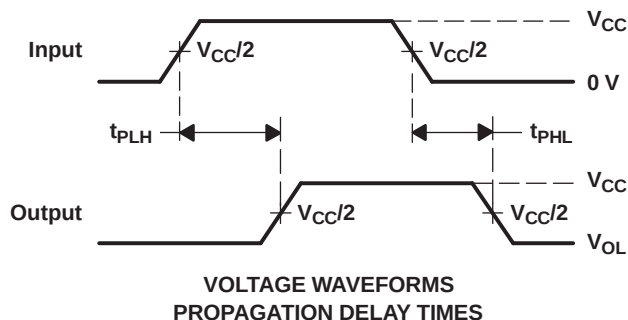
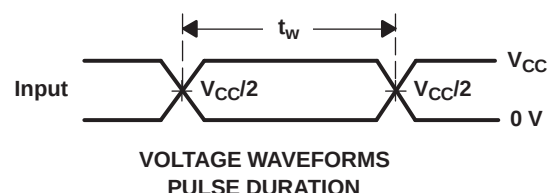
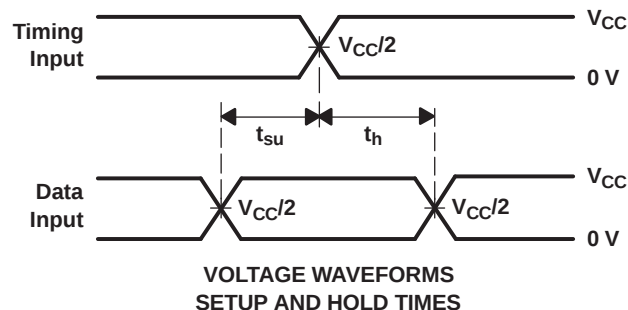
Figure 2. TPD vs Temperature

8 Parameter Measurement Information

8.1 $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$


LOAD CIRCUIT

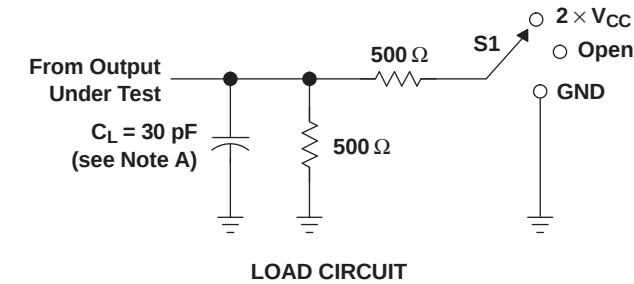
TEST	S1
t_{PZL} (see Note F)	2 $\times V_{CC}$
t_{PLZ} (see Note G)	2 $\times V_{CC}$
t_{PHZ}/t_{PHL}	2 $\times V_{CC}$



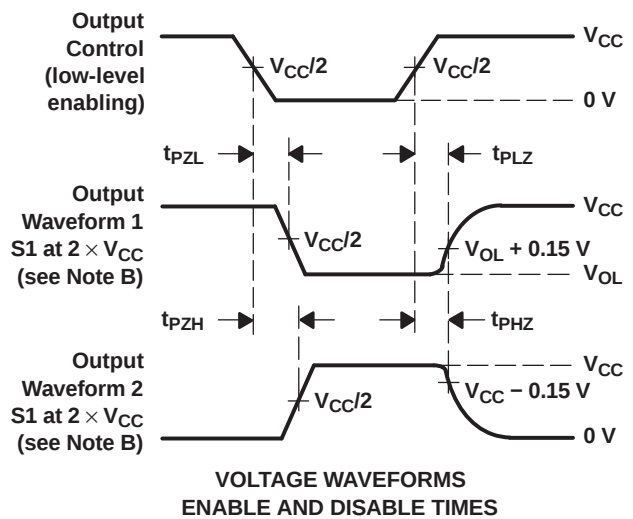
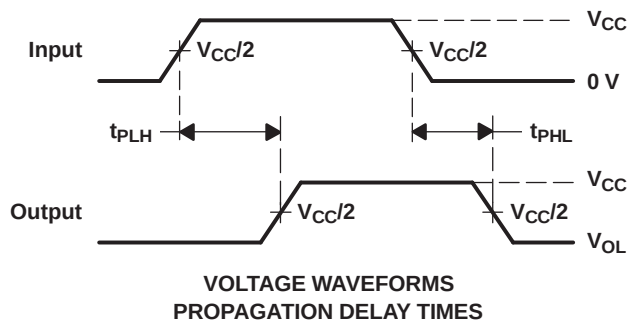
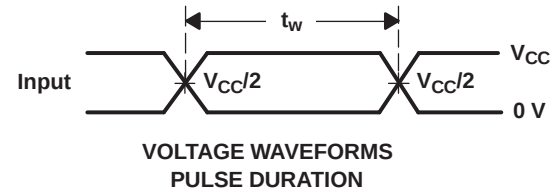
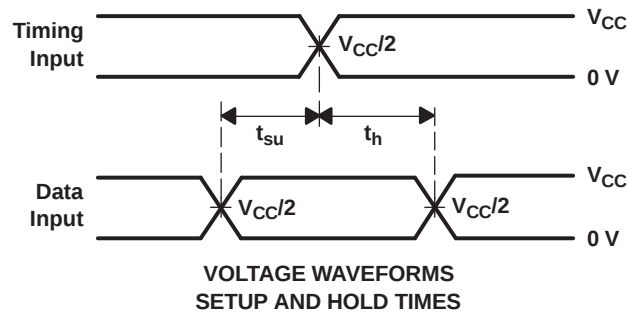
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2\text{ ns}$, $t_f \leq 2\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 - t_{PZL} is measured at $V_{CC}/2$.
 - t_{PLZ} is measured at $V_{OL} + 0.15\text{ V}$.
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8.2 $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$



TEST	S1
t_{PZL} (see Note F)	2 $\times V_{CC}$
t_{PLZ} (see Note G)	2 $\times V_{CC}$
t_{PHZ}/t_{PZH}	2 $\times V_{CC}$

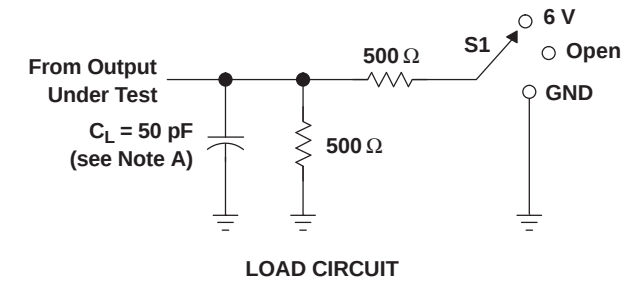


- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 - t_{PZL} is measured at $V_{CC}/2$.
 - t_{PLZ} is measured at $V_{OL} + 0.15 \text{ V}$.
 - All parameters and waveforms are not applicable to all devices.

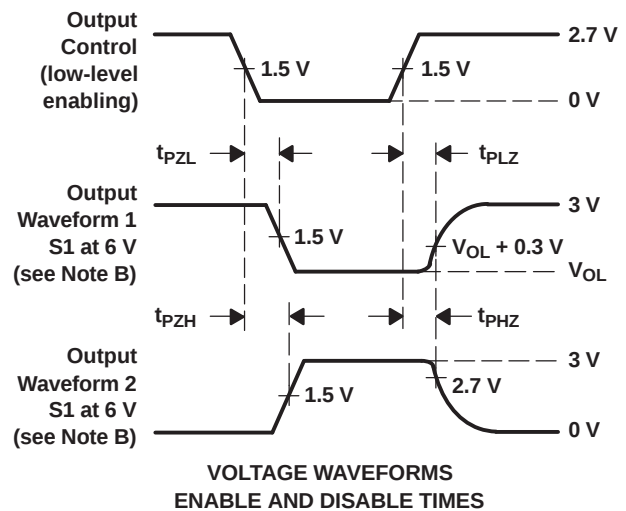
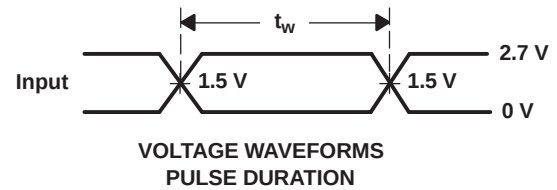
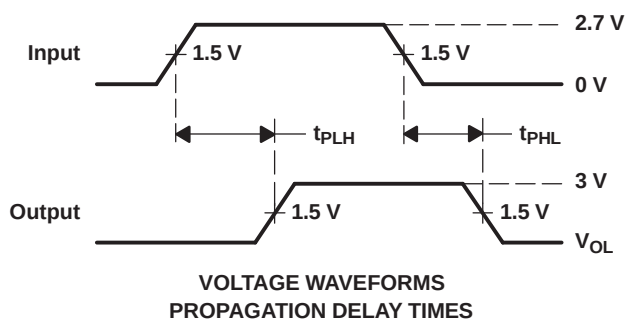
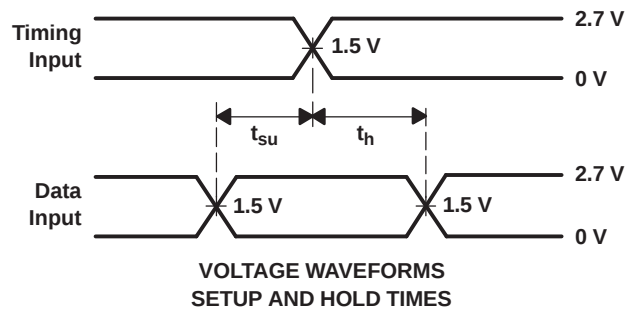
Figure 4. Load Circuit and Voltage Waveforms

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8.3 $V_{CC} = 2.7$ and $3.3\text{ V} \pm 0.3\text{ V}$


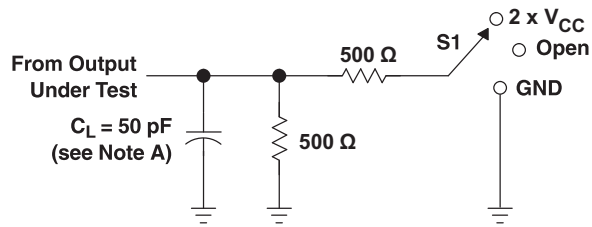
TEST	S1
t_{pZL} (see Note F)	6 V
t_{pLZ} (see Note G)	6 V
t_{PHZ}/t_{PZH}	6 V



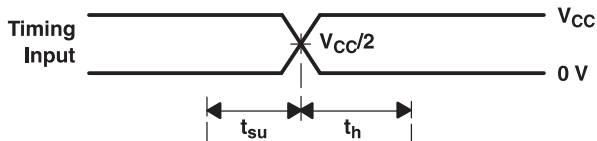
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - t_{pZL} is measured at 1.5 V.
 - t_{pLZ} is measured at $V_{OL} + 0.3\text{ V}$.
 - All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

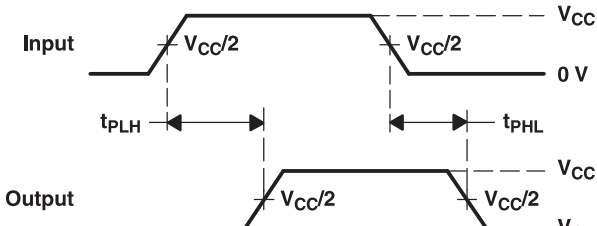
8.4 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$



LOAD CIRCUIT

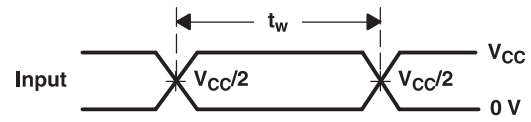


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

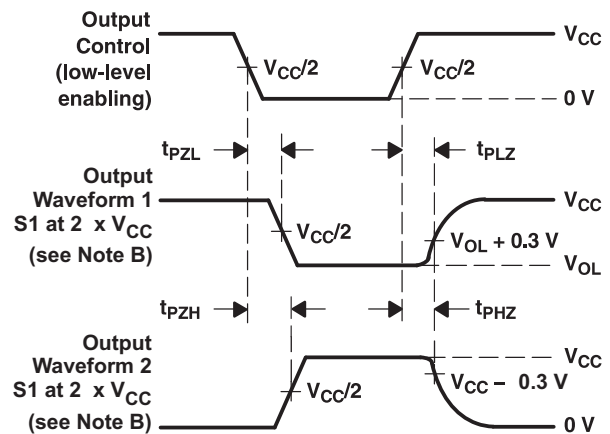


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

TEST	S1
t_{PZL} (see Note F)	2 x V_{CC}
t_{PLZ} (see Note G)	2 x V_{CC}
t_{PHZ}/t_{PZH}	2 x V_{CC}



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal connections such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal connections such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd} .
 - t_{PZL} is measured at $V_{CC}/2$.
 - t_{PLZ} is measured at $V_{OL} + 0.3\text{ V}$.
 - All parameters and waveforms are not applicable to all devices.

Figure 6. Load Circuit and Voltage Waveforms

9 Detailed Description

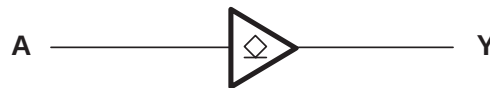
9.1 Overview

The outputs of the SN74LVC07A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of this device as translators in a mixed-system environment.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram



9.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 5.5 V
- Allows up or down voltage translation
 - Inputs and outputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

Table 1. Function Table

INPUT A	OUTPUT Y
H	H
L	L

10 Application and Implementation

10.1 Application Information

The SN74LVC07A device is a high-drive, open-drain CMOS device that can be used for a multitude of buffer-type functions. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple inputs and for high-speed applications up to 100 Mhz. The inputs and outputs are 5.5-V tolerant allowing the device to translate up to 5.5 V or down to V_{CC} .

10.2 Typical Application

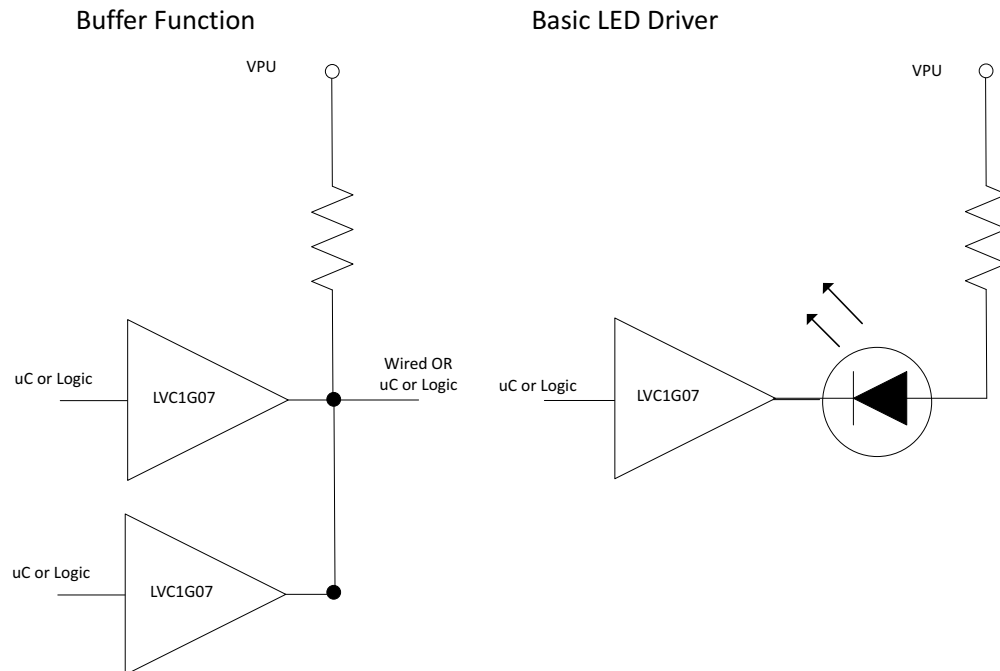


Figure 7. Typical Application Diagram

10.2.1 Design Requirements

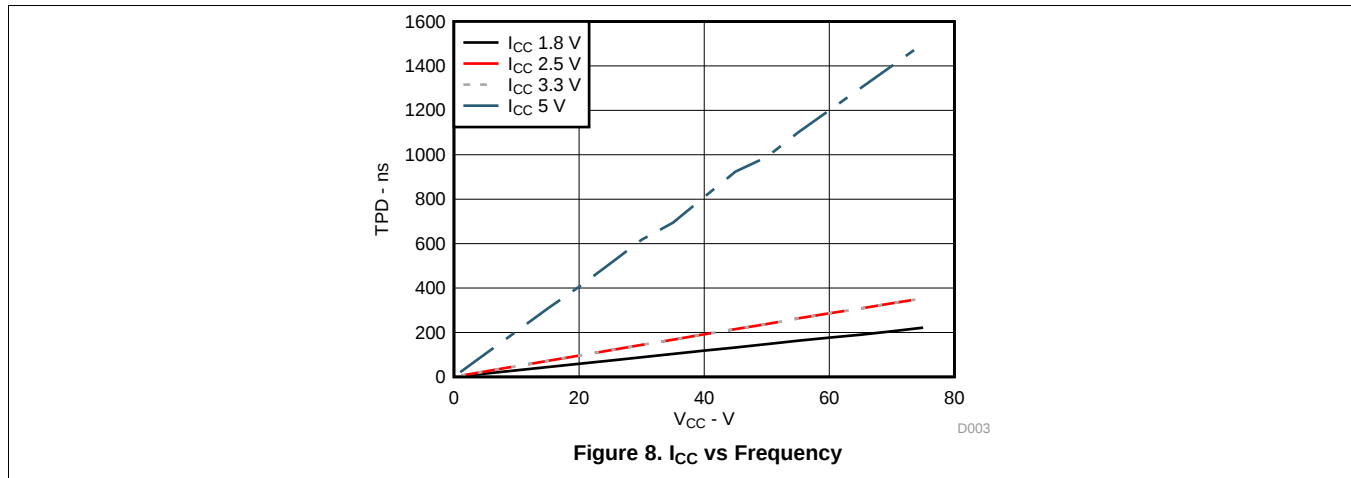
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
 - Rise time and fall time specs: See $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - Specified high and low levels: See $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above 5.5 V.

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple V_{CC} pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 9](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver.

12.2 Layout Example

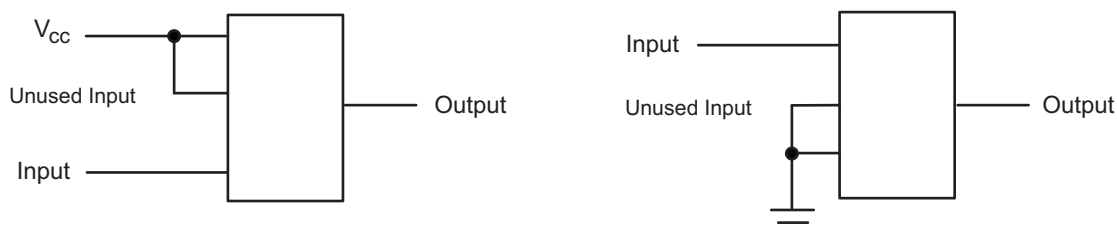


Figure 9. Layout Diagram

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC07AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ADRG3	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ADT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ADTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC07A	Samples
SN74LVC07APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC07APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWRG3	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC07A	Samples
SN74LVC07ARGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC07A	Samples
SN74LVC07ARGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC07A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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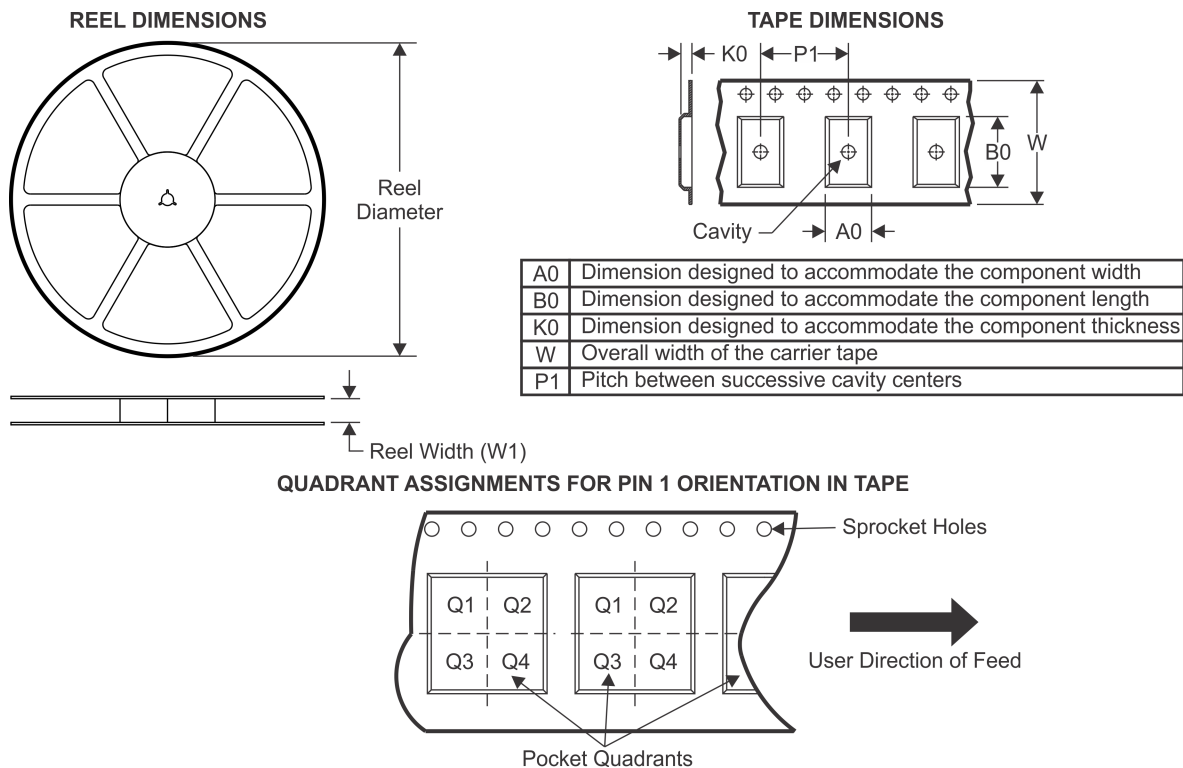
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OTHER QUALIFIED VERSIONS OF SN74LVC07A :

- Automotive: [SN74LVC07A-Q1](#)
- Enhanced Product: [SN74LVC07A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC07ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LVC07ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LVC07ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC07ADR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74LVC07ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC07ADRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74LVC07ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC07ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC07ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC07ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC07APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC07APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC07APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC07APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC07ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC07ADBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74LVC07ADGVR	TVSOP	DGV	14	2000	367.0	367.0	35.0
SN74LVC07ADR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LVC07ADR	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC07ADR	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC07ADRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC07ADRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC07ADRG4	SOIC	D	14	2500	367.0	367.0	38.0
SN74LVC07ADT	SOIC	D	14	250	367.0	367.0	38.0
SN74LVC07ANSR	SO	NS	14	2000	367.0	367.0	38.0
SN74LVC07APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC07APWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LVC07APWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74LVC07APWT	TSSOP	PW	14	250	367.0	367.0	35.0
SN74LVC07ARGYR	VQFN	RGY	14	3000	367.0	367.0	35.0

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

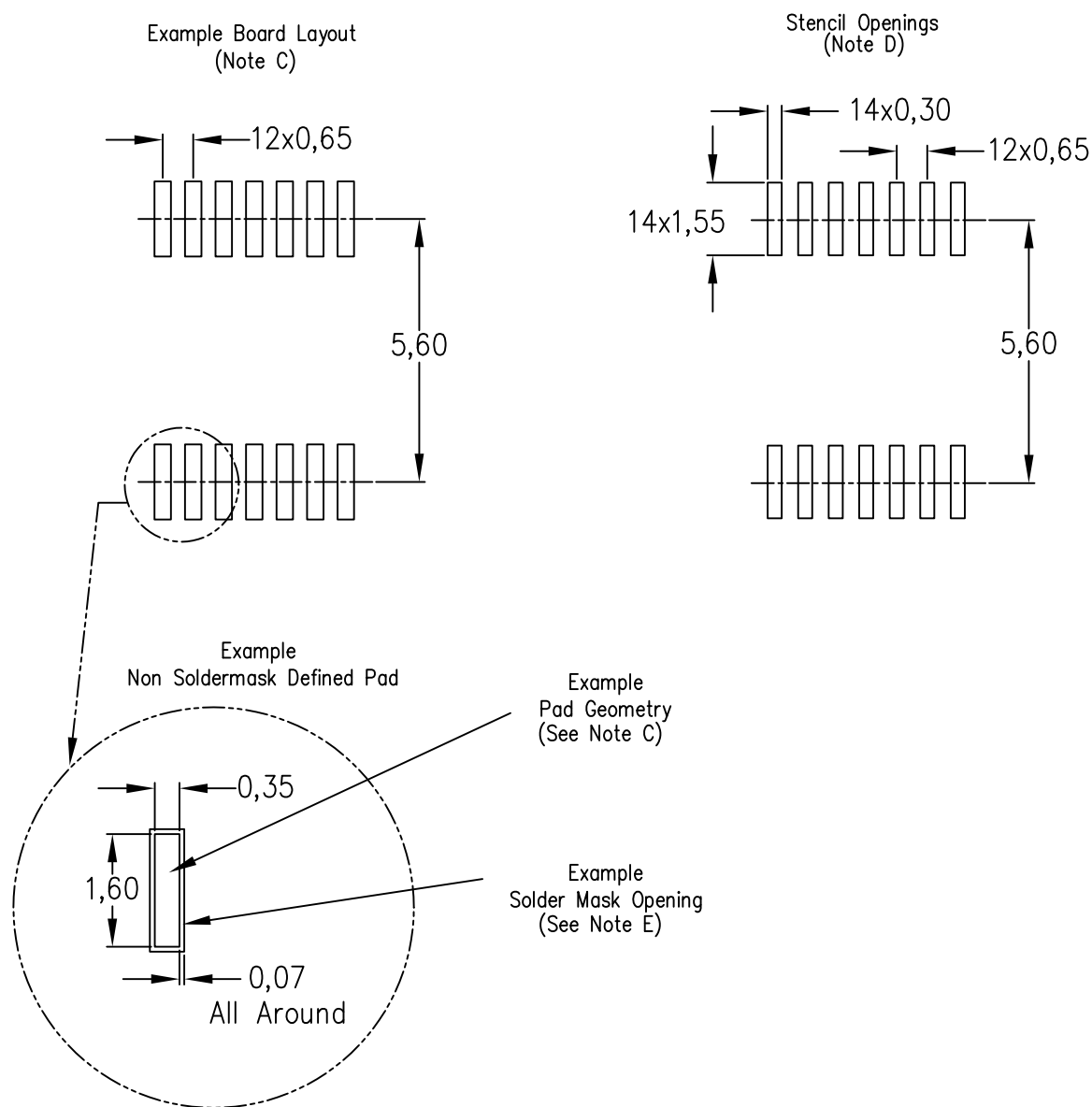
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

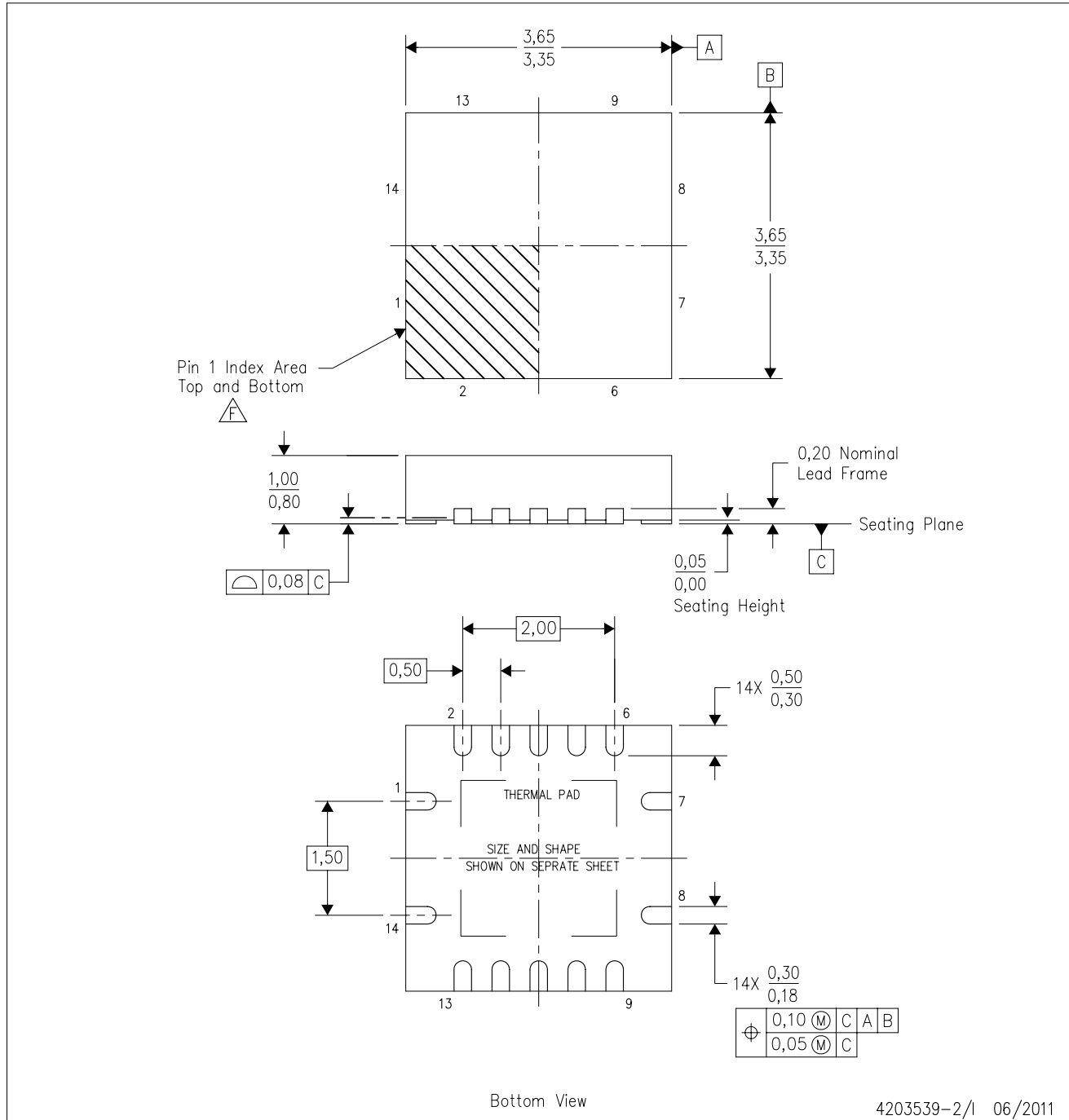


4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

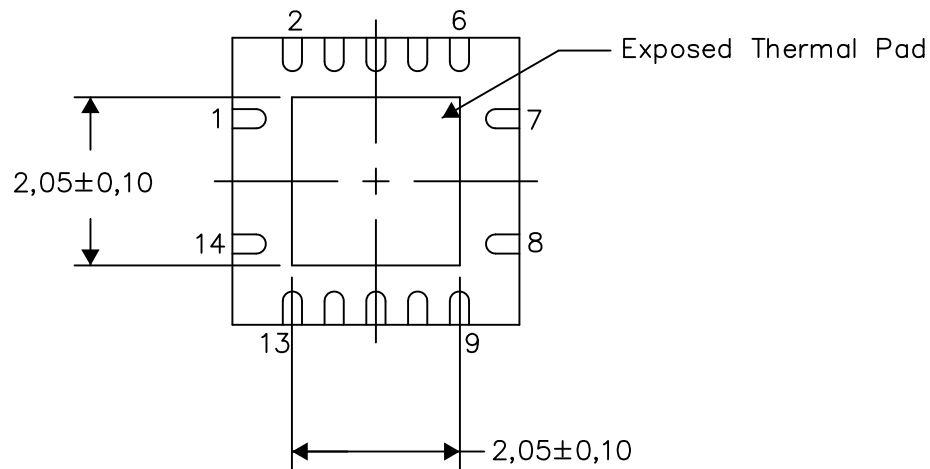
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

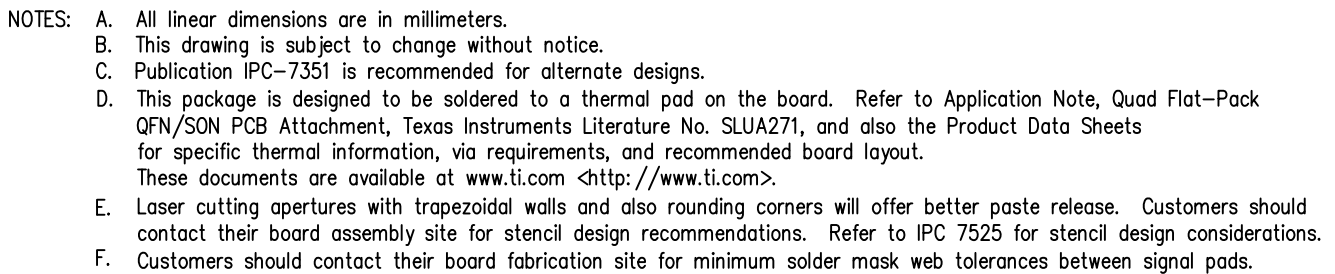


Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters



MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

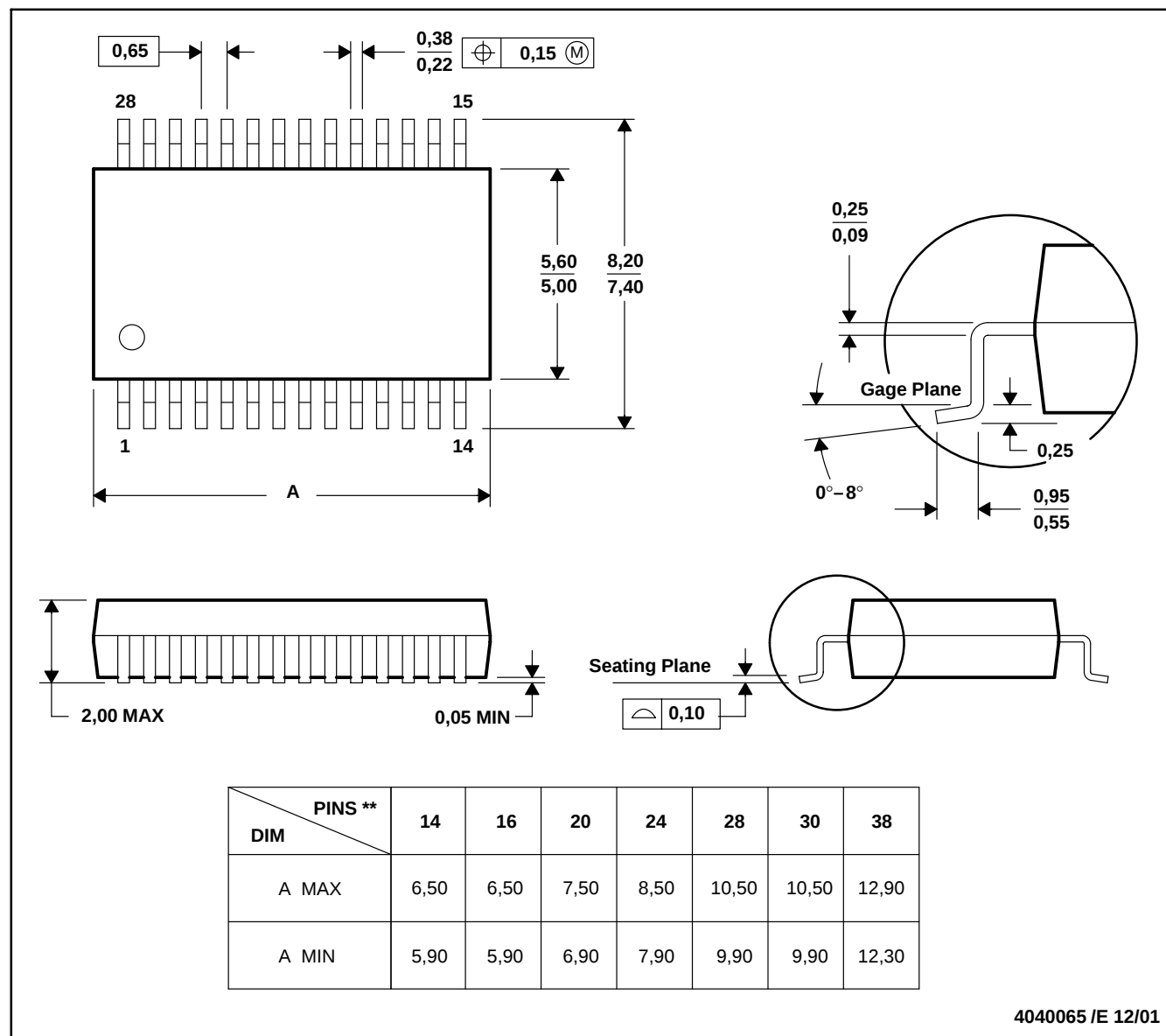
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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