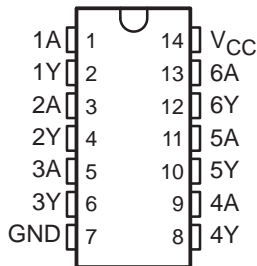


SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

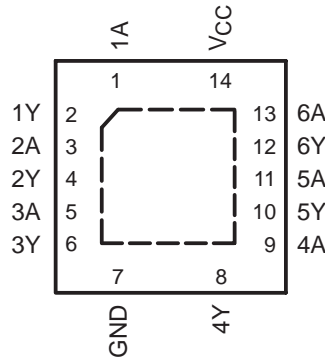
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- Operate From 1.65 V to 3.6 V
- Specified From -40°C to 85°C , -40°C to 125°C , and -55°C to 125°C
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Max t_{pd} of 3.7 ns at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17

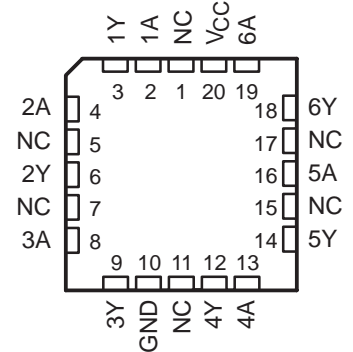
SN54LVC06A ... J OR W PACKAGE
SN74LVC06A ... D, DB, DGV, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LVC06A ... RGY PACKAGE
(TOP VIEW)



SN54LVC06A ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These hex inverter buffers/drivers are designed for 1.65-V to 3.6-V V_{CC} operation.

The outputs of the 'LVC06A devices are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
-40°C to 85°C	QFN – RGY	Reel of 1000	SN74LVC06ARGYR	LC06A	
-40°C to 125°C	SOIC – D	Tube of 50	SN74LVC06AD	LVC06A	
		Reel of 2500	SN74LVC06ADR		
		Reel of 250	SN74LVC06ADT		
		SOP – NS	Reel of 2000		SN74LVC06ANSR
	SSOP – DB	TSSOP – PW	Reel of 2000	SN74LVC06ADBR	LC06A
			Tube of 90	SN74LVC06APW	
			Reel of 2000	SN74LVC06APWR	
Reel of 250	SN74LVC06APWT				
TVSOP – DGV	Reel of 2000	SN74LVC06ADGVR	LC06A		
-55°C to 125°C	CDIP – J	Tube of 25	SNJ54LVC06AJ	SNJ54LVC06AJ	
	CFP – W	Tube of 150	SNJ54LVC06AW	SNJ54LVC06AW	
	LCCC – FK	Tube of 55	SNJ54LVC06AFK	SNJ54LVC06AFK	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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description/ordering information (continued)

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram, each inverter (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	-0.5 V to 6.5 V
Output voltage range, V_O	-0.5 V to 6.5 V
Input clamp current, I_{IK} ($V_I < 0$)	-50 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Continuous output current, I_O	± 50 mA
Continuous current through V_{CC} or GND	± 100 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): DGV package	127°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	-65°C to 150°C
Power dissipation, P_{tot} ($T_A = -40^\circ\text{C}$ to 125°C) (see Notes 4 and 5)	500 mW

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51-7.
 3. The package thermal impedance is calculated in accordance with JESD 51-5.
 4. For the D package: above 70°C the value of P_{tot} derates linearly with 8 mW/K.
 5. For the DB, DGV, NS, and PW packages: above 60°C the value of P_{tot} derates linearly with 5.5 mW/K.

SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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recommended operating conditions (see Note 6)

		SN54LVC06A		UNIT	
					-55 TO 125°C
		MIN	MAX		
V _{CC}	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 2.7 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 2.7 V to 3.6 V	0.8		
V _I	Input voltage	0	5.5		V
V _O	Output voltage	0	5.5		V
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		mA
		V _{CC} = 2.3 V	8		
		V _{CC} = 2.7 V	12		
		V _{CC} = 3 V	24		

NOTE 6: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions (see Note 6)

		SN74LVC06A						UNIT			
		T _A = 25°C		-40 TO 85°C		-40 TO 125°C					
		MIN	MAX	MIN	MAX	MIN	MAX				
V _{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V		
		Data retention only	1.5		1.5		1.5				
V _{IH}	High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		0.65 × V _{CC}		0.65 × V _{CC}		V		
		V _{CC} = 2.3 V to 2.7 V	1.7		1.7		1.7				
		V _{CC} = 2.7 V to 3.6 V	2		2		2				
V _{IL}	Low-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.35 × V _{CC}		0.35 × V _{CC}		0.35 × V _{CC}		V		
		V _{CC} = 2.3 V to 2.7 V	0.7		0.7		0.7				
		V _{CC} = 2.7 V to 3.6 V	0.8		0.8		0.8				
V _I	Input voltage	0	5.5		0	5.5		0	5.5		V
V _O	Output voltage	0	5.5		0	5.5		0	5.5		V
I _{OL}	Low-level output current	V _{CC} = 1.65 V	4		4		4		mA		
		V _{CC} = 2.3 V	8		8		8				
		V _{CC} = 2.7 V	12		12		12				
		V _{CC} = 3 V	24		24		24				

NOTE 6: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN54LVC06A			UNIT
			-55 TO 125°C			
			MIN	TYP	MAX	
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.2	V
	I _{OL} = 4 mA	1.65 V			0.45	
	I _{OL} = 8 mA	2.3 V			0.7	
	I _{OL} = 12 mA	2.7 V			0.4	
	I _{OL} = 24 mA	3 V			0.55	
I _I	V _I = 5.5 V or GND	3.6 V			±5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			10	μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500	μA
C _i	V _I = V _{CC} or GND	3.3 V			5†	pF

† T_A = 25°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	SN74LVC06A						UNIT	
			T _A = 25°C			-40 TO 85°C		-40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V _{OL}	I _{OL} = 100 μA	1.65 V to 3.6 V			0.1		0.2		0.3	V
	I _{OL} = 4 mA	1.65 V			0.24		0.45		0.6	
	I _{OL} = 8 mA	2.3 V			0.3		0.7		0.75	
	I _{OL} = 12 mA	2.7 V			0.4		0.4		0.6	
	I _{OL} = 24 mA	3 V			0.55		0.55		0.8	
I _I	V _I = 5.5 V or GND	3.6 V			±1		±5		±20	μA
I _{off}	V _I or V _O = 5.5 V	0			±1		±10		±20	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6 V			1		10		40	μA
ΔI _{CC}	One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND	2.7 V to 3.6 V			500		500		5000	μA
C _i	V _I = V _{CC} or GND	3.3 V			5					pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN54LVC06A		UNIT
				-55 TO 125°C		
				MIN	MAX	
t _{pd}	A	Y	1.8 V ± 0.15 V	1.4	5.6	ns
			2.5 V ± 0.2 V	1	3.1	
			2.7 V		3.9	
			3.3 V ± 0.3 V	1	3.7	

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SN54LVC06A, SN74LVC06A
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-DRAIN OUTPUTS

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	SN74LVC06A						UNIT	
				T _A = 25°C			-40 TO 85°C		-40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t _{pd}	A	Y	1.8 V ± 0.15 V	1.4	3	5.1	1.4	5.6	1.4	7.6	ns
			2.5 V ± 0.2 V	1	1.9	2.8	1	3.1	1	4	
			2.7 V	1	2.4	3.7	1	3.9	1	5	
			3.3 V ± 0.3 V	1	2.2	3.5	1	3.7	1	5	

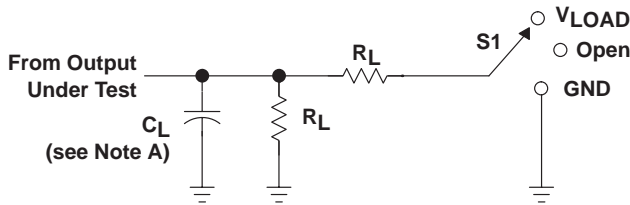
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per buffer/driver	f = 10 MHz	1.8 V	2.1	pF
			2.5 V	2.3	
			3.3 V	2.5	

SN54LVC06A, SN74LVC06A HEX INVERTER BUFFERS/DRIVERS WITH OPEN-DRAIN OUTPUTS

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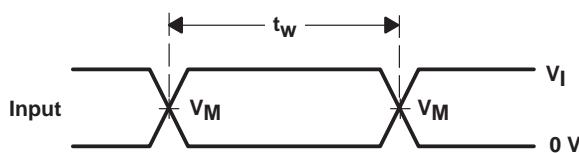
PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



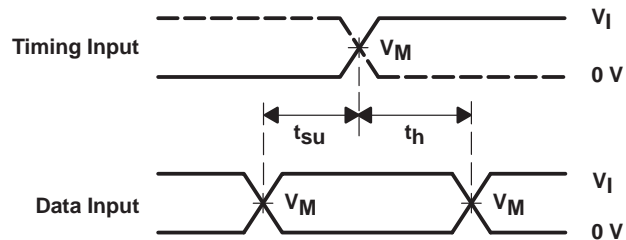
LOAD CIRCUIT

TEST	S1
t_{PZL} (see Notes E and F)	V_{LOAD}
t_{PLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

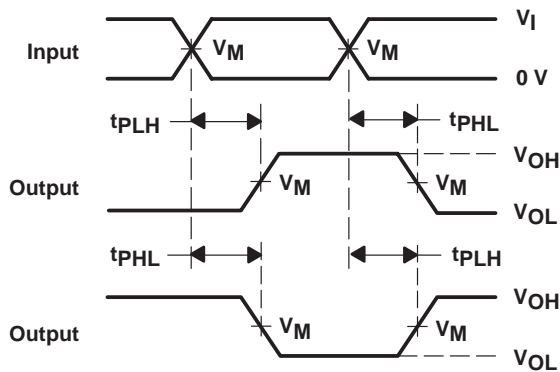
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V



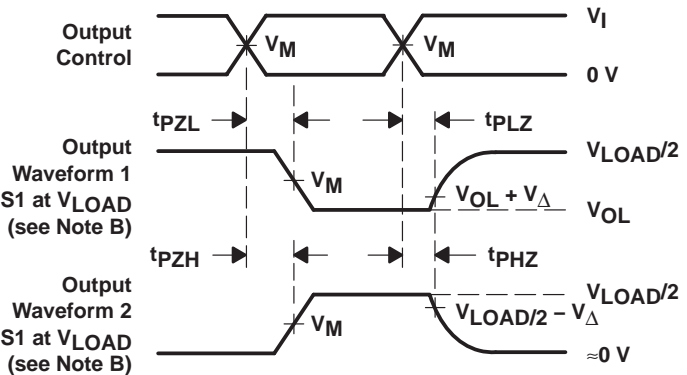
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. Since this device has open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pD} .
 - F. t_{PZL} is measured at V_M .
 - G. t_{PLZ} is measured at $V_{OL} + V_{\Delta}$.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

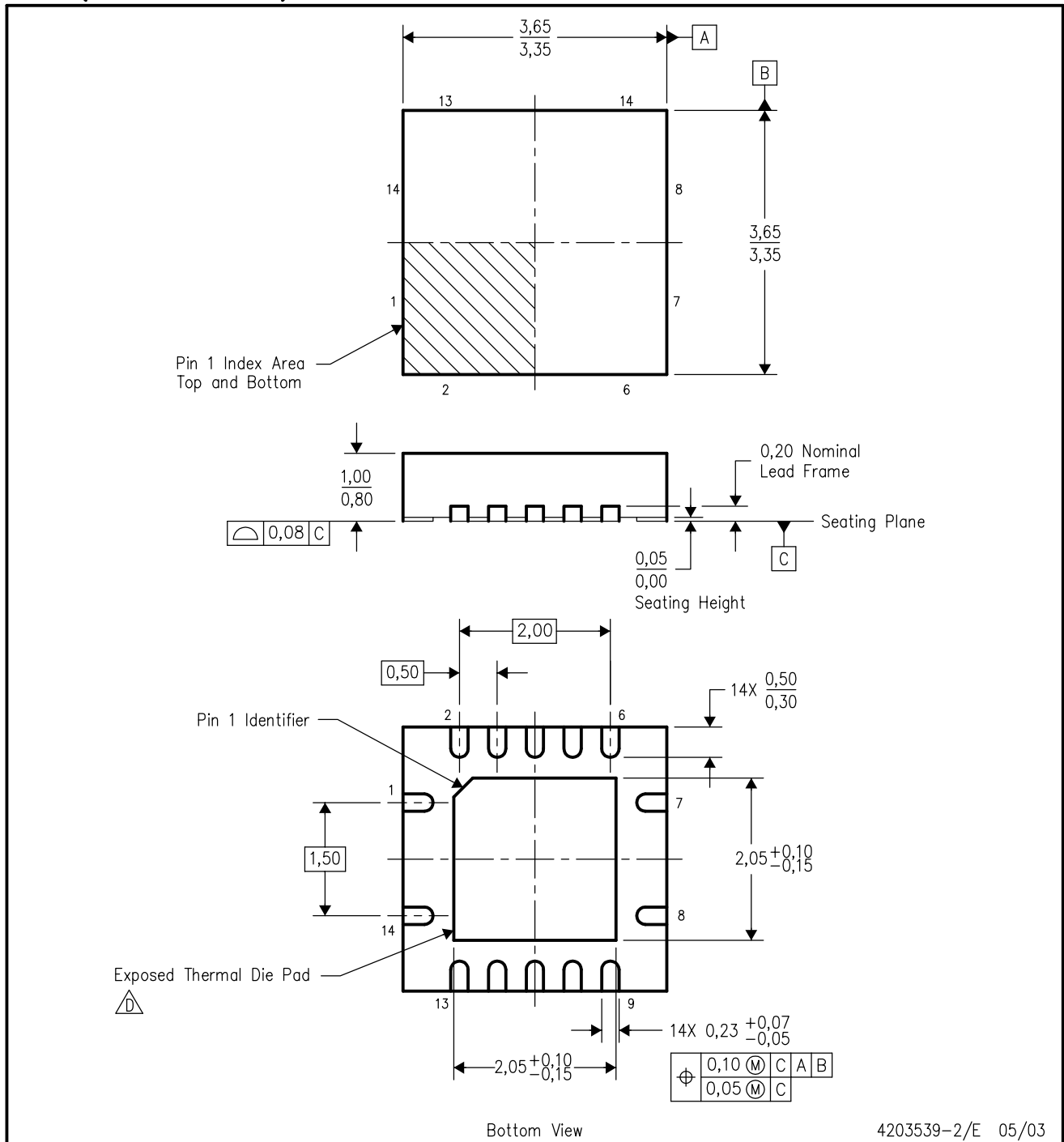
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AB.

RGY (S-PQFP-N14)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - △ The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
 - E. Package complies to JEDEC MO-241 variation BA.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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