

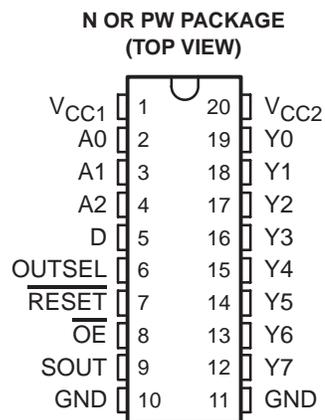
DESCRIPTION

The SN74LV8153 is a serial-to-parallel data converter. It accepts serial input data and outputs 8-bit parallel data.

The automatic data-rate detection feature of the SN74LV8153 eliminates the need for an external oscillator and helps with cost and board real-estate savings.

The OUTSEL pin is used to choose between open collector and push-pull outputs. The open-collector option is suitable when this device is used in applications such as LED interface, where high drive current is required. SOUT is the output that acknowledges reception of the serial data.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC1} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.



**FUNCTION TABLE
(each buffer)**

INPUTS				OUTPUT Y _n	OUTPUT STRUCTURE
OUTSEL	\overline{RESET}	\overline{OE}	D _n		
L	H	L	H	L	Open collector
L	H	L	L	H	
L	X	H	X	H	
L	L	X	X	H	
H	H	L	H	H	Push-pull
H	H	L	L	L	
H	X	H	X	Z	
H	L	L	X	L	

In the open-collector mode (OUTSEL = L), the outputs are inverted, e.g., Y1 = $\bar{1}$, when D1 = H

FEATURES

- Single-Wire Serial Data Input
- Compatible With UART Serial-Data Format
- Up to Eight Devices (64-Bit Parallel) Can Share the Same Bus by Using Different Combinations of A0, A1, A2
- Up to 40 mA Current Drive in Open-Collector Mode for Driving LEDs
- Outputs Can be Configured as Open-Collector or Push-Pull
- Internal Oscillator and Counter for Automatic Data-Rate Detection
- Output Levels Are Referenced to V_{CC2} and Can Be Configured From 3 V to 12 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 1000-V Charged-Device Model (C101)

SUMMARY OF RECOMMENDED OPERATING CONDITIONS

PARAMETER	
V_{CC1}	3 V to 5.5 V
V_{CC2}	3 V to 13.2 V
I_{OL}	40 mA @ $V_{CC2} = 4.5$ V (open-collector mode)
I_{OH}	–24 mA @ $V_{CC2} = 12$ V (push-pull mode)
Maximum Data Rate	24 Kbps



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74LV8153 SERIAL-TO-PARALLEL INTERFACE

SCLS555 – JUNE 2004

ORDERING INFORMATION

T _A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PDIP – N	Tube	SN74LV8153N	SN74LV8153N
	TSSOP – PW	Tube	SN74LV8153PW	LV8153
		Tape and reel	SN74LV8153PWR	

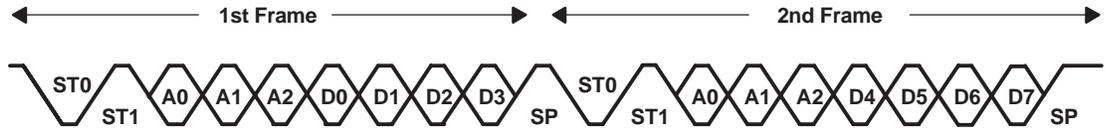
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

PIN DESCRIPTION

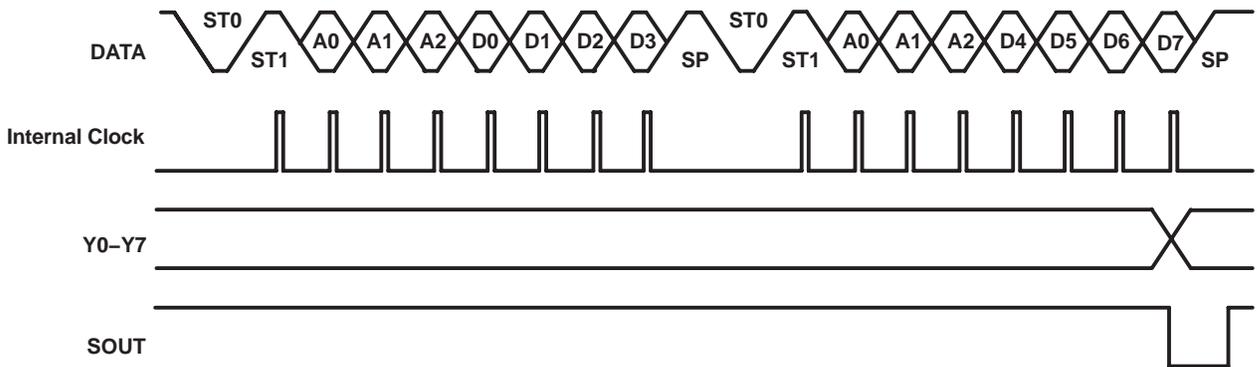
PIN #	PIN NAME	I/O	PIN FUNCTION
1	V _{CC1}		Power-supply pin (all inputs and outputs except for Y0-Y7)
2-4	A0, A1, A2	In	The address pins are used to program the address of the device and allow up to eight devices to share the same bus.
5	D	In	Serial data input
6	OUTSEL	In	Choose between open-collector and push-pull type outputs (Y0-Y7).
7	$\overline{\text{RESET}}$	In	Initialize register status
8	$\overline{\text{OE}}$	In	Force Y0-Y7 to Hi-Z
9	SOUT	Out	Outputs a pulse when latch data is changed. Supplied by V _{CC1} .
12-19	Y0-Y7	Out	Push-pull or open collector parallel data outputs. Supplied by V _{CC2} .
20	V _{CC2}		Power-supply pin for outputs (Y0-Y7). V _{CC2} can range from 3 V to 13.2 V.

data transmission protocol

- The serial data should be sent as 2START-3ADDRESS-4DATA-1STOP. Two consecutive serial-data frames transmit 8 bits of data. The first frame includes the lower four bits of data (D0-D3), and the second frame includes the upper four bits (D4-D7).
- The three address bits (in the consecutive frame) must be the same as those in the first frame; otherwise, the data will be dropped.
- The order of the two start bits must be 0, then 1 in any frame; otherwise, the data rate will not be detected correctly. The period between the falling edge of the first start bit (ST0) and the rising edge of the second start bit (ST1) is measured to generate an internal-clock synchronized data stream.



Example of Serial-Data Format



Timing Chart

(1) Internal clock cannot be observed.

(2) D0 is LSB and D7 is MSB. The data stream should be LSB first.

recommended operating conditions⁽¹⁾

			V _{CC1}	V _{CC2}	MIN	MAX	UNIT	
V _{CC1}	Supply voltage				3	5.5	V	
V _{CC2}	Supply voltage				3	13.2	V	
V _{IH}	High-level input voltage		3 V	3 V	V _{CC} × 0.7		V	
			4.5 V	4.5 V	V _{CC} × 0.7			
V _{IL}	Low-level input voltage		3 V	3 V	V _{CC} × 0.3		V	
			4.5 V	4.5 V	V _{CC} × 0.3			
V _I	Input voltage				0	5.5	V	
V _O	Output voltage		4.5 V	4.5 V	0	5.5	V	
				12 V	0	13.2		
I _{OH}	High-level output current	Y _n	OUTSEL = H		3 V	3 V	-2	mA
					4.5 V	4.5 V	-8	
					4.5 V	12 V	-24	
		SOUT		3 V	3 V	-4	mA	
				4.5 V	4.5 V	-8		
I _{OL}	Low-level output current	Y _n	OUTSEL = H		3 V	3 V	2	mA
					4.5 V	4.5 V	8	
			OUTSEL = L		3 V	3 V	20	
					4.5 V	4.5 V	40	
		SOUT		3 V	3 V	4		
				4.5 V	4.5 V	8		
T _A	Operating free-air temperature				-40	85	°C	

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VCC1	VCC2	MIN	TYP	MAX	UNIT
V_{T+} Positive-going input threshold voltage	All inputs	3.3 V	3.3 V			2.31	V
		5 V	5 V			3.5	
V_{T-} Negative-going input threshold voltage	All inputs	3.3 V	3.3 V	0.99			V
		5 V	5 V	1.5			
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	All inputs	3.3 V	3.3 V	0.33		1.32	V
		5 V	5 V	0.5		2	
V_{OH}	Yn	$I_{OH} = -2$ mA		3 V	3 V	2.38	V
		$I_{OH} = -8$ mA		4.5 V	4.5 V	3.8	
		$I_{OH} = -24$ mA		4.5 V	12 V	11	
	SOUT	$I_{OH} = -4$ mA		3 V	3 V	2.38	
		$I_{OH} = -8$ mA		4.5 V	4.5 V	3.8	
V_{OL}	Yn	$I_{OL} = 2$ mA (OUTSEL = H)		3 V	3 V	0.44	V
		$I_{OL} = 8$ mA (OUTSEL = H)		4.5 V	4.5 V	0.44	
		$I_{OL} = 40$ mA (OUTSEL = L)		4.5 V	4.5 V	0.5	
	SOUT	$I_{OL} = 4$ mA		3 V	3 V	0.44	
		$I_{OL} = 8$ mA		4.5 V	4.5 V	0.44	
I_I	$V_I = 5.5$ V or GND	0 to 5.5 V				± 1	μ A
I_{OZ}	$V_O = V_{CC}$ or GND (OUTSEL = H)	5.5 V	5.5 V			± 5	μ A
I_{OH}	$V_O = 12$ V (OUTSEL = L)	5.5 V	5.5 V			5	μ A
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	OUTSEL = H	5.5 V	5.5 V		5	mA
		OUTSEL = L				20	
I_{off} (except SOUT)	V_I or $V_O = 0$ to 5.5 V, $V_{CC} = 0$	0	0			± 50	μ A
C_i	$V_I = V_{CC}$ or GND	5 V	5 V			5	pF

switching characteristics over recommended operating free-air temperature range, $V_{CC1} = V_{CC2} = 3.3$ V \pm 0.3 V (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	D7	Y	$C_L = 50$ pF		$P_w/2$	(1)			ns
	D7	SOUT			$P_w/2$	(1)			
	$\overline{\text{RESET}}$	Y					200		
	$\overline{\text{OE}}$ (2)	Y					200		
t_{en}	$\overline{\text{OE}}$ (3)	Y					200		ns
t_{dis}	$\overline{\text{OE}}$ (3)	Y					200		ns
t_w		SOUT			P_w	(4)			ns
Data rate						2	24	Kbps	

(1) The t_{pd} is dependent on the data pulse width (P_w), and Y outputs are changed after one-half of P_w , because the internal clock is synchronized at the middle of the data pulse. Not tested, but specified by design.

(2) When outputs are open collector (OUTSEL = L)

(3) When outputs are push-pull (OUTSEL = H)

(4) SOUT goes low when the data is received correctly and maintains a low level for one data-pulse period. Not tested, but specified by design.

switching characteristics over recommended operating free-air temperature range, $V_{CC1} = V_{CC2} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	D7	Y	$C_L = 50\text{ pF}$		$P_w/2$	(1)			ns
	D7	SOUT			$P_w/2$	(1)			
	$\overline{\text{RESET}}$	Y						150	
	$\overline{\text{OE}}(2)$	Y						150	
t_{en}	$\overline{\text{OE}}(3)$	Y						150	ns
t_{dis}	$\overline{\text{OE}}(3)$	Y						150	ns
t_w		SOUT			P_w	(4)			ns
Data rate							2	24	Kbps

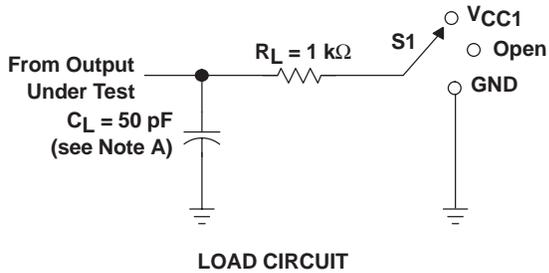
(1) The t_{pd} is dependent on the data pulse width (P_w), and Y outputs are changed after one-half of P_w , because the internal clock is synchronized at the middle of the data pulse. Not tested, but specified by design.

(2) When outputs are open collector (OUTSEL = L)

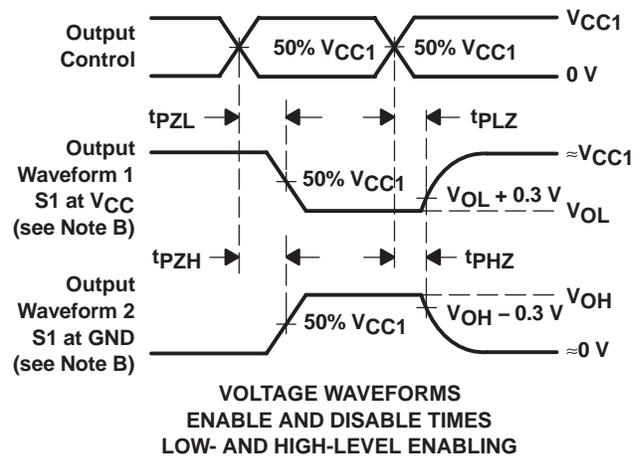
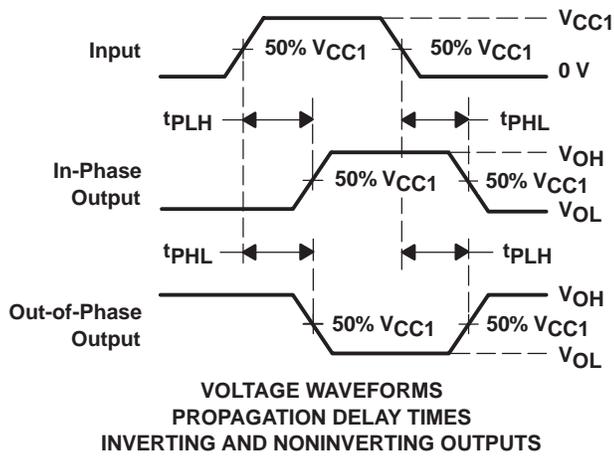
(3) When outputs are push-pull (OUTSEL = H)

(4) SOUT goes low when the data is received correctly and maintains a low level for one data-pulse period. Not tested, but specified by design.

PARAMETER MEASUREMENT INFORMATION
(PUSH-PULL OUTPUT)



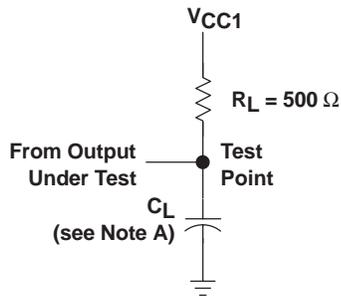
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	VCC1
t_{PHZ}/t_{PZH}	GND



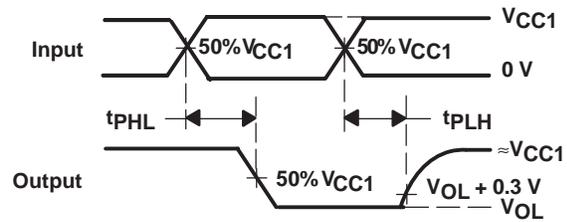
- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PZL} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
(OPEN-COLLECTOR OUTPUT)



**LOAD CIRCUIT FOR
 OPEN-COLLECTOR OUTPUTS**



**VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES**

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, t_f :
 C. The outputs are measured one at a time, with one input transition per measurement.
 D. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV8153N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV8153NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LV8153PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV8153PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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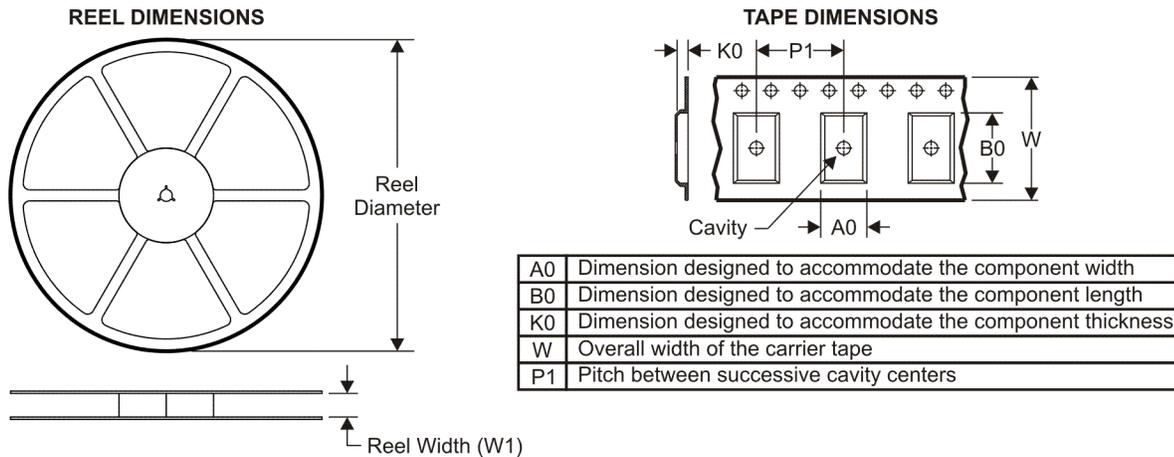
OTHER QUALIFIED VERSIONS OF SN74LV8153 :

- Automotive: [SN74LV8153-Q1](#)

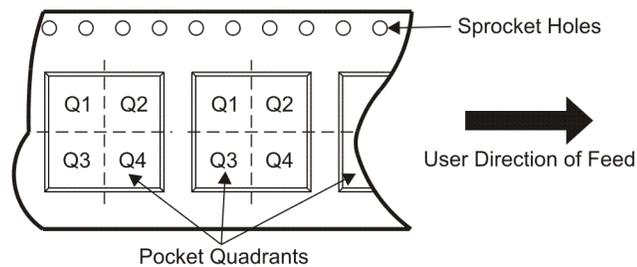
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8153PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8153PWR	TSSOP	PW	20	2000	346.0	346.0	33.0

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

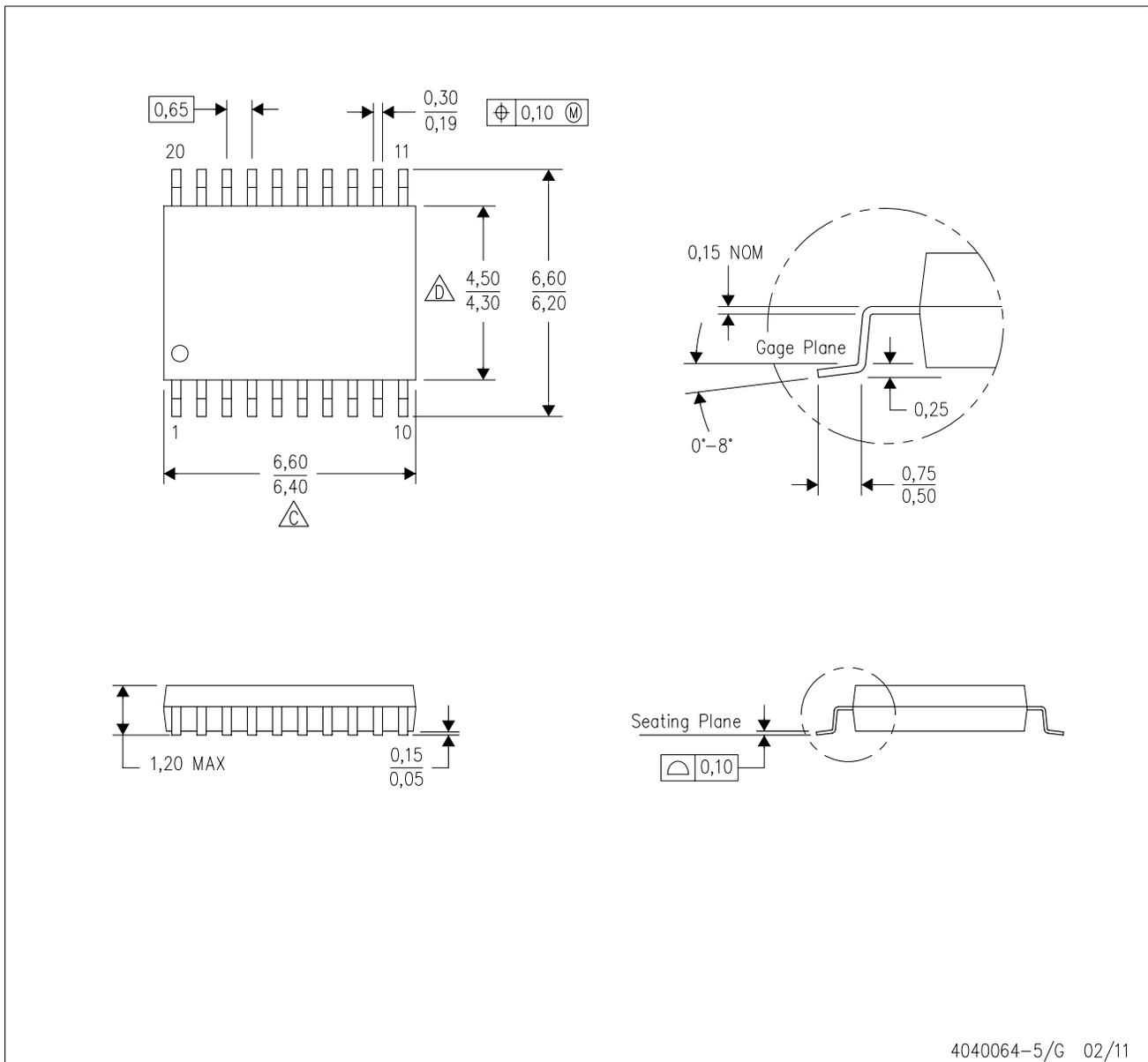
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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