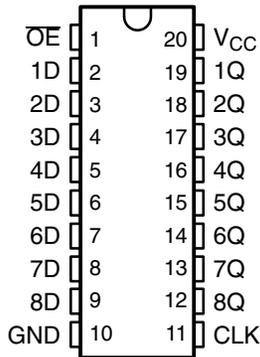


SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

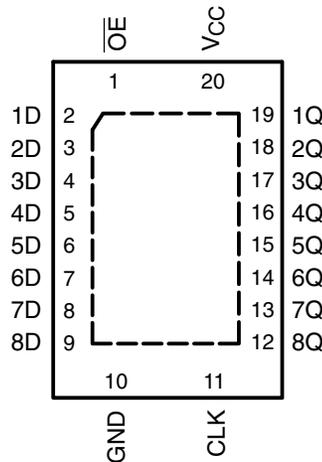
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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 10 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

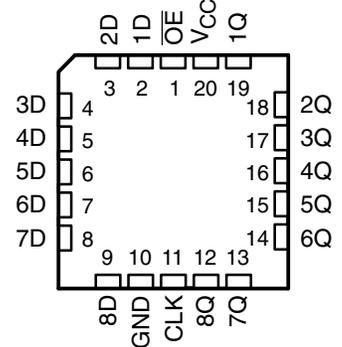
SN54LV574A . . . J OR W PACKAGE
SN74LV574A . . . DB, DGV, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV574A . . . RGY PACKAGE
(TOP VIEW)



SN54LV574A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------|----------------|-----------------------|------------------|
| -40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LV574ARGYR | LV574A |
| | SOIC – DW | Tube of 25 | SN74LV574ADW | LV574A |
| | | Reel of 2000 | SN74LV574ADWR | |
| | SOP – NS | Reel of 2000 | SN74LV574ANSR | 74LV574A |
| | SSOP – DB | Reel of 2000 | SN74LV574ADBR | LV574A |
| | TSSOP – PW | Tube of 70 | SN74LV574APW | LV574A |
| | | Reel of 2000 | SN74LV574APWR | |
| | | Reel of 250 | SN74LV574APWT | |
| TVSOP – DGV | Reel of 2000 | SN74LV574ADGVR | LV574A | |
| VFBGA – GQN | Reel of 1000 | SN74LV574AGQNR | LV574A | |
| -55°C to 125°C | CDIP – J | Tube of 20 | SNJ54LV574AJ | SNJ54LV574AJ |
| | CFP – W | Tube of 85 | SNJ54LV574AW | SNJ54LV574AW |
| | LCCC – FK | Tube of 55 | SNJ54LV574AFK | SNJ54LV574AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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description/ordering information (continued)

The 'LV574A devices are octal edge-triggered D-type flip-flops designed for 2-V to 5.5-V V_{CC} operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

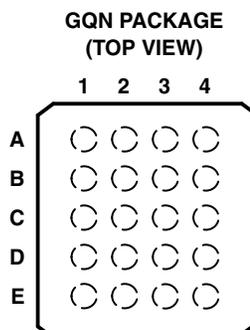
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.



terminal assignments

| | 1 | 2 | 3 | 4 |
|---|-----|-----------------|----------|----|
| A | 1D | \overline{OE} | V_{CC} | 1Q |
| B | 3D | 3Q | 2D | 2Q |
| C | 5D | 4D | 5Q | 4Q |
| D | 7D | 7Q | 6D | 6Q |
| E | GND | 8D | CLK | 8Q |

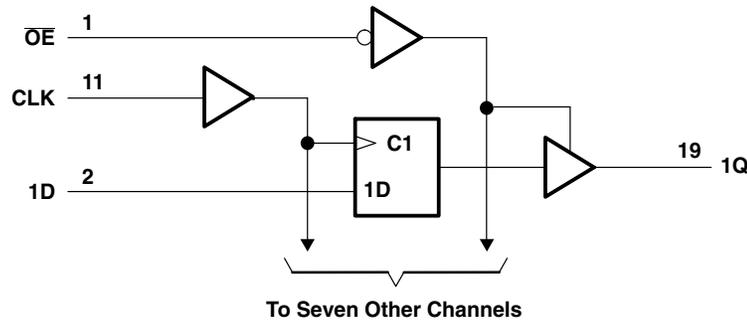
FUNCTION TABLE (each flip-flop)

| INPUTS | | | OUTPUT |
|-----------------|--------|---|--------|
| \overline{OE} | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|-----------------------------------------------------------------------------------------------------------|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | -0.5 V to 7 V |
| Output voltage range applied in the high or low state, V_O (see Notes 1 and 2) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -20 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 35 mA |
| Continuous current through V_{CC} or GND | ± 70 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DB package | 70°C/W |
| (see Note 3): DGV package | 92°C/W |
| (see Note 3): DW package | 58°C/W |
| (see Note 3): GQN package | 78°C/W |
| (see Note 3): NS package | 60°C/W |
| (see Note 3): PW package | 83°C/W |
| (see Note 4): RGY package | 37°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 2. This value is limited to 5.5 V maximum.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.
 4. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 5)

| | | SN54LV574A | | SN74LV574A | | UNIT | |
|---------------------|------------------------------------|-----------------------------------------|---------------------|---------------------|---------------------|--------------------|---|
| | | MIN | MAX | MIN | MAX | | |
| V_{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V | |
| V_{IH} | High-level input voltage | $V_{CC} = 2\text{ V}$ | 1.5 | 1.5 | | V | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.7$ | $V_{CC} \times 0.7$ | | | |
| V_{IL} | Low-level input voltage | $V_{CC} = 2\text{ V}$ | 0.5 | | 0.5 | V | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | $V_{CC} \times 0.3$ | | $V_{CC} \times 0.3$ | | |
| V_I | Input voltage | 0 | 5.5 | 0 | 5.5 | V | |
| V_O | Output voltage | High or low state | 0 | V_{CC} | 0 | V_{CC} | V |
| | | 3-state | 0 | 5.5 | 0 | 5.5 | |
| I_{OH} | High-level output current | $V_{CC} = 2\text{ V}$ | -50 | | -50 | μA | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | -2 | | -2 | mA | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | -8 | | -8 | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | -16 | | -16 | | |
| I_{OL} | Low-level output current | $V_{CC} = 2\text{ V}$ | 50 | | 50 | μA | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 2 | | 2 | mA | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 8 | | 8 | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 16 | | 16 | | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 200 | | 200 | ns/V | |
| | | $V_{CC} = 3\text{ V to }3.6\text{ V}$ | 100 | | 100 | | |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 20 | | 20 | | |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | $^{\circ}\text{C}$ | |

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | SN54LV574A | | | SN74LV574A | | | UNIT |
|-----------|-----------------------------------------------------|--------------|--------------|-----|--------------|------------|-----|---------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{OH} | $I_{OH} = -50\ \mu\text{A}$ | 2 V to 5.5 V | $V_{CC}-0.1$ | | $V_{CC}-0.1$ | | | V | |
| | $I_{OH} = -2\ \text{mA}$ | 2.3 V | 2 | | 2 | | | | |
| | $I_{OH} = -8\ \text{mA}$ | 3 V | 2.48 | | 2.48 | | | | |
| | $I_{OH} = -16\ \text{mA}$ | 4.5 V | 3.8 | | 3.8 | | | | |
| V_{OL} | $I_{OL} = 50\ \mu\text{A}$ | 2 V to 5.5 V | | | 0.1 | | | V | |
| | $I_{OL} = 2\ \text{mA}$ | 2.3 V | | | 0.4 | | | | |
| | $I_{OL} = 8\ \text{mA}$ | 3 V | | | 0.44 | | | | |
| | $I_{OL} = 16\ \text{mA}$ | 4.5 V | | | 0.55 | | | | |
| I_I | $V_I = 5.5\ \text{V or GND}$ | 0 to 5.5 V | | | ± 1 | | | μA | |
| I_{OZ} | $V_O = V_{CC}\ \text{or GND}$ | 5.5 V | | | ± 5 | | | μA | |
| I_{CC} | $V_I = V_{CC}\ \text{or GND, } I_O = 0$ | 5.5 V | | | 20 | | | μA | |
| I_{off} | $V_I\ \text{or } V_O = 0\ \text{to } 5.5\ \text{V}$ | 0 | | | 5 | | | μA | |
| C_i | $V_I = V_{CC}\ \text{or GND}$ | 3.3 V | 1.8 | | 1.8 | | | pF | |

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SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | | | $T_A = 25^\circ\text{C}$ | | SN54LV574A | | SN74LV574A | | UNIT |
|-----------|----------------|-----------------------------------|--------------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | CLK high or low | 7 | | 7 | | 7 | | ns |
| t_{su} | Setup time | High or low before CLK \uparrow | 5.5 | | 5.5 | | 5.5 | | ns |
| t_h | Hold time | Data after CLK \uparrow | 2 | | 2 | | 2 | | ns |

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | | | $T_A = 25^\circ\text{C}$ | | SN54LV574A | | SN74LV574A | | UNIT |
|-----------|----------------|-----------------------------------|--------------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | CLK high or low | 5 | | 5 | | 5 | | ns |
| t_{su} | Setup time | High or low before CLK \uparrow | 3.5 | | 3.5 | | 3.5 | | ns |
| t_h | Hold time | Data after CLK \uparrow | 1.5 | | 1.5 | | 1.5 | | ns |

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | | | $T_A = 25^\circ\text{C}$ | | SN54LV574A | | SN74LV574A | | UNIT |
|-----------|----------------|-----------------------------------|--------------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_w | Pulse duration | CLK high or low | 5 | | 5 | | 5 | | ns |
| t_{su} | Setup time | High or low before CLK \uparrow | 3.5 | | 3.5 | | 3.5 | | ns |
| t_h | Hold time | Data after CLK \uparrow | 1.5 | | 1.5 | | 1.5 | | ns |

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV574A | | SN74LV574A | | UNIT |
|-------------|-----------------|-------------|----------------------|--------------------------|-------|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | $C_L = 15\text{ pF}$ | 60* | 100* | | 50* | | 50 | MHz | |
| | | | $C_L = 50\text{ pF}$ | 50 | 85 | | 40 | | 40 | | |
| t_{pd} | CLK | Q | $C_L = 15\text{ pF}$ | 9.6* | 16.6* | | 1* | 20* | 1 | 20 | ns |
| t_{en} | \overline{OE} | Q | | 9.2* | 16.1* | | 1* | 19* | 1 | 19 | |
| t_{dis} | \overline{OE} | Q | | 6.5* | 12.8* | | 1* | 15* | 1 | 15 | |
| t_{pd} | CLK | Q | $C_L = 50\text{ pF}$ | 11.6 | 19.6 | | 1 | 23 | 1 | 23 | ns |
| t_{en} | \overline{OE} | Q | | 10.9 | 19 | | 1 | 22 | 1 | 22 | |
| t_{dis} | \overline{OE} | Q | | 8.4 | 17.5 | | 1 | 20 | 1 | 20 | |
| $t_{sk(o)}$ | | | | | | 2 | | | | 2 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ C$ | | | SN54LV574A | | SN74LV574A | | UNIT |
|-------------|-----------------|-------------|-----------------------|--------------------|------|-------|------------|-------|------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | $C_L = 15 \text{ pF}$ | 80* | 145* | | 65* | | 65 | | MHz |
| | | | $C_L = 50 \text{ pF}$ | 50 | 120 | | 45 | | 45 | | |
| t_{pd} | CLK | Q | $C_L = 15 \text{ pF}$ | | 6.8* | 13.2* | 1* | 15.5* | 1 | 15.5 | ns |
| t_{en} | \overline{OE} | Q | | | 6.4* | 12.8* | 1* | 15* | 1 | 15 | |
| t_{dis} | \overline{OE} | Q | | | 4.8* | 13* | 1* | 15* | 1 | 15 | |
| t_{pd} | CLK | Q | $C_L = 50 \text{ pF}$ | | 8.1 | 16.7 | | | 19 | 19 | ns |
| t_{en} | \overline{OE} | Q | | | 7.7 | 16.3 | 1 | 18.5 | 1 | 18.5 | |
| t_{dis} | \overline{OE} | Q | | | 6.1 | 15 | 1 | 17 | 1 | 17 | |
| $t_{sk(o)}$ | | | | | | | 1.5 | | | 1.5 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ C$ | | | SN54LV574A | | SN74LV574A | | UNIT |
|-------------|-----------------|-------------|-----------------------|--------------------|------|------|------------|-------|------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | $C_L = 15 \text{ pF}$ | 130* | 205* | | 110* | | 110 | | MHz |
| | | | $C_L = 50 \text{ pF}$ | 85 | 175 | | 75 | | 75 | | |
| t_{pd} | CLK | Q | $C_L = 15 \text{ pF}$ | | 4.8* | 8.6* | 1* | 10* | 1 | 10 | ns |
| t_{en} | \overline{OE} | Q | | | 4.6* | 9* | 1* | 10.5* | 1 | 10.5 | |
| t_{dis} | \overline{OE} | Q | | | 3.5* | 9* | 1* | 10.5* | 1 | 10.5 | |
| t_{pd} | CLK | Q | $C_L = 50 \text{ pF}$ | | 5.7 | 10.6 | | | 12 | 12 | ns |
| t_{en} | \overline{OE} | Q | | | 5.5 | 11 | 1 | 12.5 | 1 | 12.5 | |
| t_{dis} | \overline{OE} | Q | | | 4.1 | 10.1 | 1 | 11.5 | 1 | 11.5 | |
| $t_{sk(o)}$ | | | | | | | 1 | | | 1 | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3 V$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ C$ (see Note 6)

| PARAMETER | | SN74LV574A | | | UNIT |
|-------------|----------------------------------------|------------|------|------|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.7 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.6 | -0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 2.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 0.99 | | V |

NOTE 6: Characteristics are for surface-mount packages only.

operating characteristics, $T_A = 25^\circ C$

| PARAMETER | | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|-----------|-------------------------------|-----------------|-----------------------------------------------------------------|-------|------|
| C_{pd} | Power dissipation capacitance | | Outputs enabled $C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$ | 3.3 V | |
| | | | 5 V | 23.8 | |

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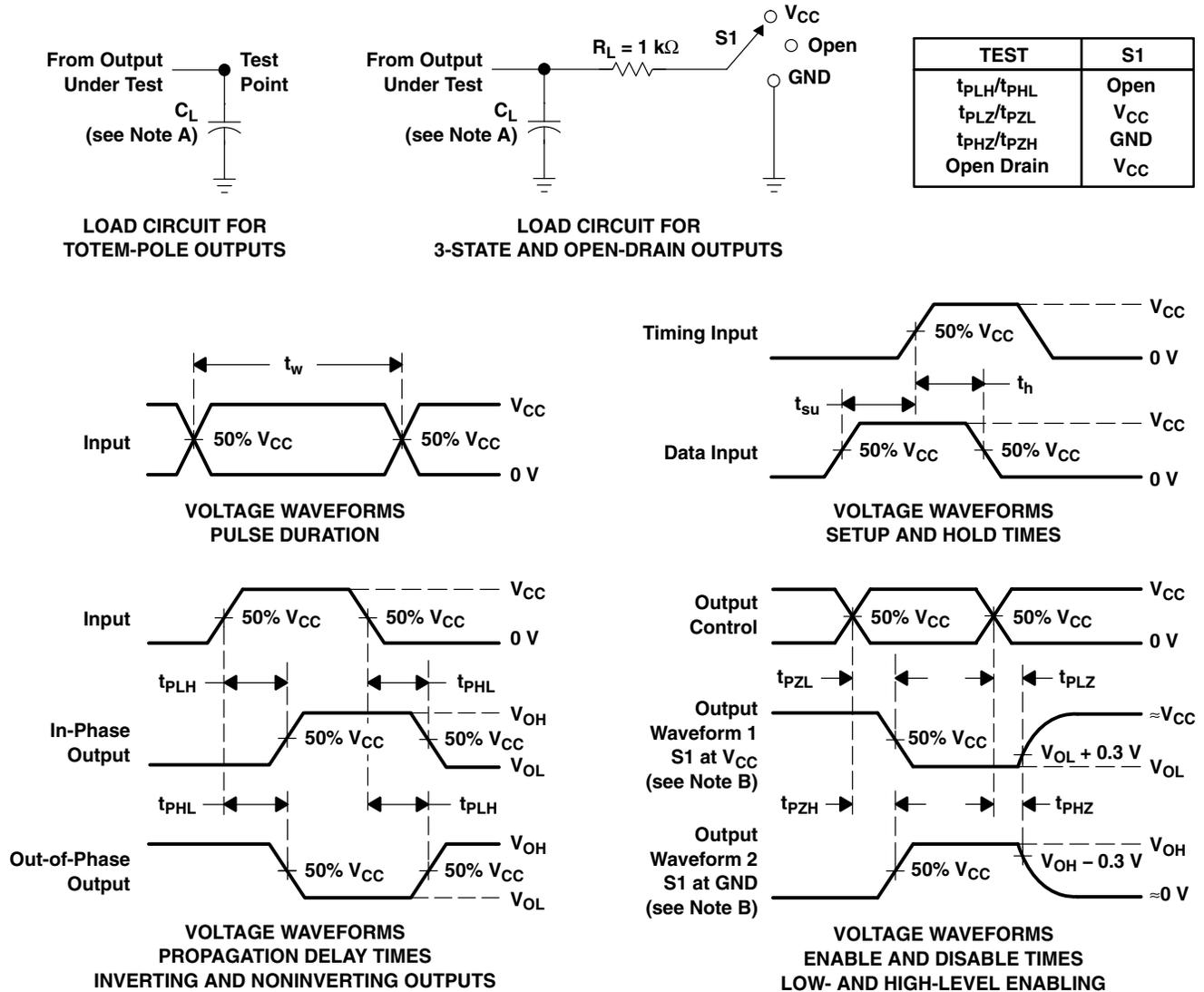


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SN54LV574A, SN74LV574A OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV574ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADGVRE4 | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADGVRG4 | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV574A | Samples |
| SN74LV574ANSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV574A | Samples |
| SN74LV574ANSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV574A | Samples |
| SN74LV574APW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574APWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV574APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574APWT | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574APWTE4 | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574APWTG4 | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV574A | Samples |
| SN74LV574ARGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LV574A | Samples |
| SN74LV574ARGYRG4 | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | LV574A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION

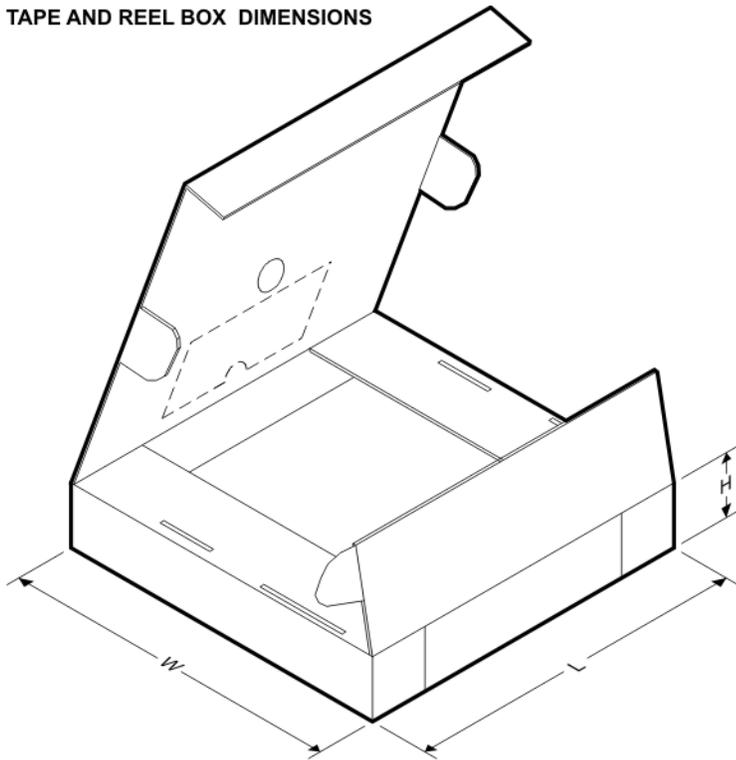


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV574ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV574ADGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV574ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LV574ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LV574APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV574APWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV574ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


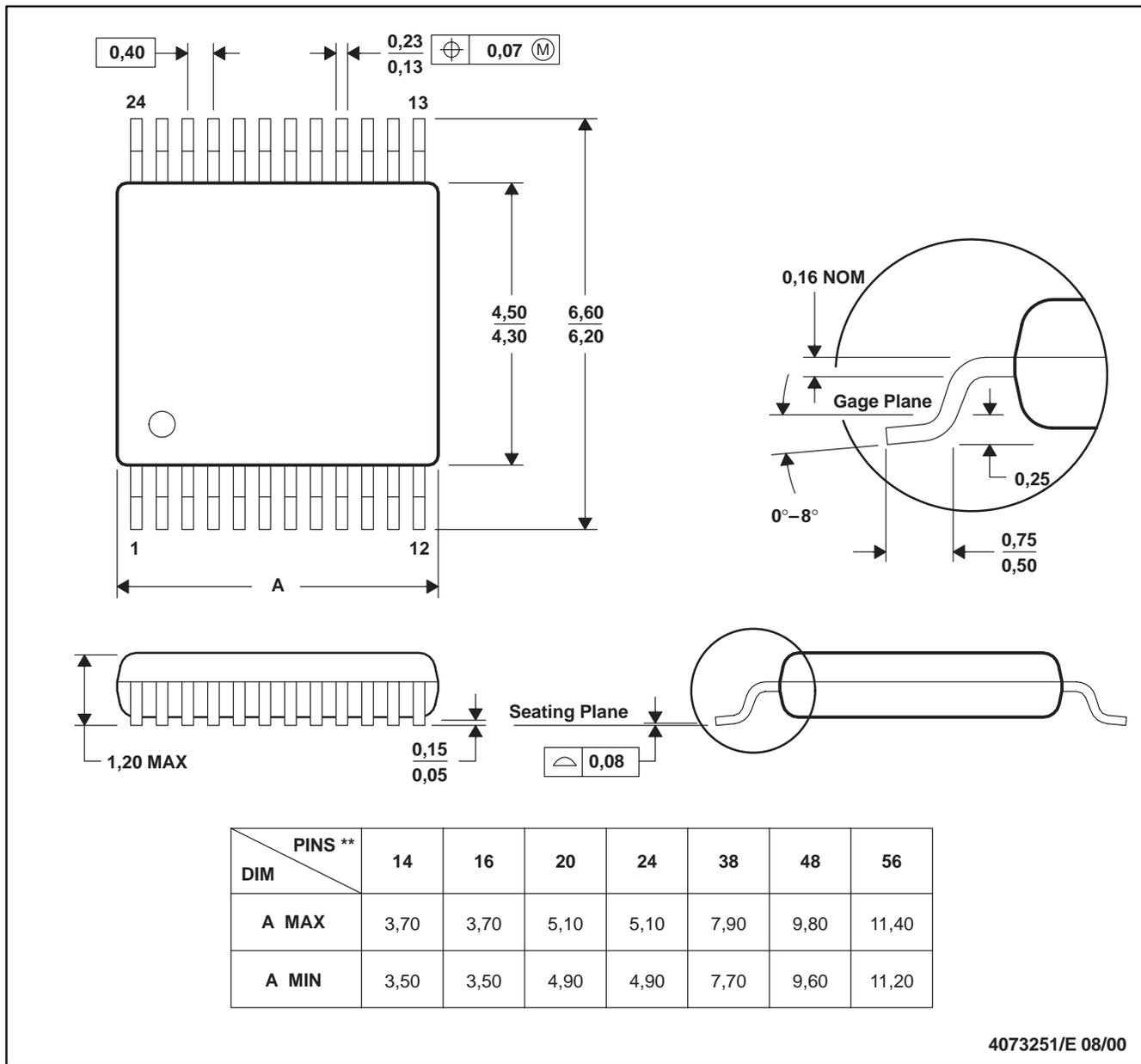
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV574ADBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV574ADGVR | TVSOP | DGV | 20 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV574ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV574ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV574APWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV574APWT | TSSOP | PW | 20 | 250 | 367.0 | 367.0 | 38.0 |
| SN74LV574ARGYR | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

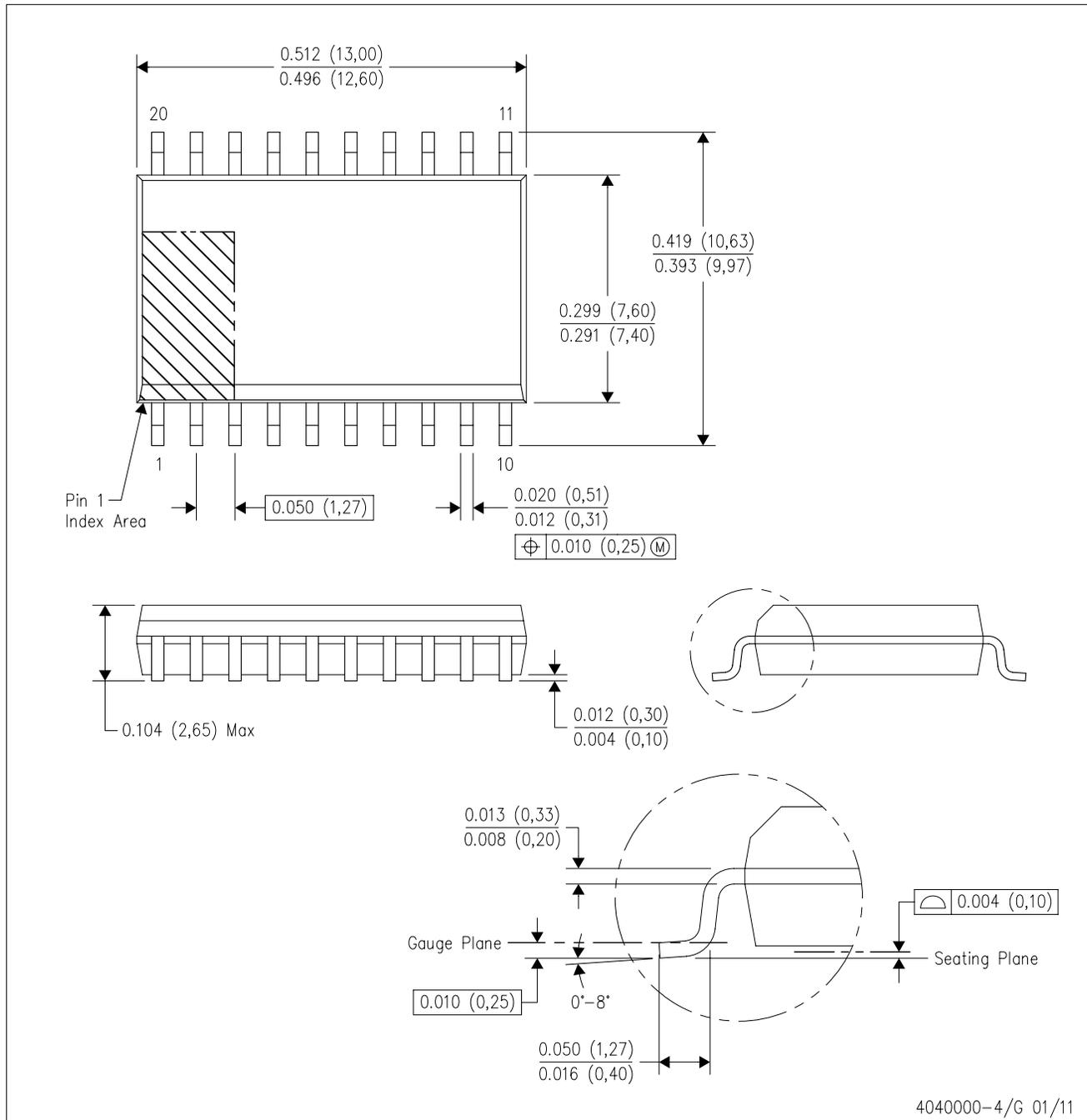
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

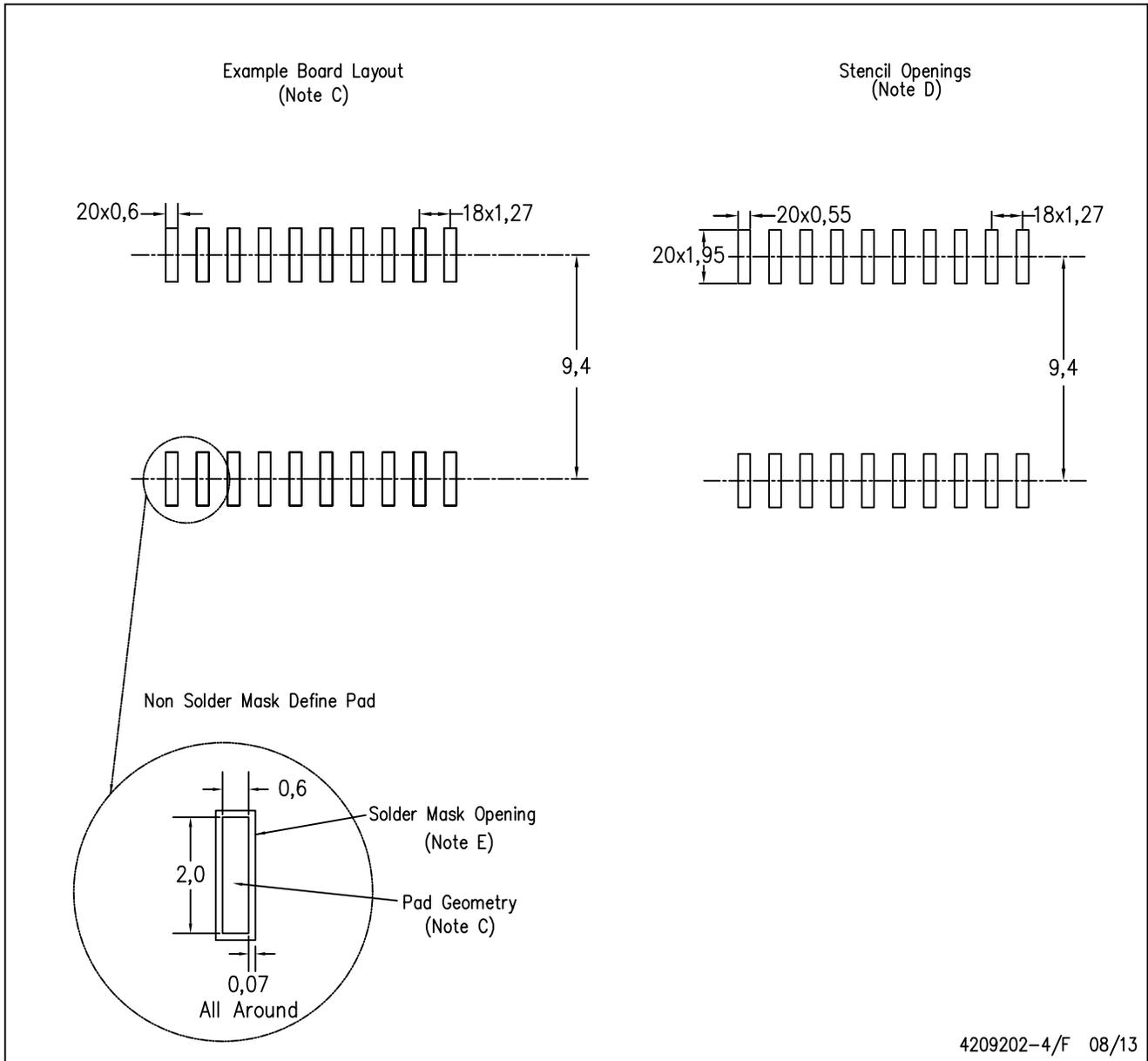
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

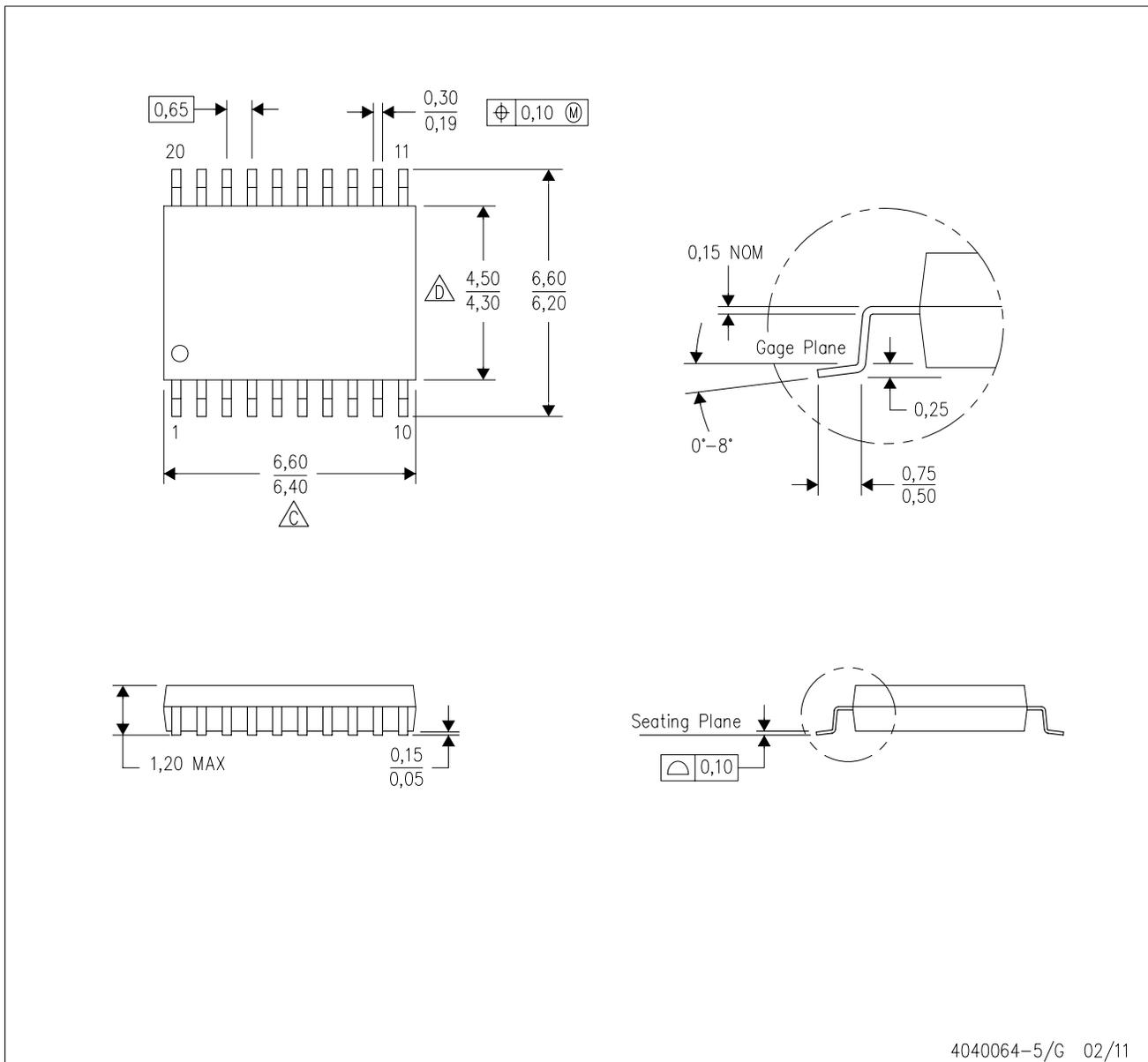
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

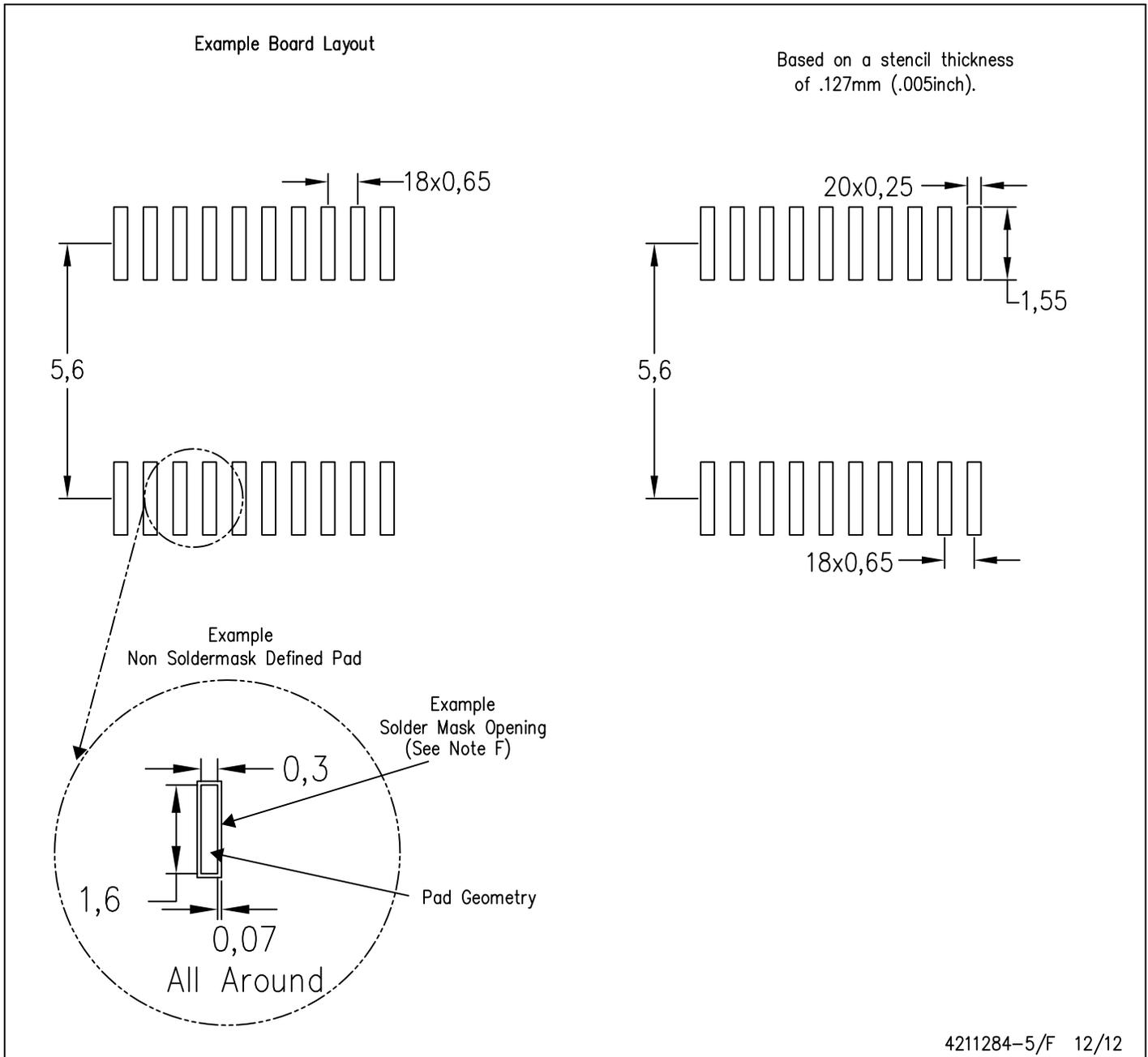


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

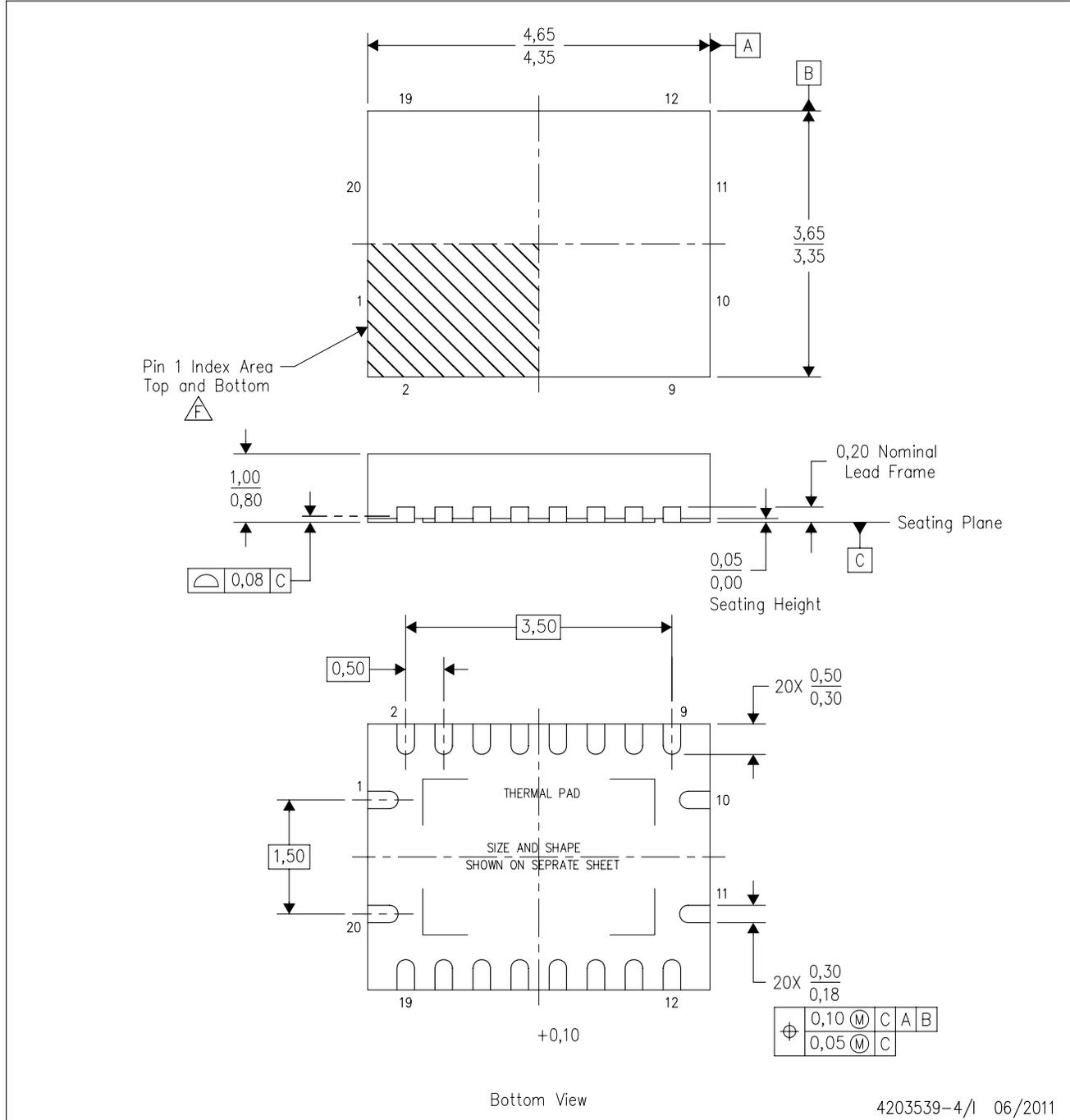
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

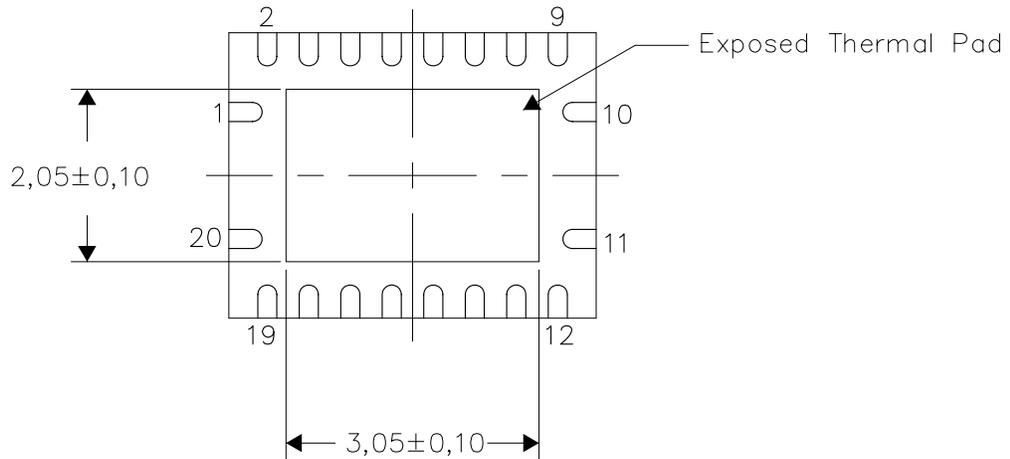
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

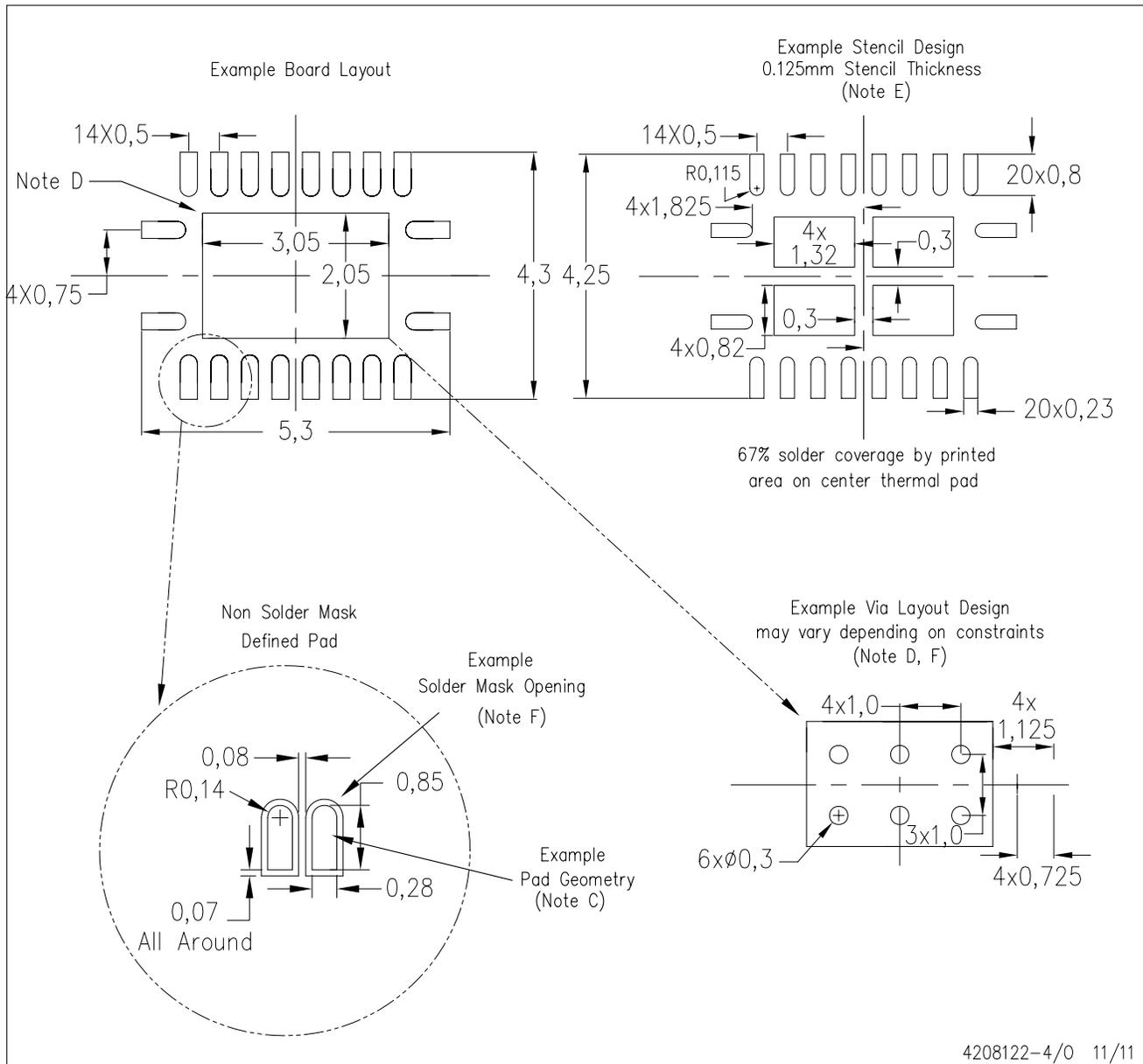
Exposed Thermal Pad Dimensions

4206353-4/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-4/0 11/11

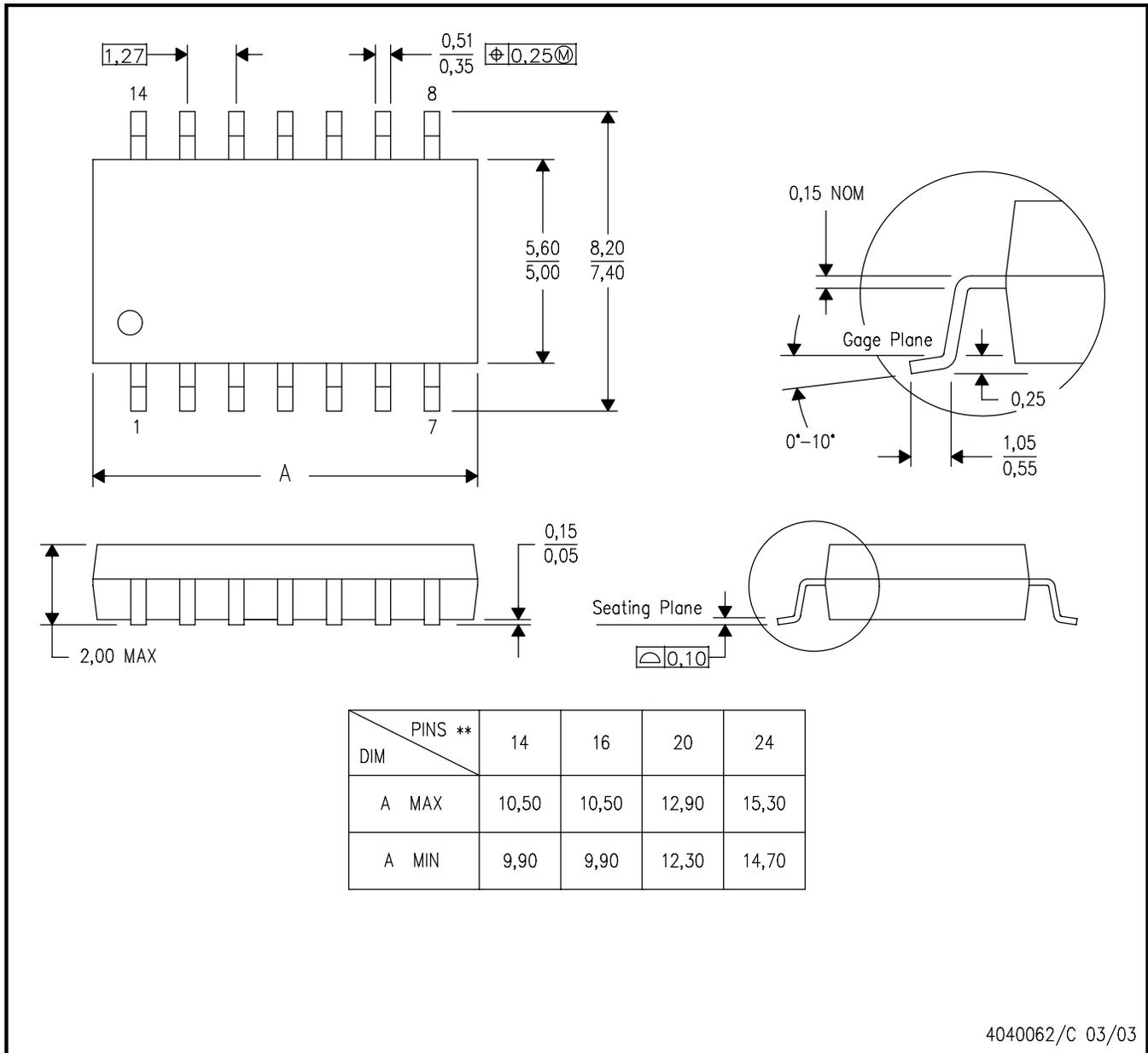
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

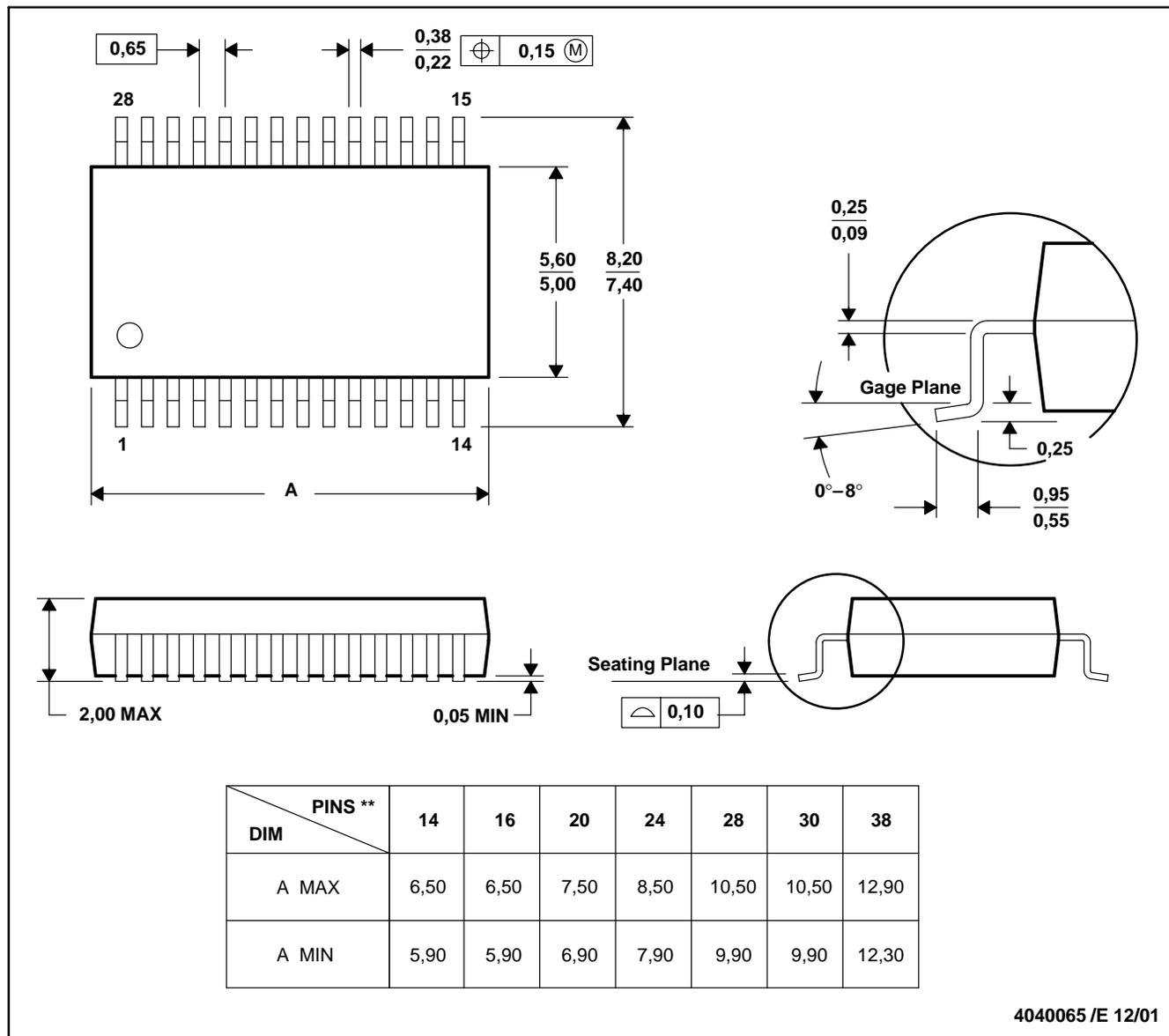


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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