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- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 7 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce)
 <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot)
 >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

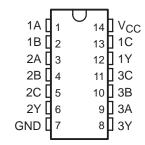
description/ordering information

These triple 3-input positive-NOR gates are designed for 2-V to 5.5-V V_{CC} operation.

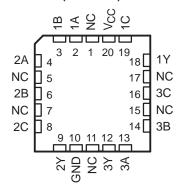
The 'LV27A devices perform the Boolean function $Y = \overline{A} + \overline{B} + \overline{C}$ or $Y = \overline{A} \bullet \overline{B} \bullet \overline{C}$ in positive logic.

These devices are fully specified for partial-power-down applications using $I_{\rm off}$. The $I_{\rm off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

SN54LV27A . . . J OR W PACKAGE SN74LV27A . . . D, DB, DGV, NS, OR PW PACKAGE (TOP VIEW)



SN54LV27A . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

TA	PACKA	GEŤ	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	0010 D	Tube of 50	SN74LV27AD	11/074
	SOIC - D	Reel of 2500	SN74LV27ADR	LV27A
4000 (- 0500	SOP – NS	Reel of 2000	SN74LV27ANSR	74LV27A
	SSOP – DB	Reel of 2000	SN74LV27ADBR	LV27A
-40°C to 85°C		Tube of 90	SN74LV27APW	
	TSSOP – PW	Reel of 2000	SN74LV27APWR	LV27A
		Reel of 250	SN74LV27APWT	
	TVSOP – DGV	Reel of 2000	SN74LV27ADGVR	LV27A
	CDIP – J	Tube of 25	SNJ54LV27AJ	SNJ54LV27AJ
–55°C to 125°C	CFP – W	Tube of 150	SNJ54LV27AW	SNJ54LV27AW
	LCCC – FK	Tube of 55	SNJ54LV27AFK	SNJ54LV27AFK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



FUNCTION TABLE (each gate)

	INPUTS	OUTPUT	
Α	В	С	Y
Н	Х	Χ	L
X	Н	Χ	L
Х	X	Н	L
L	L	L	Н

logic diagram, each gate (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	e, V _O (see Notes 1 and 2), V _O (see Note 1) D package DB package DGV package NS package PW package	-0.5 V to 7 V -0.5 V to V _{CC} + 0.5 V -0.5 V to 7 V -20 mA -50 mA ±25 mA ±50 mA 86°C/W 96°C/W 127°C/W 113°C/W
Storage temperature range, T _{stg}		05 6 10 150 6

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
 - 2. This value is limited to 5.5 V maximum.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.



recommended operating conditions (see Note 4)

			SN54L\	/27A	SN74L	UNIT	
			MIN	MAX	MIN	MAX	UNII
Vcc	Supply voltage		2	5.5	2	5.5	V
		V _{CC} = 2 V	1.5		1.5		
V	High level innerteelte as	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V _{CC} ×0.7		$V_{CC} \times 0.7$		V
VIH	High-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V _{CC} = 2 V		0.5		0.5	
V.	Low-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	V	$CC \times 0.3$	V	CC×0.3	V
VIL	Low-level input voltage	$V_{CC} = 3 V \text{ to } 3.6 V$	V	$CC \times 0.3$	V	CC×0.3	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	V _{CC} × 0.3		V	$V_{CC} \times 0.3$	
٧ı	Input voltage		0,0	5.5	0	5.5	V
٧o	Output voltage		0	VCC	0	VCC	V
		V _{CC} = 2 V	S. S	-50		-50	μΑ
la	High-level output current	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-2		-2	
Іон	nigii-level output current	$V_{CC} = 3 V \text{ to } 3.6 V$		-6		-6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		-12		-12	
		$V_{CC} = 2 V$		50		50	μΑ
	Low lovel output ourrent	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2		2	
lOL	Low-level output current	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		6		6	mA
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		12		12	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		200		200	
Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		100		100	ns/V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		20		20	
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TOT COMPLETIONS		SN54LV27A	SN74LV27A		
PARAMETER	TEST CONDITIONS	VCC	MIN TYP MAX	MIN TYP MAX	UNIT	
	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} -0.1	V _{CC} -0.1		
.,	$I_{OH} = -2 \text{ mA}$	2.3 V	2	2	.,	
VOH	I _{OH} = -6 mA	3 V	2.48	2.48	_ v	
	I _{OH} = -12 mA	4.5 V	3.8	3.8		
	I _{OL} = 50 μA	2 V to 5.5 V	0.1	0.1	1	
	I _{OL} = 2 mA	2.3 V	0.4	0.4	V	
VOL	I _{OL} = 6 mA	3 V	0.44	0.44	V	
	I _{OL} = 12 mA	4.5 V	0.55	0.55		
lį	V _I = 5.5 V or GND	0 to 5.5 V	±1	±1	μΑ	
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V	20	20	μΑ	
l _{off}	V_I or $V_O = 0$ to 5.5 V	0	5	5	μΑ	
Ci	V _I = V _{CC} or GND	3.3 V	1.9	1.9	pF	

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V \pm 0.2 V (unless otherwise noted) (see Figure 1)

DADAMETER	FROM	то	LOAD	T,	4 = 25°C	;	SN54LV27A	SN74L	.V27A	
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
t _{pd}	A, B, or C	Υ	C _L = 15 pF		6.7*	13.8*	1* 16*	1	16	ns
t _{pd}	A, B, or C	Υ	C _L = 50 pF		9.5	17.5	1 21	1	21	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	չ = 25°C	;	SN54LV27A	SN74L	.V27A	LINUT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT
t _{pd}	A, B, or C	Υ	C _L = 15 pF		5*	8.8*	1* 10.5*	1	10.5	ns
t _{pd}	A, B, or C	Υ	C _L = 50 pF		6.9	12.3	1 14	1	14	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	4 = 25°C	;	SN54LV27A	SN74L	V27A	LINUT
PARAMETER (INPUT) (OUTPUT) CAPA		CAPACITANCE	MIN	TYP	MAX	MIN MAX	MIN	MAX	UNIT	
t _{pd}	A, B, or C	Υ	C _L = 15 pF		3.9*	5.9*	1* 7*	1	7	ns
t _{pd}	A, B, or C	Υ	C _L = 50 pF		5.2	7.9	21 9	1	9	ns

^{*} On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^{\circ}\text{C}$ (see Note 5)

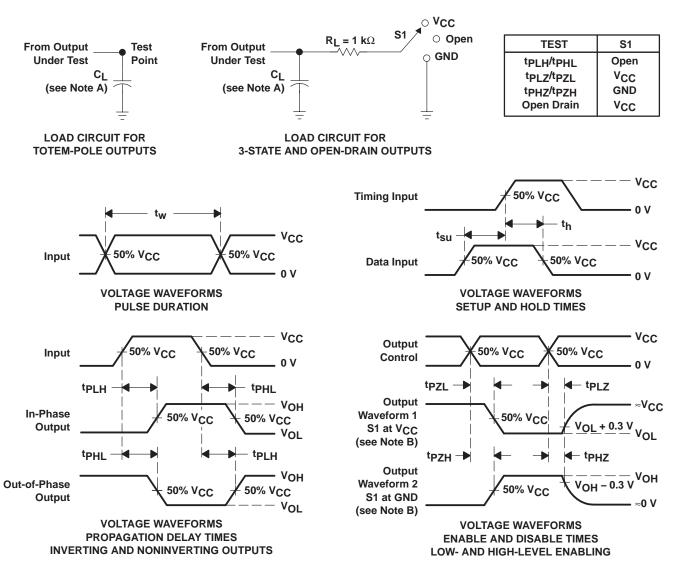
	DADAMETED		SN74LV27A			
	PARAMETER	MIN	TYP	MAX	UNIT	
VOL(P)	Quiet output, maximum dynamic VOL		0.2	0.8	V	
VOL(V)	Quiet output, minimum dynamic V _{OL}		0	-0.8	V	
VOH(V)	Quiet output, minimum dynamic VOH		3.2		V	
VIH(D)	High-level dynamic input voltage	2.31			V	
V _{IL(D)}	Low-level dynamic input voltage			0.99	V	

NOTE 5: Characteristics are for surface-mount packages only.

operating characteristics, T_A = 25°C

		PARAMETER	TEST CO	VCC	TYP	UNIT	
ſ	<u> </u>	Down discination consistence	C:	f 40 MH-	3.3 V	13.7	pF
L	Cpd	Power dissipation capacitance	$C_L = 50 \text{ pF},$	f = 10 MHz	5 V	15	pΕ

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_Q = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. tpLZ and tpHZ are the same as tdis.
- F. tpzi and tpzH are the same as ten.
- G. tpHL and tpLH are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LV27AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADGVR	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADGVRE4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADGVRG4	ACTIVE	TVSOP	DGV	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ADRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ANSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ANSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27ANSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APWTE4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV27APWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

 $^{^{(1)}}$ The marketing status values are defined as follows:



PACKAGE OPTION ADDENDUM

18-Sep-2008

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

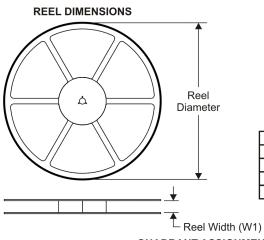
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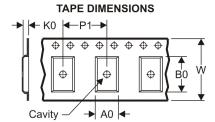
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PACKAGE MATERIALS INFORMATION

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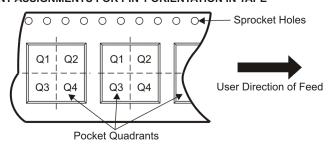
TAPE AND REEL INFORMATION





_		
		Dimension designed to accommodate the component width
Γ	B0	Dimension designed to accommodate the component length
	K0	Dimension designed to accommodate the component thickness
Γ	W	Overall width of the carrier tape
Γ	P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV27ADBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LV27ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV27ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV27ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV27APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV27APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV27ADBR	SSOP	DB	14	2000	346.0	346.0	33.0
SN74LV27ADGVR	TVSOP	DGV	14	2000	346.0	346.0	29.0
SN74LV27ADR	SOIC	D	14	2500	346.0	346.0	33.0
SN74LV27ANSR	SO	NS	14	2000	346.0	346.0	33.0
SN74LV27APWR	TSSOP	PW	14	2000	346.0	346.0	29.0
SN74LV27APWT	TSSOP	PW	14	250	346.0	346.0	29.0

DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

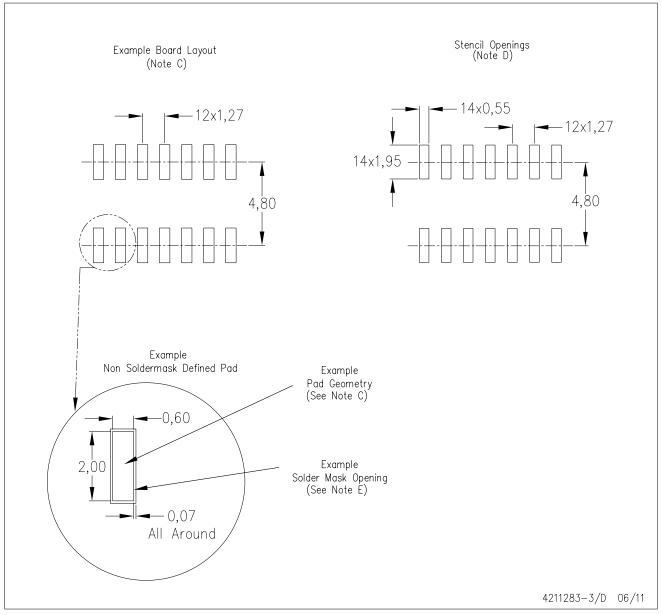


- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

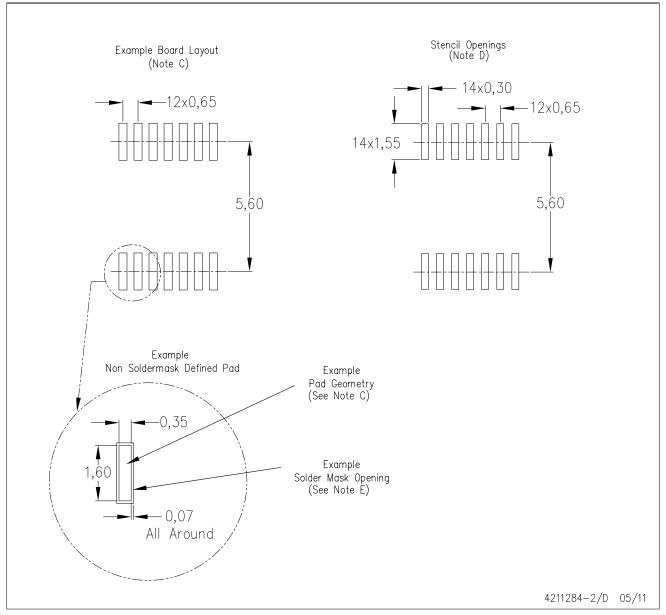


- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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