

The SN5405 is obsolete  
and no longer is supplied.

# SN54LS05, SN54S05 SN7405, SN74LS05, SN74S05 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

SDLS030A – DECEMBER 1983 – REVISED NOVEMBER 2003

- Package Options Include Plastic Small-Outline (D, NS), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

- Dependable Texas Instrument Quality and Reliability

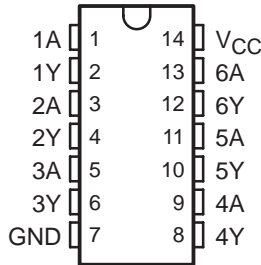
SN5405, SN54LS05, SN54S05 . . . J PACKAGE

SN7405 . . . N PACKAGE

SN74LS05 . . . D, DB, N, OR NS PACKAGE

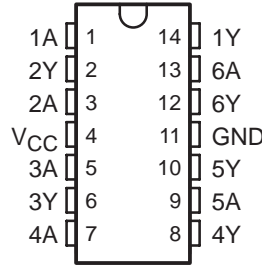
SN74S05 . . . D, N, OR NS PACKAGE

(TOP VIEW)



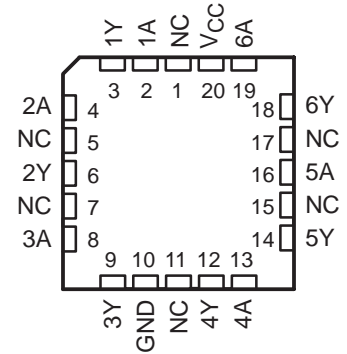
SN54LS05, SN54S05 . . . W PACKAGE

(TOP VIEW)



SN54LS05, SN54S05 . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection

## description/ordering information

These devices contain six independent inverters. To perform correctly, the open-collector outputs require pullup resistors. These devices may be connected to other open-collector outputs to implement active-low wired-OR or active-high wire-AND functions. Open-collector devices often are used to generate high  $V_{OH}$  levels.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN7405N	SN7405N
			SN74LS05N	SN74LS05N
			SN74S05N	SN74S05N
	SOIC – D	Tube	SN74LS05D	LS05
		Tape and reel	SN74LS05DR	
		Tube	SN74S05D	S05
		Tape and reel	SN74S05DR	
	SOP – NS	Tape and reel	SN74LS05NSR	74LS05
–55°C to 125°C	CDIP – J	Tube	SNJ54LS05J	SNJ54LS05J
			SNJ54S05J	SNJ54S05J
	CDIP – W	Tube	SNJ54LS05W	SNJ54LS05W
			SNJ54S05W	SNJ54S05W
	LCCC – FK	Tube	SNJ54LS05FK	SNJ54LS05FK
			SNJ54S05FK	SNJ54S05FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54LS05, SN54S05  
SN7405, SN74LS05, SN74S05  
HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

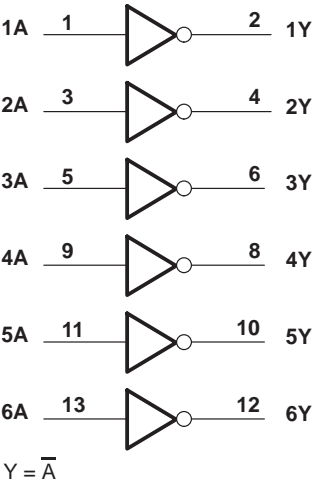
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FUNCTION TABLE  
(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)

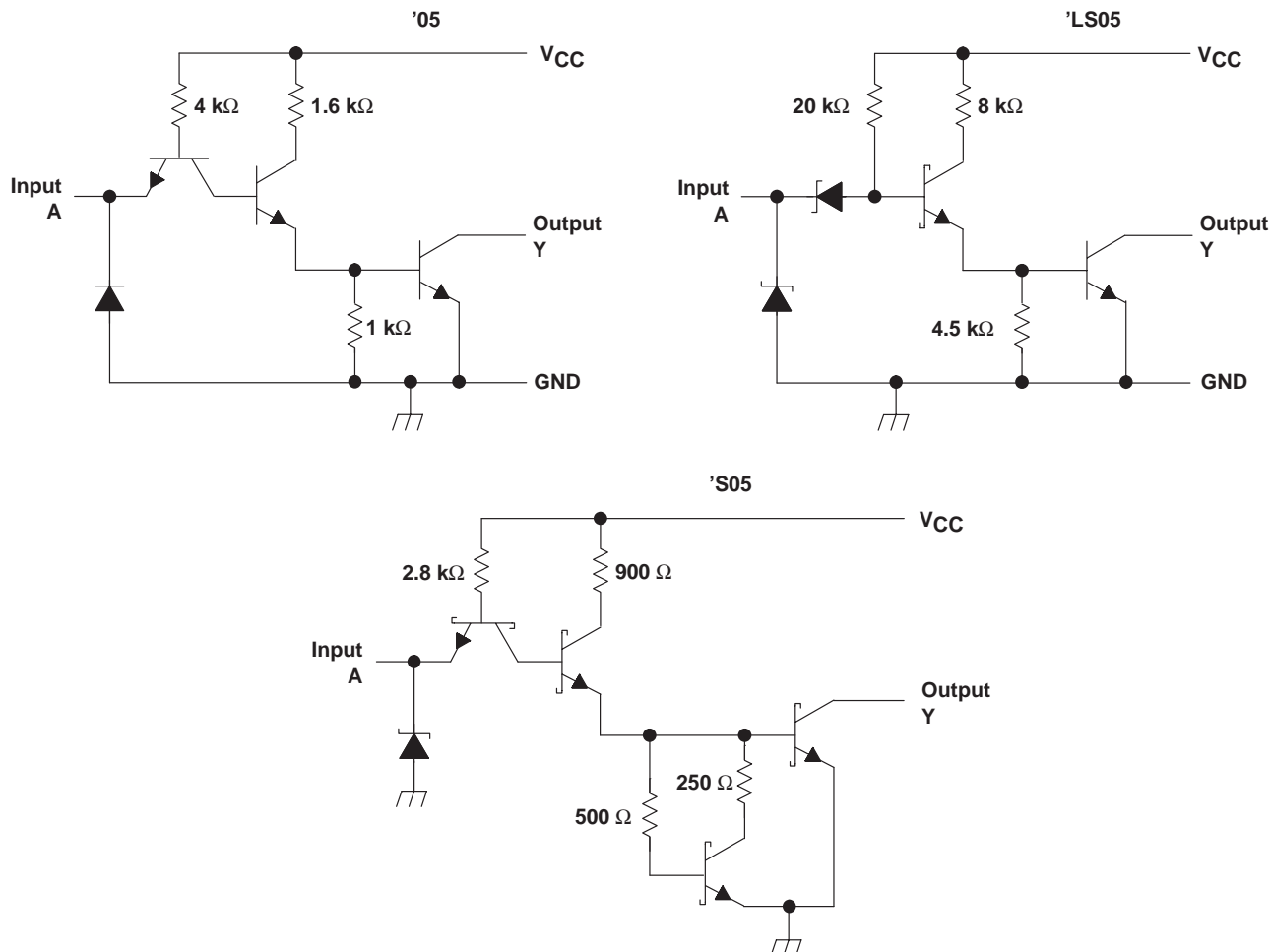


Pin numbers shown are for the D, DB, J, N, and NS packages.

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# SN54LS05, SN54S05 SN7405, SN74LS05, SN74S05 HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS SDLS030A – DECEMBER 1983 – REVISED NOVEMBER 2003

## schematic (each inverter)



Resistor values shown are nominal.

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$ (see Note 1): '05, 'LS05, 'S05	7 V
Input voltage, $V_I$ : '05, 'S05	5.5 V
'LS05	7 V
Off-state output voltage, $V_O$	7 V
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network ground terminal.

2. The package thermal impedance is calculated in accordance with JESD 51-7.



**SN54LS05, SN54S05**  
**SN7405, SN74LS05, SN74S05**  
**HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

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**recommended operating conditions**

		SN5405			SN7405			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_{OH}$	High-level output voltage			5.5			5.5	V
$I_{OL}$	Low-level output current			16			16	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†		SN5405			SN7405			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN},$	$I_I = -12 \text{ mA}$			–1.5			–1.5	V
$I_{OH}$	$V_{CC} = \text{MIN},$	$V_{OH} = 5.5 \text{ V}$						0.25	mA
		$V_{IL} = 0.8 \text{ V}$ $V_{IL} = 0.7 \text{ V}$			0.25				
$V_{OL}$	$V_{CC} = \text{MIN},$	$V_{IH} = 2 \text{ V},$			0.2			0.2	V
		$I_{OL} = 16 \text{ mA}$			0.4			0.4	
$I_I$	$V_{CC} = \text{MAX},$	$V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX},$	$V_I = 2.4 \text{ V}$			40			40	µA
$I_{IL}$	$V_{CC} = \text{MAX},$	$V_I = 0.4 \text{ V}$			–1.6			–1.6	mA
$I_{CCH}$	$V_{CC} = \text{MAX},$	$V_I = 0 \text{ V}$			6			6	12
					12			12	mA
$I_{CCL}$	$V_{CC} = \text{MAX},$	$V_I = 4.5 \text{ V}$			18			18	33
					33			33	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}.$

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$  (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	A	Y	$R_L = 4 \text{ k}\Omega$	$C_L = 15 \text{ pF}$		40	55	ns
$t_{PHL}$			$R_L = 400 \Omega$			8	15	



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**SN54LS05, SN54S05**  
**SN7405, SN74LS05, SN74S05**  
**HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**  
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**recommended operating conditions**

		SN54LS05			SN74LS05			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage			0.7			0.8	V
V <sub>OH</sub>	High-level output voltage			5.5			5.5	V
I <sub>OL</sub>	Low-level output current			4			8	mA
T <sub>A</sub>	Operating free-air temperature	–55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54LS05			SN74LS05			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = –18 mA			–1.5			–1.5	V
I <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>OH</sub> = 5.5 V			0.1			0.1	mA
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V			0.25			0.25	V
	I <sub>OL</sub> = 4 mA						0.35	
	I <sub>OL</sub> = 8 mA						0.5	
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1			0.1	mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20			20	μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			–0.4			–0.4	mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0 V			1.2			1.2	mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 4.5 V			3.6			3.6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

**switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C (see Figure 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	A	Y	R <sub>L</sub> = 2 kΩ, C <sub>L</sub> = 15 pF		17	32	ns
t <sub>PHL</sub>					15	28	



**SN54LS05, SN54S05**  
**SN7405, SN74LS05, SN74S05**  
**HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

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**recommended operating conditions**

		SN54S05			SN74S05			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	2			2			V
$V_{IL}$	Low-level input voltage			0.8			0.8	V
$V_{OH}$	High-level output voltage			5.5			5.5	V
$I_{OL}$	Low-level output current			20			20	mA
$T_A$	Operating free-air temperature	–55		125	0		70	°C

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†		SN54S05			SN74S05			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN},$	$I_I = -18 \text{ mA}$			–1.2			–1.2	V
$I_{OH}$	$V_{CC} = \text{MIN},$	$V_{OH} = 5.5 \text{ V}$						0.25	mA
		$V_{IL} = 0.8 \text{ V}$ $V_{IL} = 0.7 \text{ V}$			0.25				
$V_{OL}$	$V_{CC} = \text{MIN},$	$V_{IH} = 2 \text{ V},$			0.5			0.5	V
		$I_{OL} = 20 \text{ mA}$							
$I_I$	$V_{CC} = \text{MAX},$	$V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX},$	$V_I = 2.7 \text{ V}$			50			50	µA
$I_{IL}$	$V_{CC} = \text{MAX},$	$V_I = 0.5 \text{ V}$			–2			–2	mA
$I_{CCH}$	$V_{CC} = \text{MAX},$	$V_I = 0 \text{ V}$			9			9	19.8
$I_{CCL}$	$V_{CC} = \text{MAX},$	$V_I = 4.5 \text{ V}$			30			30	54

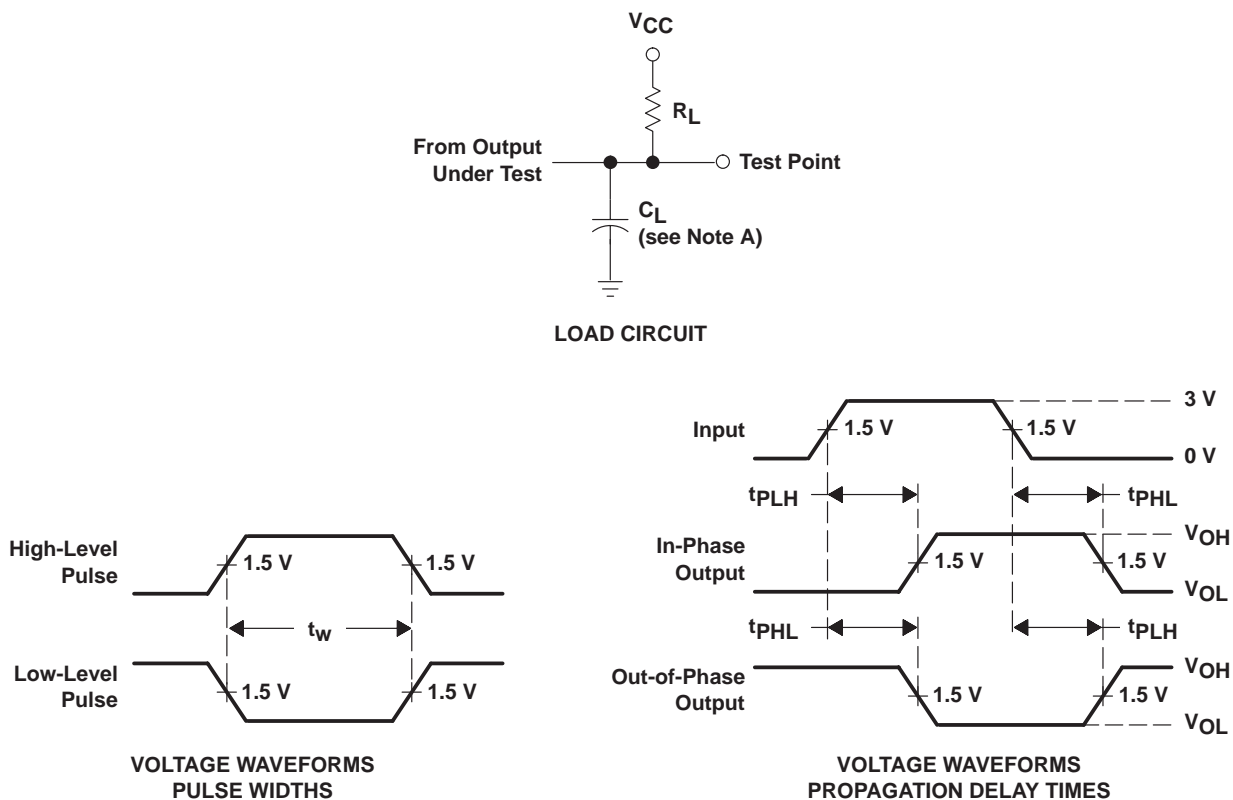
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}.$

**switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$  (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	A	Y	$R_L = 280 \Omega$	$C_L = 15 \text{ pF}$	2	5	7.5	ns
$t_{PHL}$					2	4.5	7	
$t_{PLH}$				$C_L = 50 \text{ pF}$		7.5		ns
$t_{PHL}$						7		

**PARAMETER MEASUREMENT INFORMATION  
SERIES 54/74 AND 54S/74S DEVICES**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , and:  
For Series 54/74,  $t_r \leq 7 \text{ ns}$ ,  $t_f \leq 7 \text{ ns}$ .  
For Series 54S/74S,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one input transition per measurement.

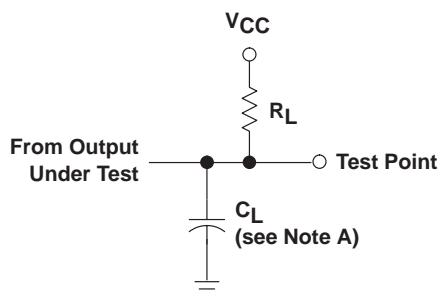
**Figure 1. Load Circuit and Voltage Waveforms**

**SN54LS05, SN54S05**  
**SN7405, SN74LS05, SN74S05**  
**HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS**

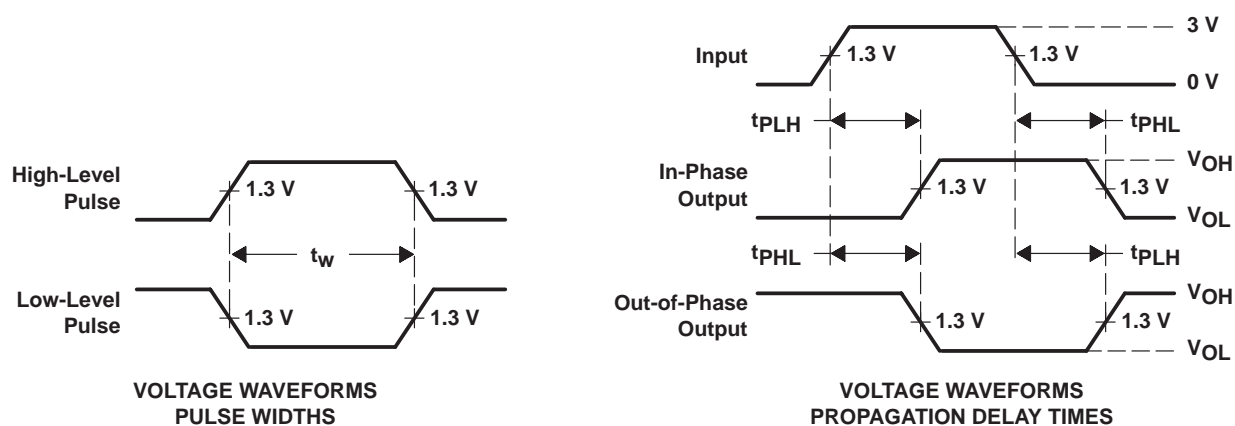
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**PARAMETER MEASUREMENT INFORMATION**  
**SERIES 54LS/74LS DEVICES**



**LOAD CIRCUIT**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 1.5$  ns,  $t_f \leq 2.6$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
JM38510/07003BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
JM38510/07004BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
M38510/07003BDA	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
M38510/07004BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54LS05J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN54S05J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SN7405D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	
SN7405DR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	
SN7405N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN7405N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN7405NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS05D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05DBLE	OBSOLETE	SSOP	DB	14		TBD	Call TI	Call TI	
SN74LS05DBR	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05DBRE4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05DBRG4	ACTIVE	SSOP	DB	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS05N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
SN74LS05NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS05NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS05NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S05D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S05DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S05DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S05N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S05N3	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	
SN74S05NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74S05NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S05NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74S05NSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SNJ54LS05FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54LS05J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54LS05W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S05FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
SNJ54S05J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
SNJ54S05W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN54LS05, SN54S05, SN7405, SN74LS05, SN74S05 :**

- Catalog: [SN74LS05](#), [SN74S05](#)
- Military: [SN5405](#), [SN54LS05](#), [SN54S05](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS05DBR	SSOP	DB	14	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74LS05DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS05NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74S05NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS05DBR	SSOP	DB	14	2000	367.0	367.0	38.0
SN74LS05DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS05NSR	SO	NS	14	2000	367.0	367.0	38.0
SN74S05NSR	SO	NS	14	2000	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004



N (R-PDIP-T\*\*)

16 PINS SHOWN

# PLASTIC DUAL-IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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