

SDLS028

# SN5403, SN54LS03, SN54S03, SN7403, SN74LS03, SN74S03

## QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

DECEMBER 1983—REVISED MARCH 1988

- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

### description

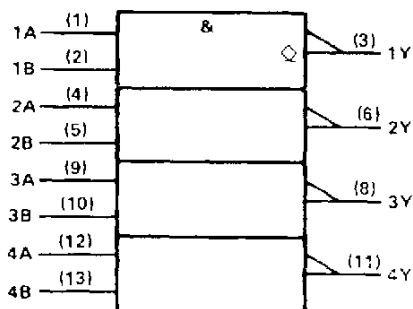
These devices contain four independent 2-input-NAND gates. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher  $V_{OH}$  levels.

The SN5403, SN54LS03 and SN54S03 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7403, SN74LS03 and SN74S03 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

### logic symbol†

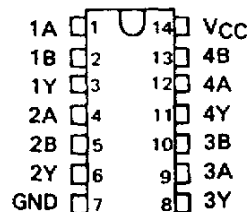


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.

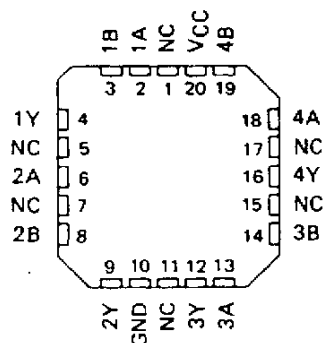
SN5403 . . . J OR W PACKAGE  
SN54LS03, SN54S03 . . . J OR W PACKAGE  
SN7403 . . . N PACKAGE  
SN74LS03, SN74S03 . . . D OR N PACKAGE

(TOP VIEW)



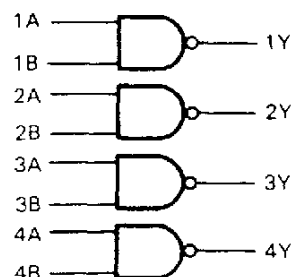
SN54LS03, SN54S03 . . . FK PACKAGE

(TOP VIEW)



NC - No internal connection

### logic diagram (positive logic)



$$Y = \overline{A \cdot B} \text{ or } Y = \overline{A} + \overline{B}$$

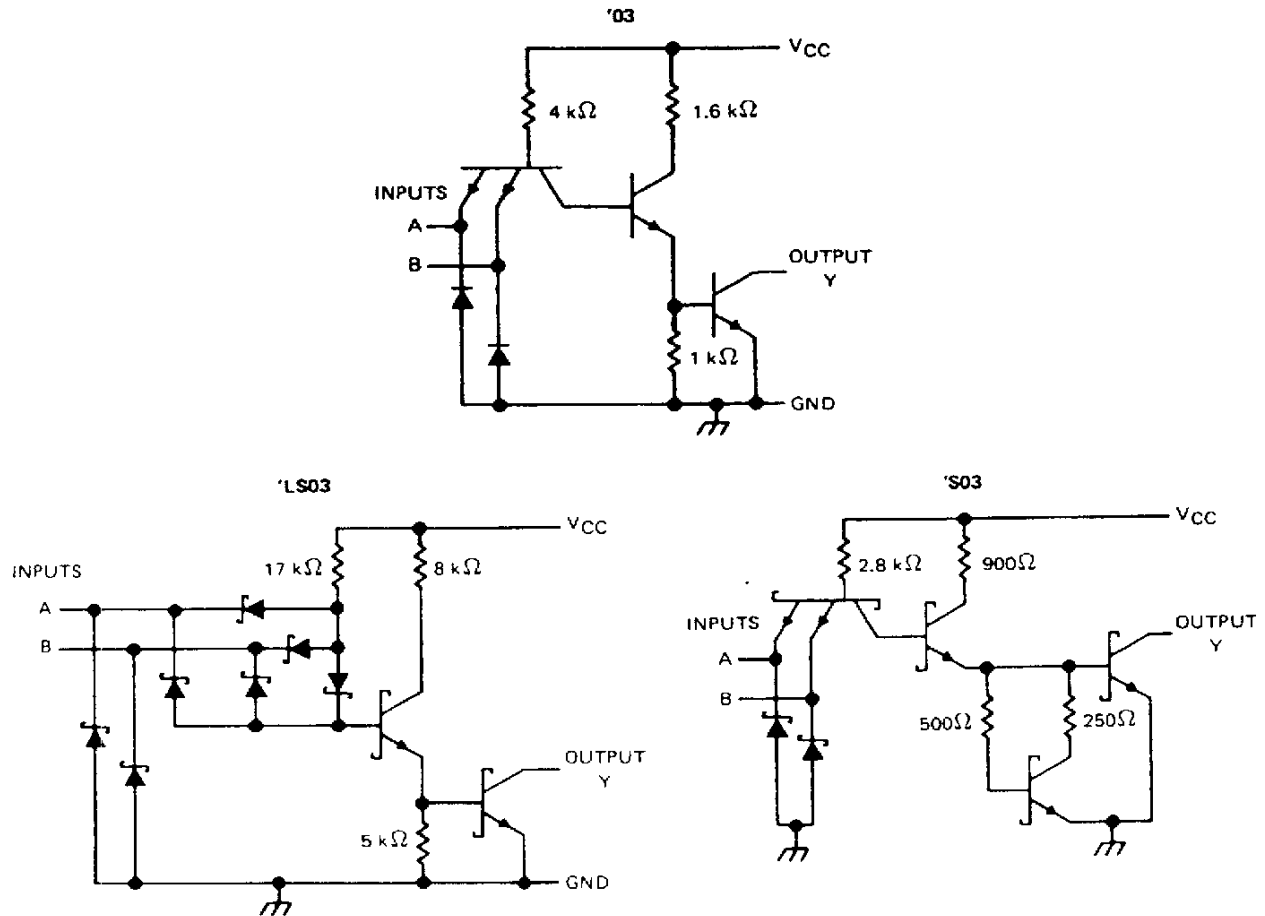
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**SN5403, SN54LS03, SN54S03,  
SN7403, SN74LS03, SN74S03  
QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

schematics (each gate)



Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage: '03, 'S03	5.5 V
'LS03	7 V
Off-state output voltage	7 V
Operating free-air temperature range: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

# **SN5403, SN7403** **QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

## recommended operating conditions

	SN5403			SN7403			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$V_{OH}$ High-level output voltage			5.5			5.5	V
$I_{OL}$ Low-level output current			16			16	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5403			SN7403			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
$I_{OH}$	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$						0.25	mA
	$V_{CC} = \text{MIN}, V_{IL} = 0.7 \text{ V}, V_{OH} = 5.5 \text{ V}$			0.25				
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	µA
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
$I_{CCH}$	$V_{CC} = \text{MAX}, V_I = 0$		4	8		4	8	mA
$I_{CCL}$	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$		12	22		12	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Y	$R_L = 4 \text{ k}\Omega,$	$C_L = 15 \text{ pF}$		35	45	ns
$t_{PHL}$			$R_L = 400 \Omega,$	$C_L = 15 \text{ pF}$		8	15	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

# **SN54LS03, SN74LS03** **QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

## **recommended operating conditions**

	SN54LS03			SN74LS03			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.7			0.8	V
$V_{OH}$ High-level output voltage			5.5			5.5	V
$I_{OL}$ Low-level output current			4			8	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

## **electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	SN54LS03			SN74LS03			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN.}$ , $I_I = -18 \text{ mA}$		-1.5			-1.5		V
$I_{OH}$	$V_{CC} = \text{MIN.}$ , $V_{IL} = \text{MAX.}$ , $V_{OH} = 5.5 \text{ V}$		0.1			0.1		mA
$V_{OL}$	$V_{CC} = \text{MIN.}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 4 \text{ mA}$	0.25	0.4		0.25	0.4		V
	$V_{CC} = \text{MIN.}$ , $V_{IH} = 2 \text{ V}$ , $I_{OL} = 8 \text{ mA}$				0.35	0.5		
$I_I$	$V_{CC} = \text{MAX.}$ , $V_I = 7 \text{ V}$		0.1			0.1		mA
$I_{IH}$	$V_{CC} = \text{MAX.}$ , $V_I = 2.7 \text{ V}$		20			20		µA
$I_{IL}$	$V_{CC} = \text{MAX.}$ , $V_I = 0.4 \text{ V}$		-0.4			-0.4		mA
$I_{CCH}$	$V_{CC} = \text{MAX.}$ , $V_I = 0$	0.8	1.6		0.8	1.6		mA
$I_{CCL}$	$V_{CC} = \text{MAX.}$ , $V_I = 4.5 \text{ V}$	2.4	4.4		2.4	4.4		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

## **switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ (see note 2)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Y	$R_L = 2 \text{ k}\Omega$ , $C_L = 15 \text{ pF}$		17	32	ns
$t_{PHL}$					15	28	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

# **SN54S03, SN74S03** **QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS**

recommended operating conditions

	SN54S03			SN74S03			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			2			V
$V_{IL}$ Low-level input voltage			0.8			0.8	V
$V_{OH}$ High-level output voltage			5.5			5.5	V
$I_{OL}$ Low-level output current			20			20	mA
$T_A$ Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54S03			SN74S03			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$V_{IK}$	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.2			-1.2		V
$I_{OH}$	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$						0.25	mA
	$V_{CC} = \text{MIN}, V_{IL} = 0.7 \text{ V}, V_{OH} = 5.5 \text{ V}$			0.25				
$V_{OL}$	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 20 \text{ mA}$			0.5			0.5	V
$I_I$	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
$I_{IH}$	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			50			50	μA
$I_{IL}$	$V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$			-2			-2	mA
$I_{CCH}$	$V_{CC} = \text{MAX}, V_I = 0$	6	13.2		6	13.2		mA
$I_{CCL}$	$V_{CC} = \text{MAX}, V_I = 4.5 \text{ V}$	20	36		20	36		mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

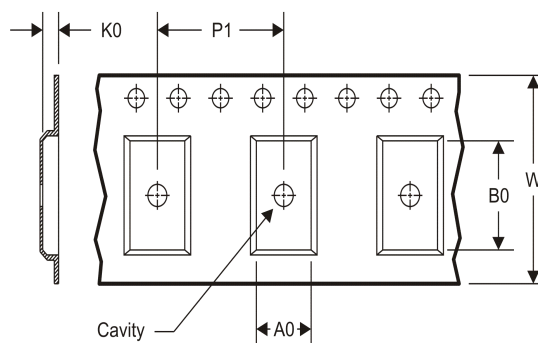
‡All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

switching characteristics,  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$  (see note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A or B	Y	$R_L = 280 \Omega, C_L = 15 \text{ pF}$	2	5	7.5	ns
$t_{PHL}$				2	4.5	7	ns
$t_{PLH}$			$R_L = 280 \Omega, C_L = 50 \text{ pF}$		7.5		ns
$t_{PHL}$					7		ns

NOTE 2. Load circuits and voltage waveforms are shown in Section 1.

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS03DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS03NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS03DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS03NSR	SO	NS	14	2000	367.0	367.0	38.0

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