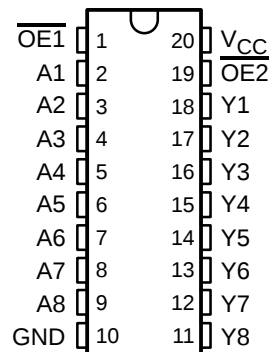


# SN54HCT540, SN74HCT540 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

SCLS008C – MARCH 1984 – REVISED MARCH 2003

- Operating Voltage Range of 4.5 V to 5.5 V
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Inputs Are TTL-Voltage Compatible
- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive Up To 15 LSTTL Loads
- Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)

SN54HCT540 . . . J PACKAGE  
SN74HCT540 . . . DW OR N PACKAGE  
(TOP VIEW)



## description/ordering information

These octal buffers and line drivers are designed to have the performance of the 'HCT240 devices and a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly facilitates printed circuit board layout.

The 3-state control gate is a 2-input NOR. If either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all eight outputs are in the high-impedance state. The 'HCT540 devices provide inverted data at the outputs.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$          | PACKAGE†  |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------------|------------------|
| –40°C to 85°C  | PDIP – N  | Tube          | SN74HCT540N           | SN74HCT540N      |
|                | SOIC – DW | Tube          | SN74HCT540DW          | HCT540           |
|                |           | Tape and reel | SN74HCT540DWR         |                  |
| –55°C to 125°C | CDIP – J  | Tube          | SNJ54HCT540J          | SNJ54HCT540J     |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each buffer/driver)

| INPUTS           |                  |   | OUTPUT<br>Y |
|------------------|------------------|---|-------------|
| $\overline{OE1}$ | $\overline{OE2}$ | A |             |
| L                | L                | L | H           |
| L                | L                | H | L           |
| H                | X                | X | Z           |
| X                | H                | X | Z           |



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## SCLS008C – MARCH 1984 – REVISED MARCH 2003

Logic diagram for the 74VHC125 3-state buffer. The diagram shows the following components and connections:

- Inputs:**
  - OE1 (Pin 1):** Active-low enable input.
  - OE2 (Pin 19):** Active-low enable input.
  - A1 (Pin 2):** Data input to the buffer.
- Logic:**
  - An **AND gate** has its two inputs connected to OE1 and OE2.
  - The output of the AND gate is connected to the output of a **buffer** (represented by a triangle with a circle at the output).
  - The output of the buffer is labeled **18 Y1**.
  - The output of the AND gate is also connected to a bus symbol (a vertical line with a downward arrow and a bracket) labeled **To Seven Other Channels**.

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# SN54HCT540, SN74HCT540

## OCTAL BUFFERS AND LINE DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                     | TEST CONDITIONS                                                                            | V <sub>CC</sub> | T <sub>A</sub> = 25°C    |      |     | SN54HCT540 |       | SN74HCT540 |      | UNIT |
|-------------------------------|--------------------------------------------------------------------------------------------|-----------------|--------------------------|------|-----|------------|-------|------------|------|------|
|                               |                                                                                            |                 | MIN                      | TYP  | MAX | MIN        | MAX   | MIN        | MAX  |      |
| V <sub>OH</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                        | 4.5 V           | I <sub>OH</sub> = –20 µA |      |     | 4.4        | 4.499 | 4.4        | 4.4  | V    |
|                               |                                                                                            |                 | I <sub>OH</sub> = –6 mA  |      |     | 3.98       | 4.3   | 3.7        | 3.84 |      |
| V <sub>OL</sub>               | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>                                        | 4.5 V           | I <sub>OL</sub> = 20 µA  |      |     | 0.001      | 0.1   | 0.1        | 0.1  | V    |
|                               |                                                                                            |                 | I <sub>OL</sub> = 6 mA   |      |     | 0.17       | 0.26  | 0.4        | 0.33 |      |
| I <sub>I</sub>                | V <sub>I</sub> = V <sub>CC</sub> or 0                                                      | 5.5 V           | ±0.1                     | ±100 |     | ±1000      |       | ±1000      |      | nA   |
| I <sub>OZ</sub>               | V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> | 5.5 V           | ±0.01                    | ±0.5 |     | ±10        |       | ±5         |      | µA   |
| I <sub>CC</sub>               | V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0                                  | 5.5 V           |                          | 8    |     | 160        |       | 80         |      | µA   |
| ΔI <sub>CC</sub> <sup>†</sup> | One input at 0.5 V or 2.4 V, Other inputs at 0 or V <sub>CC</sub>                          | 5.5 V           |                          | 1.4  | 2.4 | 3          |       | 2.9        |      | mA   |
| C <sub>i</sub>                |                                                                                            | 4.5 V to 5.5 V  |                          | 3    | 10  | 10         |       | 10         |      | pF   |

<sup>†</sup> This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT)           | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54HCT540 |     | SN74HCT540 |     | UNIT |
|------------------|------------------------|-------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
|                  |                        |             |                 | MIN                   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>pd</sub>  | A                      | Y           | 4.5 V           |                       | 13  | 20  |            | 30  |            | 25  | ns   |
|                  |                        |             | 5.5 V           |                       | 12  | 18  |            | 27  |            | 23  |      |
| t <sub>en</sub>  | $\overline{\text{OE}}$ | Y           | 4.5 V           |                       | 20  | 30  |            | 45  |            | 38  | ns   |
|                  |                        |             | 5.5 V           |                       | 18  | 27  |            | 41  |            | 34  |      |
| t <sub>dis</sub> | $\overline{\text{OE}}$ | Y           | 4.5 V           |                       | 19  | 30  |            | 45  |            | 38  | ns   |
|                  |                        |             | 5.5 V           |                       | 18  | 27  |            | 41  |            | 34  |      |
| t <sub>t</sub>   |                        | Y           | 4.5 V           |                       | 8   | 12  |            | 18  |            | 15  | ns   |
|                  |                        |             | 5.5 V           |                       | 7   | 11  |            | 16  |            | 14  |      |

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 150 pF (unless otherwise noted) (see Figure 1)

| PARAMETER       | FROM (INPUT)           | TO (OUTPUT) | V <sub>CC</sub> | T <sub>A</sub> = 25°C |     |     | SN54HCT540 |     | SN74HCT540 |     | UNIT |
|-----------------|------------------------|-------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
|                 |                        |             |                 | MIN                   | TYP | MAX | MIN        | MAX | MIN        | MAX |      |
| t <sub>pd</sub> | A                      | Y           | 4.5 V           |                       | 20  | 30  |            | 45  |            | 38  | ns   |
|                 |                        |             | 5.5 V           |                       | 19  | 27  |            | 41  |            | 34  |      |
| t <sub>en</sub> | $\overline{\text{OE}}$ | Y           | 4.5 V           |                       | 26  | 40  |            | 60  |            | 50  | ns   |
|                 |                        |             | 5.5 V           |                       | 25  | 36  |            | 54  |            | 45  |      |
| t <sub>t</sub>  |                        | Y           | 4.5 V           |                       | 17  | 42  |            | 63  |            | 53  | ns   |
|                 |                        |             | 5.5 V           |                       | 14  | 38  |            | 57  |            | 48  |      |

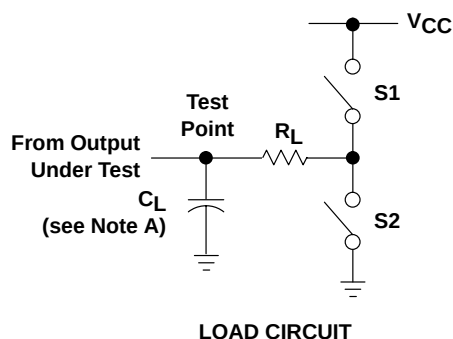
operating characteristics, T<sub>A</sub> = 25°C

| PARAMETER                                                       | TEST CONDITIONS | TYP | UNIT |
|-----------------------------------------------------------------|-----------------|-----|------|
| C <sub>pd</sub> Power dissipation capacitance per buffer/driver | No load         | 35  | pF   |

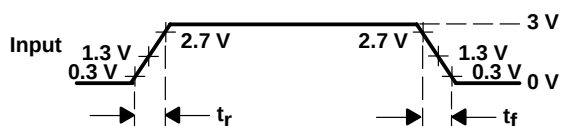
# SN54HCT540, SN74HCT540 OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

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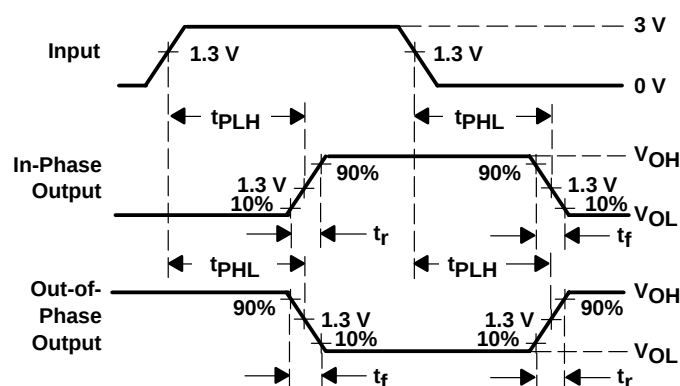
## PARAMETER MEASUREMENT INFORMATION



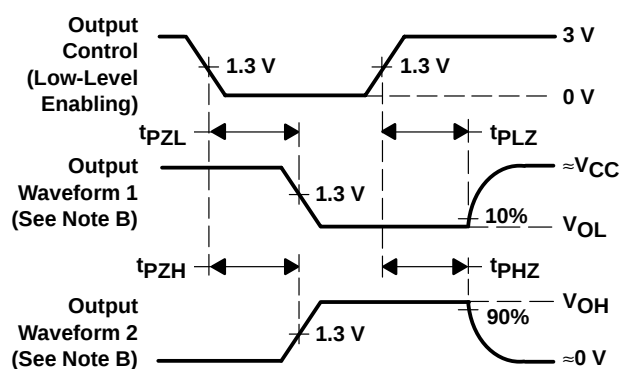
| PARAMETER         | $R_L$        | $C_L$           | S1     | S2     |
|-------------------|--------------|-----------------|--------|--------|
| $t_{en}$          | 1 k $\Omega$ | 50 pF or 150 pF | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{dis}$         | 1 k $\Omega$ | 50 pF           | Open   | Closed |
|                   |              |                 | Closed | Open   |
| $t_{pd}$ or $t_t$ | --           | 50 pF or 150 pF | Open   | Open   |



VOLTAGE WAVEFORM  
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - The outputs are measured one at a time with one input transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/ Ball Finish | MSL Peak Temp <sup>(3)</sup> | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|-------------------|------------------------------|--------------------------|
| JM38510/65760BRA | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                     | A42               | N / A for Pkg Type           |                          |
| M38510/65760BRA  | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                     | A42               | N / A for Pkg Type           |                          |
| SN54HCT540J      | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                     | A42               | N / A for Pkg Type           |                          |
| SN74HCT540DW     | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| SN74HCT540DWE4   | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| SN74HCT540DWG4   | ACTIVE                | SOIC         | DW              | 20   | 25          | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| SN74HCT540DWR    | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| SN74HCT540DWRE4  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| SN74HCT540DWRG4  | ACTIVE                | SOIC         | DW              | 20   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU         | Level-1-260C-UNLIM           |                          |
| SN74HCT540N      | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU         | N / A for Pkg Type           |                          |
| SN74HCT540N3     | OBSOLETE              | PDIP         | N               | 20   |             | TBD                     | Call TI           | Call TI                      |                          |
| SN74HCT540NE4    | ACTIVE                | PDIP         | N               | 20   | 20          | Pb-Free (RoHS)          | CU NIPDAU         | N / A for Pkg Type           |                          |
| SNJ54HCT540FK    | OBSOLETE              | LCCC         | FK              | 20   |             | TBD                     | Call TI           | Call TI                      |                          |
| SNJ54HCT540J     | ACTIVE                | CDIP         | J               | 20   | 1           | TBD                     | A42               | N / A for Pkg Type           |                          |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN54HCT540, SN74HCT540 :**

- Catalog: [SN74HCT540](#)
- Military: [SN54HCT540](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HCT540DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT540DWR | SOIC         | DW              | 20   | 2000 | 346.0       | 346.0      | 41.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



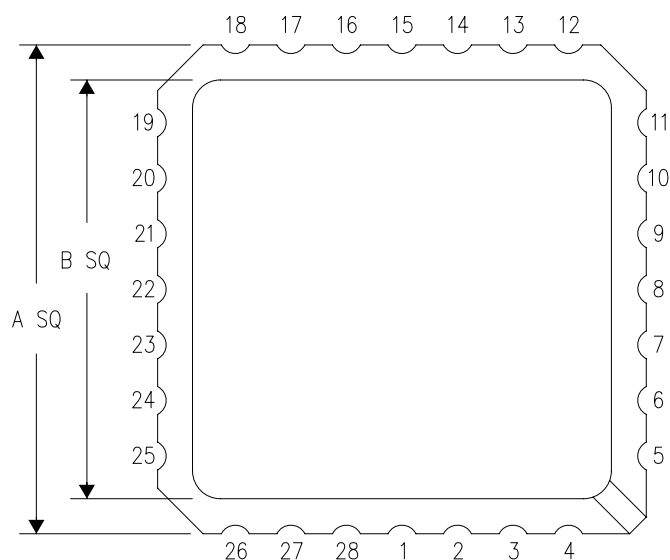
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



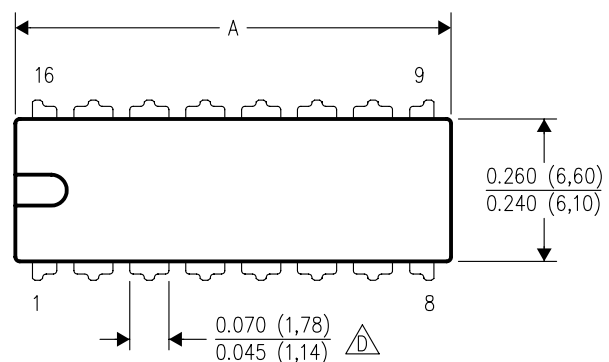
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

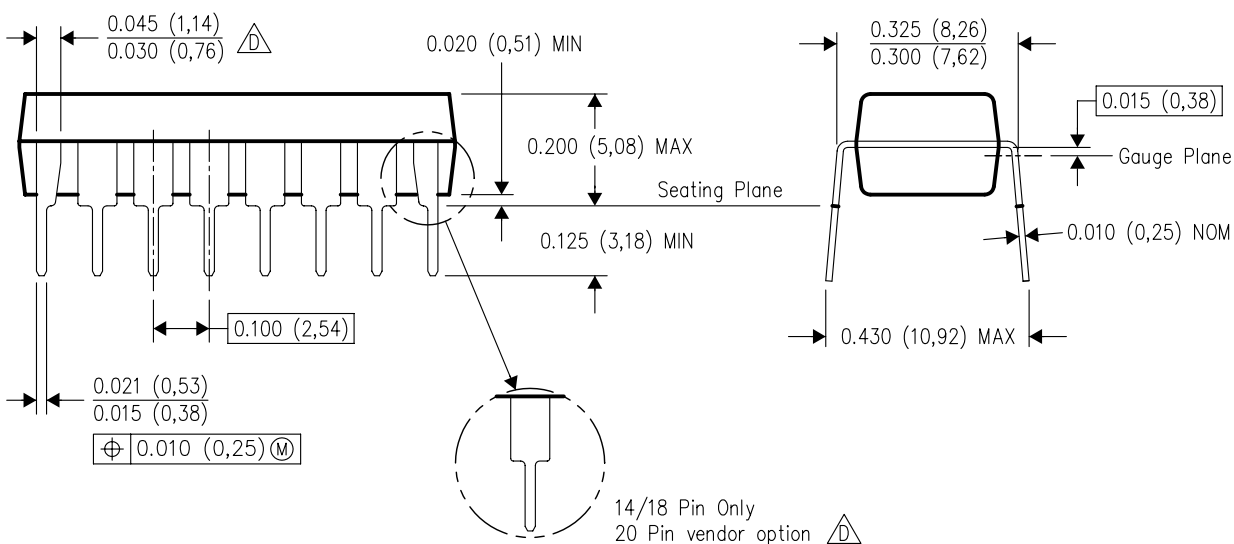
N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **<br>DIM      | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |

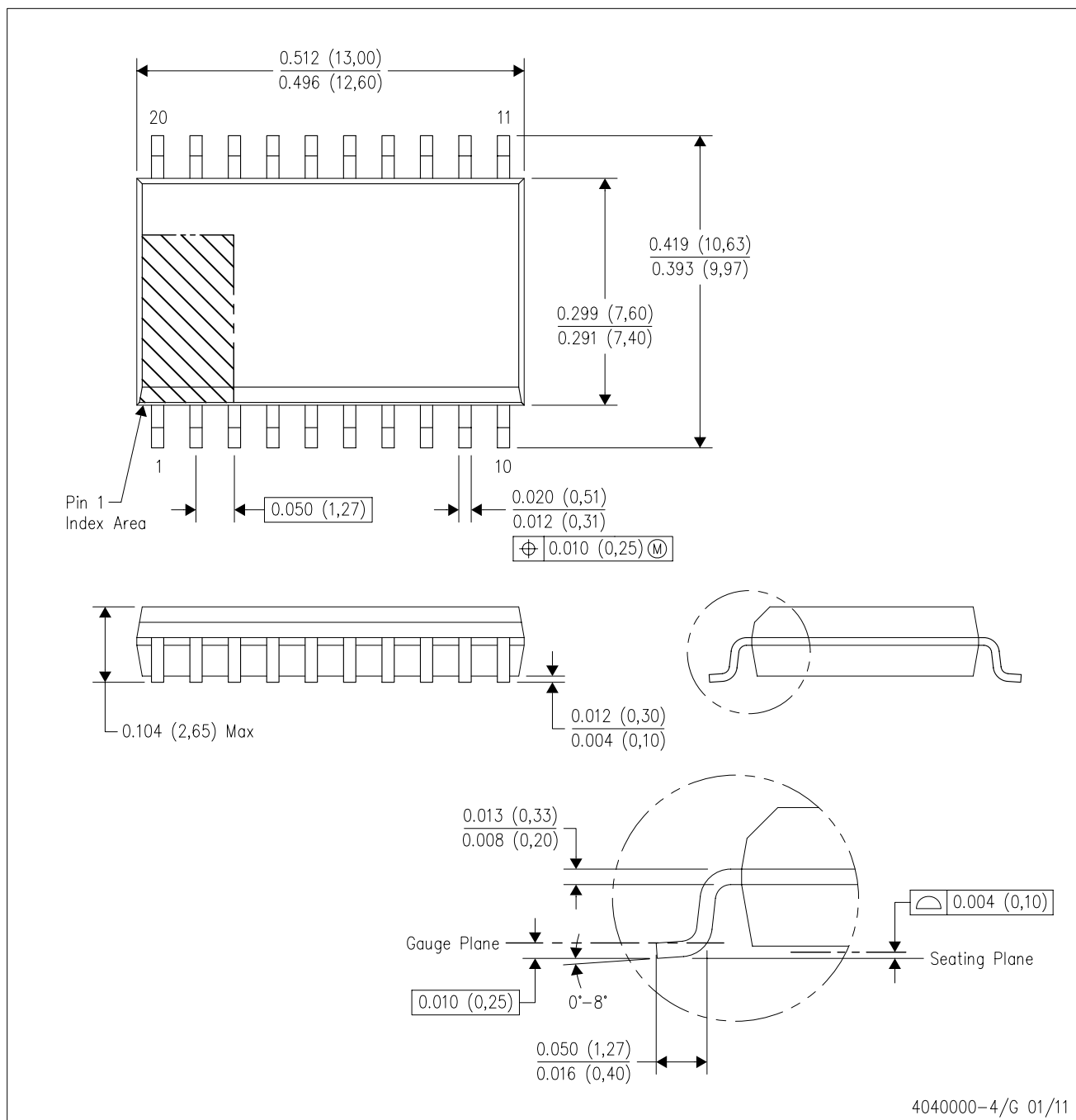


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

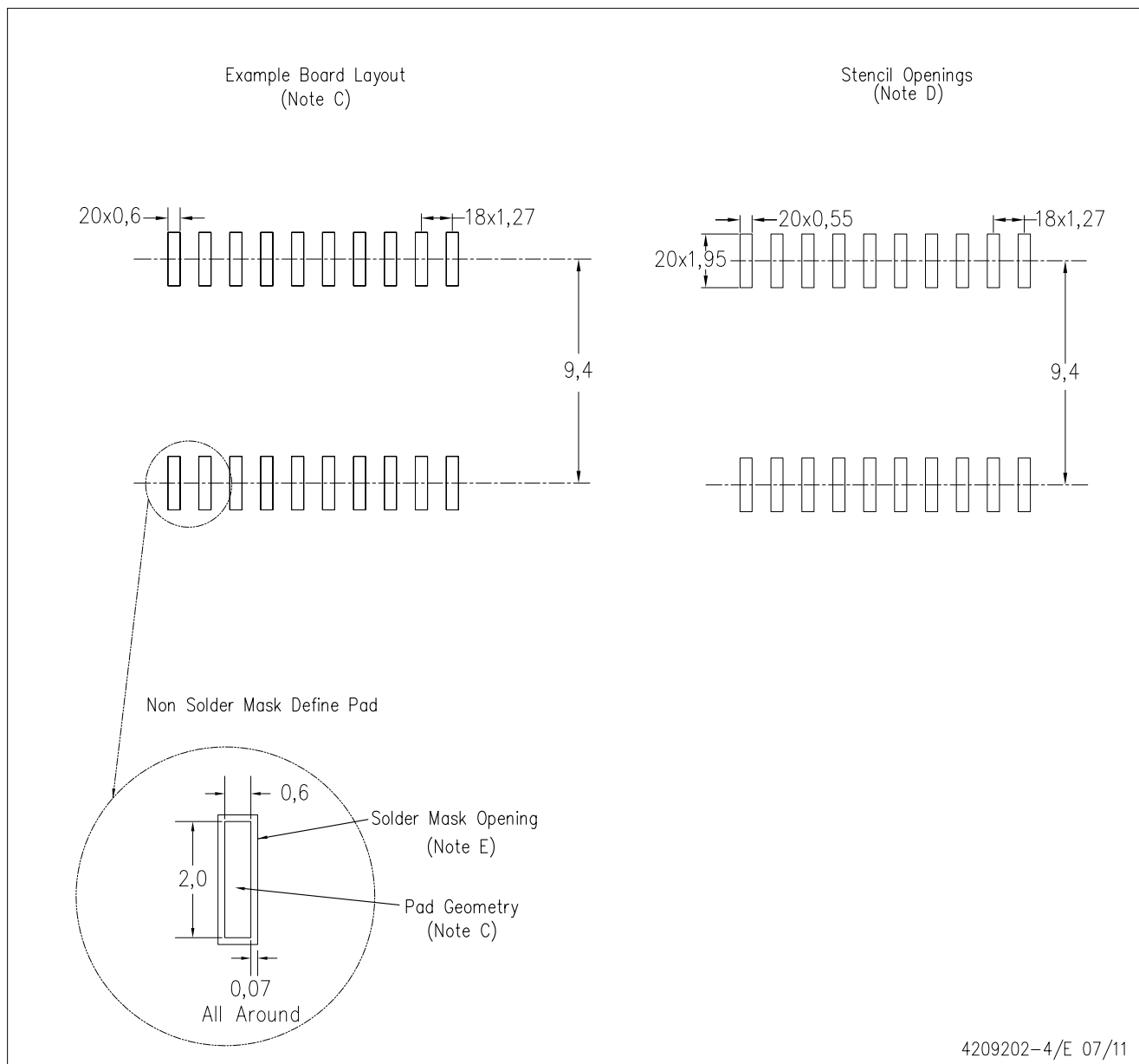
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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