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## 4 Revision History

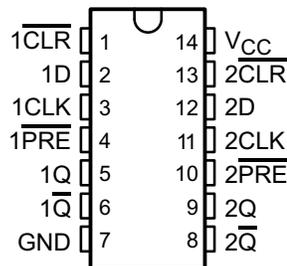
### Changes from Revision D (July 2003) to Revision E

**Page**

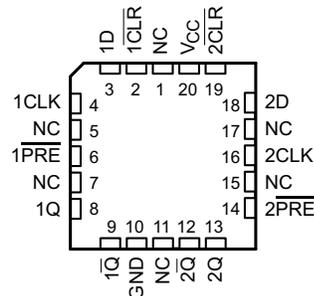
- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**

## 5 Pin Configuration and Functions

N, NS, D, DB, PW, J, or W Package  
14-Pin PDIP, SO, SOIC, SSOP, TSSOP, CDIP, or CFP  
Top View



FK Package  
20-Pin LCCC  
Top View



NC – No internal connection

### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	LCCC	SOIC, SSOP, CDIP, PDIP, SO, TSSOP, CFP NO.		
1CLK	4	3	I	Clock input
1CLR	2	1	I	Clear input - Pull low to set 1Q output low
1D	3	2	I	Input
1PRE	6	4	I	Preset input
1Q	8	5	O	Output
1Q	9	6	O	Inverted output
2CLK	16	11	I	Clock input
2CLR	19	13	I	Clear input - Pull low to set 1Q output low
2D	18	12	I	Input
2PRE	14	10	I	Preset input
2Q	13	9	O	Output
2Q	12	8	O	Inverted output
GND	10	7	—	Ground
NC	1	—	—	No connect (no internal connection)
	5			
	7			
	11			
	15			
V <sub>CC</sub>	20	14	—	Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$I_{IK}$	Input clamp current <sup>(2)</sup>	$V_I < 0$ or $V_I > V_{CC}$		±20 mA
$I_{OK}$	Output clamp current <sup>(2)</sup>	$V_O < 0$ or $V_O > V_{CC}$		±20 mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		±25 mA
Continuous current through $V_{CC}$ or GND				±50 mA
$T_j$	Junction temperature range			150 °C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 6.3 Recommended Operating Conditions

 See <sup>(1)</sup>

		SN54HC74			SN74HC74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5		V	
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V			0.5		V	
		$V_{CC} = 4.5$ V			1.35			
		$V_{CC} = 6$ V			1.8			
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise and fall time	$V_{CC} = 2$ V		1000		1000		ns
		$V_{CC} = 4.5$ V		500		500		
		$V_{CC} = 6$ V		400		400		
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74HC74					SN54HC74			UNIT
		D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	J (CDIP)	W (CFP)	FK (LCCC)	
		14 PINS					14 PINS		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	86	96	80	76	113	—	—	—	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	—	—	—	—	—	15.05	14.65	5.61	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range, T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP	MAX	UNIT	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		V	
			4.5 V	4.4	4.499			
			6 V	5.9	5.999			
		I <sub>OH</sub> = -4 mA	T <sub>A</sub> = 25°C	4.5 V	3.98	4.3		
			SN54HC74		3.7			
			SN74HC74		3.84			
	I <sub>OH</sub> = -5.2 mA	T <sub>A</sub> = 25°C	6 V	5.48	5.8			
		SN54HC74		5.2				
SN74HC74	5.34							
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1	V	
			4.5 V		0.001	0.1		
			6 V		0.001	0.1		
		I <sub>OL</sub> = 4 mA	T <sub>A</sub> = 25°C	4.5 V		0.17		0.26
			SN54HC74					0.4
			SN74HC74					0.33
	I <sub>OL</sub> = 5.2 mA	T <sub>A</sub> = 25°C	6 V		0.15	0.26		
		SN54HC74				0.4		
SN74HC74			0.33					
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	T <sub>A</sub> = 25°C	6 V		±0.1	±100	nA	
		SN54HC74, SN74HC74				±1000		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0,	I <sub>O</sub> = 0	T <sub>A</sub> = 25°C	6 V		4	μA	
			SN54HC74			80		
			SN74HC74			40		
C <sub>i</sub>			2 V to 6 V		3	10	pF	
C <sub>pd</sub>	No load		2 V to 6 V		35		pF	

## 6.6 Timing Requirements

 over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

		$V_{CC}$	$T_A$	MIN	MAX	UNIT
$f_{\text{clock}}$	Clock frequency	2 V	$T_A = 25^\circ\text{C}$		6	MHz
			SN54HC74		4.2	
			SN74HC74		5	
		4.5 V	$T_A = 25^\circ\text{C}$		31	
			SN54HC74		21	
			SN74HC74		25	
		6 V	$T_A = 25^\circ\text{C}$	0	36	
			SN54HC74	0	25	
			SN74HC74	0	29	
$t_w$	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	2 V	$T_A = 25^\circ\text{C}$	100		ns
			SN54HC74	150		
			SN74HC74	125		
		4.5 V	$T_A = 25^\circ\text{C}$	20		
			SN54HC74	30		
			SN74HC74	25		
		6 V	$T_A = 25^\circ\text{C}$	14		
			SN54HC74	25		
			SN74HC74	21		
	CLK high or low	2 V	$T_A = 25^\circ\text{C}$	80		
			SN54HC74	120		
			SN74HC74	100		
		4.5 V	$T_A = 25^\circ\text{C}$	16		
			SN54HC74	24		
			SN74HC74	20		
		6 V	$T_A = 25^\circ\text{C}$	14		
			SN54HC74	20		
			SN74HC74	17		
$t_{\text{su}}$	Data	2 V	$T_A = 25^\circ\text{C}$	100		ns
			SN54HC74	150		
			SN74HC74	125		
		4.5 V	$T_A = 25^\circ\text{C}$	20		
			SN54HC74	30		
			SN74HC74	25		
		6 V	$T_A = 25^\circ\text{C}$	17		
			SN54HC74	25		
			SN74HC74	21		
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	2 V	$T_A = 25^\circ\text{C}$	25		
			SN54HC74	40		
			SN74HC74	30		
		4.5 V	$T_A = 25^\circ\text{C}$	5		
			SN54HC74	8		
			SN74HC74	6		
		6 V	$T_A = 25^\circ\text{C}$	4		
			SN54HC74	7		
			SN74HC74	5		

## Timing Requirements (continued)

over recommended operating free-air temperature range,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

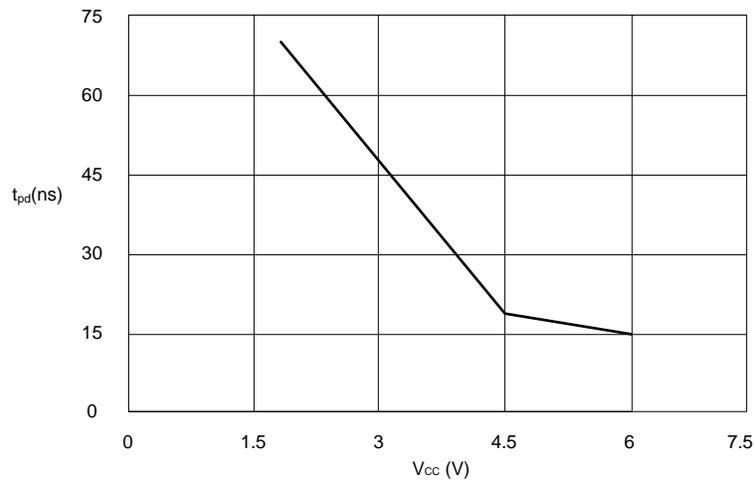
		$V_{CC}$	$T_A$	MIN	MAX	UNIT
$t_h$	Hold time, data after CLK↑	2 V		0		ns
		4.5 V		0		
		6 V		0		

## 6.7 Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see [Figure 2](#))

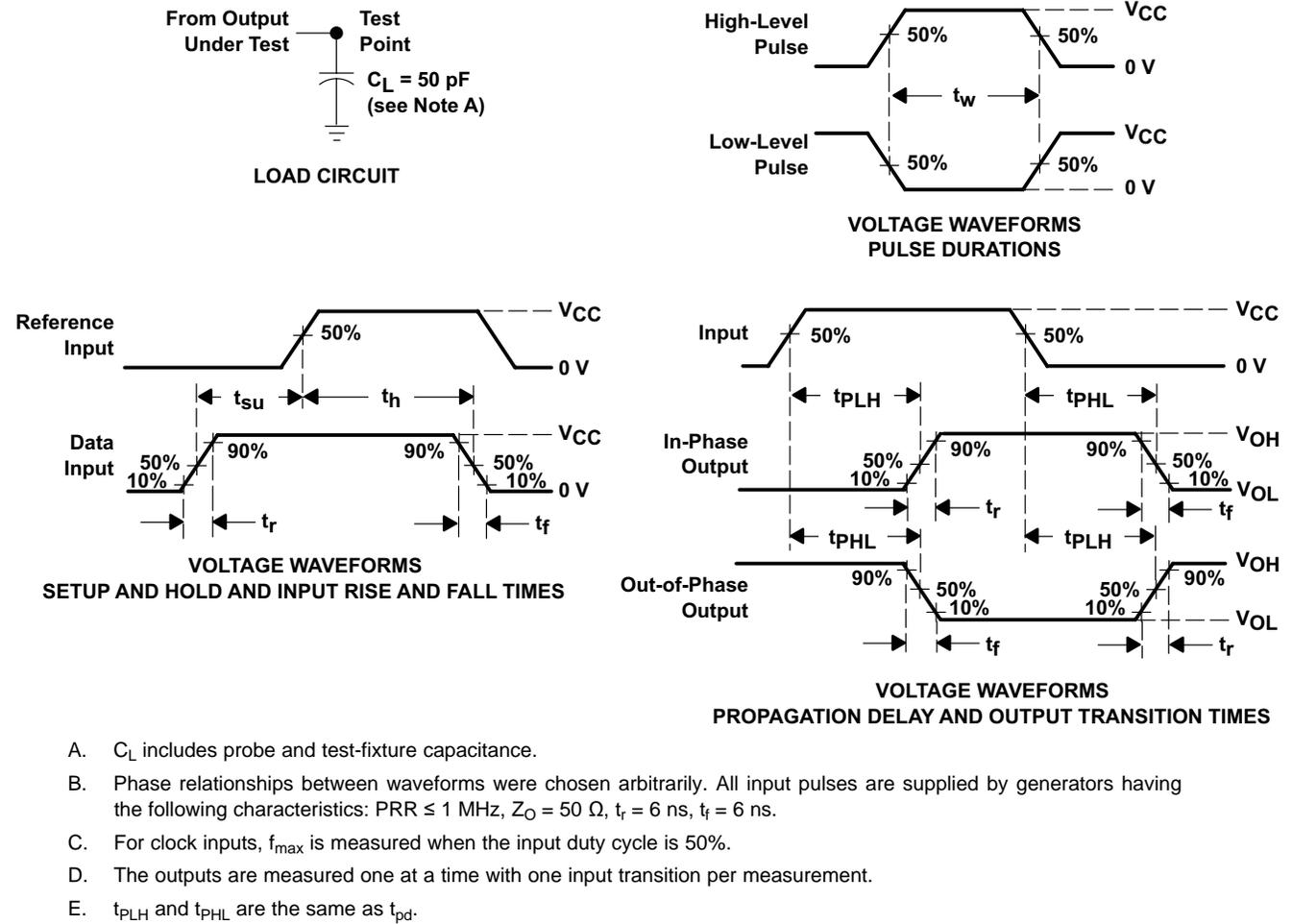
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A$	MIN	TYP	MAX	UNIT
$f_{max}$			2 V	$T_A = 25^\circ\text{C}$	6	10		MHz
				SN54HC74	4.2			
				SN74HC74	6			
			4.5 V	$T_A = 25^\circ\text{C}$	31	50		
				SN54HC74	21			
				SN74HC74	25			
			6 V	$T_A = 25^\circ\text{C}$	36	60		
				SN54HC74	25			
				SN74HC74	29			
$t_{pd}$	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2 V	$T_A = 25^\circ\text{C}$		70	230	ns
				SN54HC74		345		
				SN74HC74		290		
			4.5 V	$T_A = 25^\circ\text{C}$		20	46	
				SN54HC74		69		
				SN74HC74		58		
			6 V	$T_A = 25^\circ\text{C}$		15	39	
				SN54HC74		59		
				SN74HC74		49		
	CLK	Q or $\overline{Q}$	2 V	$T_A = 25^\circ\text{C}$		70	175	
				SN54HC74		250		
				SN74HC74		220		
			4.5 V	$T_A = 25^\circ\text{C}$		20	35	
				SN54HC74		50		
				SN74HC74		44		
			6 V	$T_A = 25^\circ\text{C}$		15	30	
				SN54HC74		42		
				SN74HC74		37		
$t_t$		Q or $\overline{Q}$	2 V	$T_A = 25^\circ\text{C}$		28	75	ns
				SN54HC74		110		
				SN74HC74		95		
			4.5 V	$T_A = 25^\circ\text{C}$		8	15	
				SN54HC74		22		
				SN74HC74		19		
			6 V	$T_A = 25^\circ\text{C}$		6	13	
				SN54HC74		19		
				SN74HC74		16		

## 6.8 Typical Characteristics



**Figure 1. Typical Propagation Delay - CLK to Q**

## 7 Parameter Measurement Information



- A.  $C_L$  includes probe and test-fixture capacitance.
- B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
- C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
- D. The outputs are measured one at a time with one input transition per measurement.
- E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

A low level at the preset ( $\overline{\text{PRE}}$ ) or clear ( $\overline{\text{CLR}}$ ) input sets or resets the outputs, regardless of the levels of the other inputs. When  $\overline{\text{PRE}}$  and  $\overline{\text{CLR}}$  are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

The resistor and capacitor at the  $\overline{\text{CLR}}$  pin are optional. If they are not used, the  $\overline{\text{CLR}}$  pin should be connected directly to  $V_{\text{CC}}$  to be inactive.

### 9.2 Typical Application

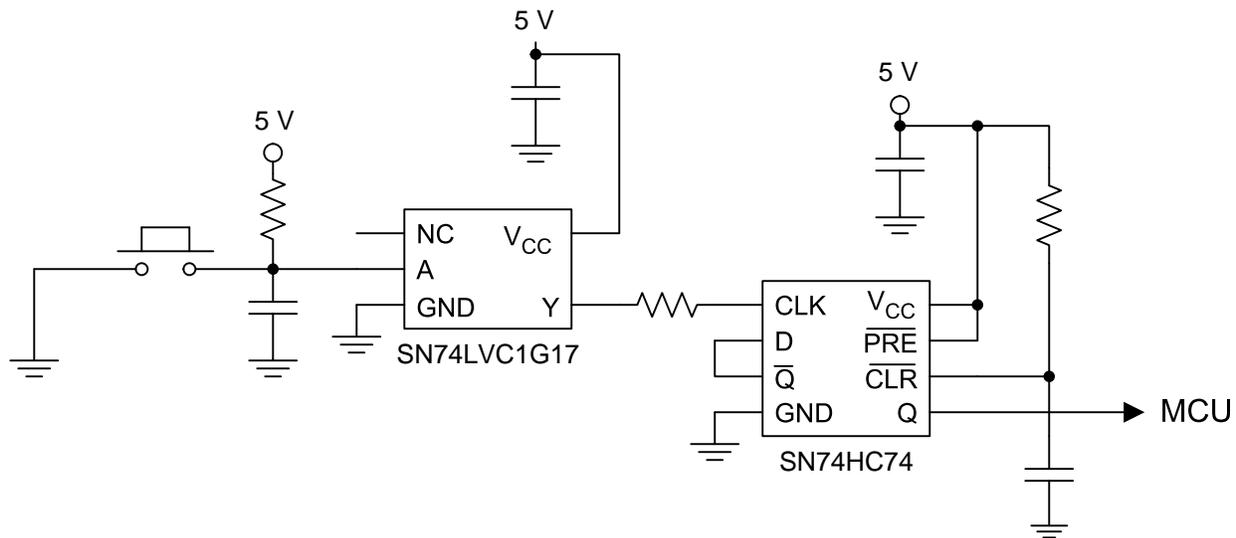


Figure 4. Device Power Button Circuit

#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs may be combined to produce higher drive, but the high drive will also create faster edges into light loads. Because of this, routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

##### 1. Recommended Input Conditions:

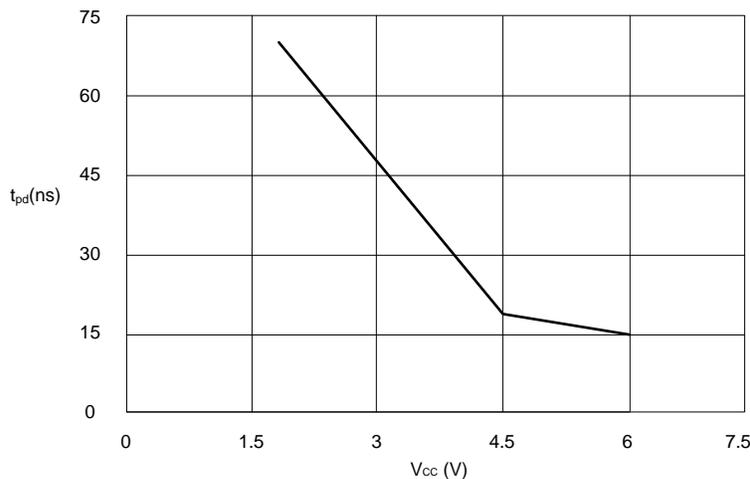
- For rise time and fall time specifications, see ( $\Delta t/\Delta V$ ) in [Recommended Operating Conditions](#) table.
- For specified high and low levels, see ( $V_{\text{IH}}$  and  $V_{\text{IL}}$ ) in [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{\text{CC}}$ .

##### 2. Recommended Output Conditions:

- Load currents should not exceed 25 mA per output and 50 mA total for the part.
- Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

## Typical Application (continued)

### 9.2.3 Application Curve



**Figure 5. Typical Propagation Delay -  $\overline{\text{CLR}}$  to Q**

## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#) table. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu\text{F}$  capacitor is recommended and if there are multiple  $V_{CC}$  terminals then .01- $\mu\text{F}$  or .022- $\mu\text{F}$  capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- $\mu\text{F}$  and 1- $\mu\text{F}$  capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

### 11.2 Layout Example

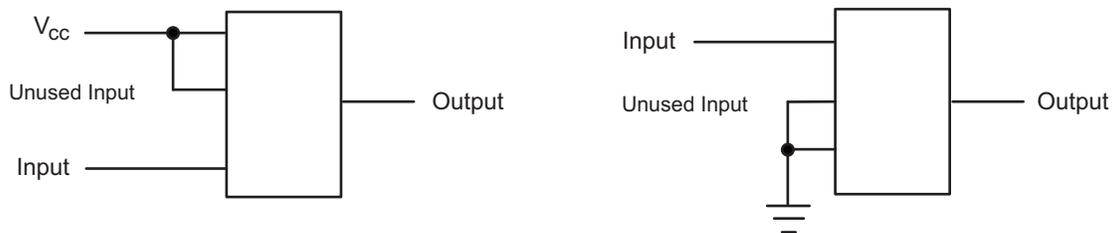


Figure 6. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC74	<a href="#">Click here</a>				
SN74HC74	<a href="#">Click here</a>				

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

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### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
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