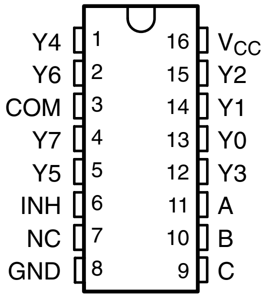
SN74HC4851-Q1
8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER WITH INJECTION-CURRENT EFFECT CONTROL

SCLS554B – JANUARY 2004 – REVISED APRIL 2008

- **Qualified for Automotive Applications**
- **Injection-Current Cross Coupling <1mV/mA (see Figure 1)**
- **Low Crosstalk Between Switches**
- **Pin Compatible With CD74HC4051, SN74LV4051A, and CD4051B**
- **2-V to 6-V V_{CC} Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**

D OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

This eight-channel CMOS analog multiplexer/demultiplexer is pin compatible with the ’4051 function and, additionally, features injection-current effect control, which has excellent value in automotive applications where voltages in excess of normal supply voltages are common.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Tape and reel	SN74HC4851QDRQ1	HC4851Q
	TSSOP – PW	Tape and reel	SN74HC4851QPWRQ1	HC4851Q

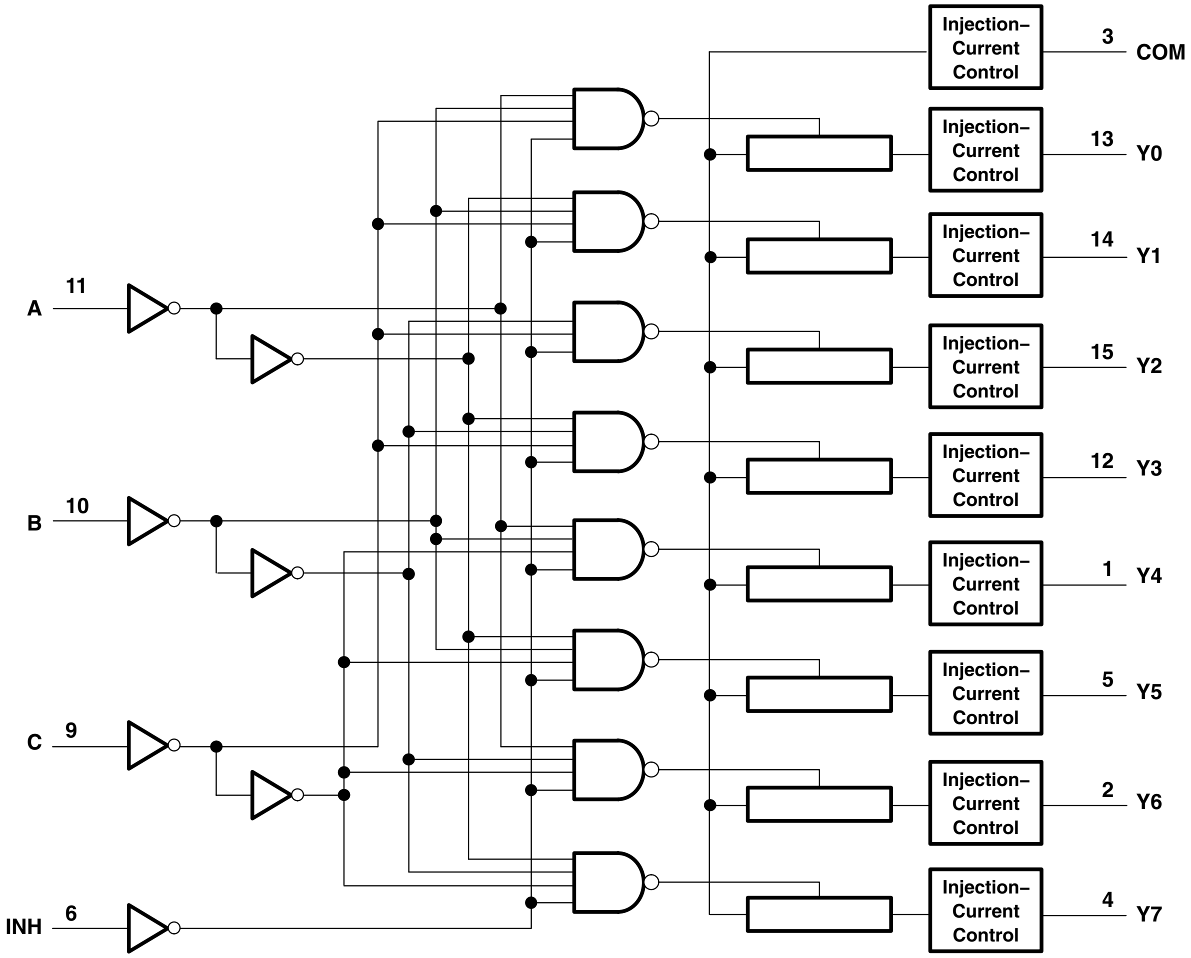
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}		–0.5 V to 7 V
Input voltage range, V_I (see Note 1)		–0.5 V to V_{CC} + 0.5 V
Switch I/O voltage range, V_{IO} (see Notes 1 and 2)		–0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)		±20 mA
I/O diode current, I_{IOK} ($V_{IO} < 0$ or $V_{IO} > V_{CC}$)		±20 mA
Switch through current, I_T (V_{IO} = 0 to V_{CC})		±25 mA
Continuous current through V_{CC} or GND		±50 mA
Package thermal impedance, θ_{JA} (see Note 3):	D package	73°C/W
	PW package	108°C/W
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage, control inputs	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 3.3 V	2.3		
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage, control inputs	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 3.3 V		1	
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Control input voltage		0	V_{CC}	V
V_{IO}	Input/output voltage		0	V_{CC}	V
Δt/Δv	Input transition rise or fall time	V_{CC} = 2 V		1000	ns
		V_{CC} = 3 V		800	
		V_{CC} = 3.3 V		700	
		V_{CC} = 4.5 V		500	
		V_{CC} = 6 V		400	
T_A	Operating free-air temperature		–40	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
r_{on}	On-state switch resistance	$I_T \leq 2$ mA, $V_I = V_{CC}$ to GND, $V_{INH} = V_{IL}$ (see Figure 5)	2.V		500	650		670		700	Ω
			3 V		215	280		320		360	
			3.3 V		210	270		305		345	
			4.5 V		160	210		240		270	
			6 V		150	195		220		250	
Δr_{on}	Difference in on-state resistance between switches	$I_T \leq 2$ mA, $V_I = V_{CC}/2$, $V_{INH} = V_{IL}$	2.V		4	13		18		23	Ω
			3 V		2	10		12		16	
			3.3 V		2	9		12		16	
			4.5 V		2	9		12		16	
			6 V		3	10		14		19	
I_I	Control input current	$V_I = V_{CC}$ or GND	6 V			±0.1		±0.1		±1	µA
$I_{S(off)}$	Off-state switch leakage current (any one channel)	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IH}$ (see Figure 6)	6 V			±0.1		±0.5		±1	µA
	Off-state switch leakage current (common channel)	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IH}$ (see Figure 7)				±0.2		±2		±4	
$I_{S(on)}$	On-state switch leakage current	$V_I = V_{CC}$ or GND, $V_{INH} = V_{IL}$ (see Figure 8)	6 V			±0.1		±0.5		±1	µA
I_{CC}	Supply current	$V_I = V_{CC}$ or GND	6 V			2		20		40	µA
C_{IC}	Control input capacitance	A, B, C, INH			3.5	10		10		10	pF
C_{IS}	Common terminal capacitance	Switch off			22	40		40		40	pF
C_{OS}	Switch terminal capacitance	Switch off			6.7	15		15		15	pF

injection current coupling specifications, T_A = –40°C to 125°C

PARAMETER		V_{CC}	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V\Delta_{out}$	Maximum shift of output voltage of enabled analog channel	3.3 V	$R_S \leq 3.9$ kΩ	I_I‡ ≤ 1 mA		0.05	1	mV
		5 V				0.1	1	
		3.3 V		I_I‡ ≤ 10 mA		0.345	5	
		5 V				0.067	5	
		3.3 V	$R_S \leq 20$ kΩ	I_I‡ ≤ 1 mA		0.05	2	
		5 V				0.11	2	
		3.3 V		I_I‡ ≤ 10 mA		0.05	20	
		5 V				0.024	20	

† Typical values are measured at T_A = 25°C.

‡ I_I = total current injected into all disabled channels

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2 V, C_L = 50 pF (unless otherwise noted) (see Figures 9–14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		19.5	30		34		37	ns
t_{PLH} t_{PHL}	Propagation delay time	A, B, C	COM or Yn		23	35		40		45	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			95		105		115	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			95		105		115	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3 V, C_L = 50 pF (unless otherwise noted) (see Figures 9–14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		12	17.5		19.5		21.5	ns
t_{PLH} t_{PHL}	Propagation delay time	A, B, C	COM or Yn		13.5	19.5		22		25	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			90		100		110	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			90		100		110	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V, C_L = 50 pF (unless otherwise noted) (see Figures 9–14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		11	16.5		18.5		20.5	ns
t_{PLH} t_{PHL}	Propagation delay time	A, B, C	COM or Yn		12.5	18.5		21		24	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			85		95		105	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			85		95		105	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 4.5 V, C_L = 50 pF (unless otherwise noted) (see Figures 9–14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		8.6	14		15		16	ns
t_{PLH} t_{PHL}	Propagation delay time	A, B, C	COM or Yn		10	16		18		20	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			80		90		100	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			80		90		100	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, C_L = 50 pF (unless otherwise noted) (see Figures 9–14)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			UP TO 85°C		UP TO 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM		8	12.5		13.5		14.5	ns
t_{PLH} t_{PHL}	Propagation delay time	A, B, C	COM or Yn		9.5	15		17		19	ns
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn			78		80		80	ns
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn			78		80		80	ns

operating characteristics, T_A = 25°C (see Figure 15)

PARAMETER		V_{CC}	TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	3.3 V	No load	32	pF
		5 V		37	

APPLICATION INFORMATION

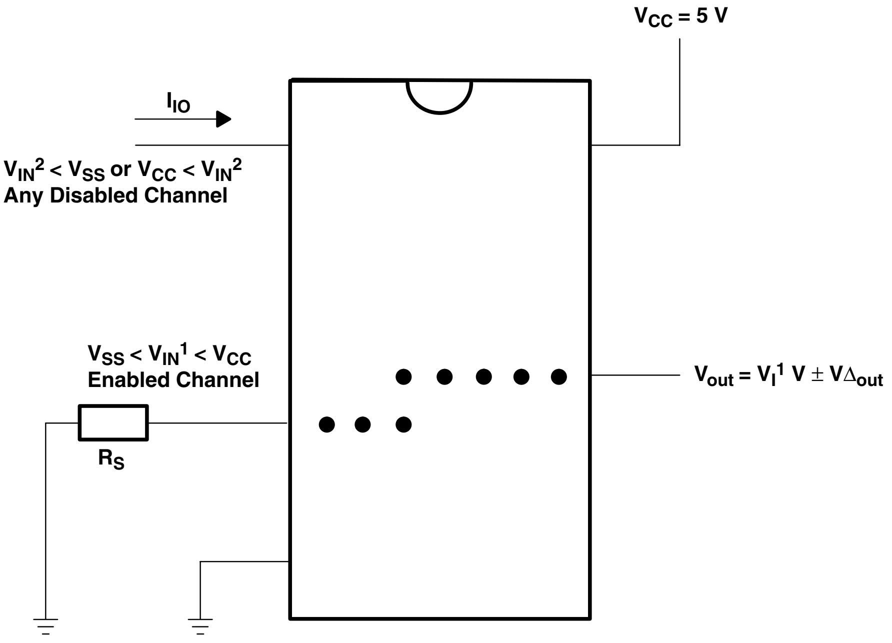


Figure 1. Injection-Current Coupling Specification

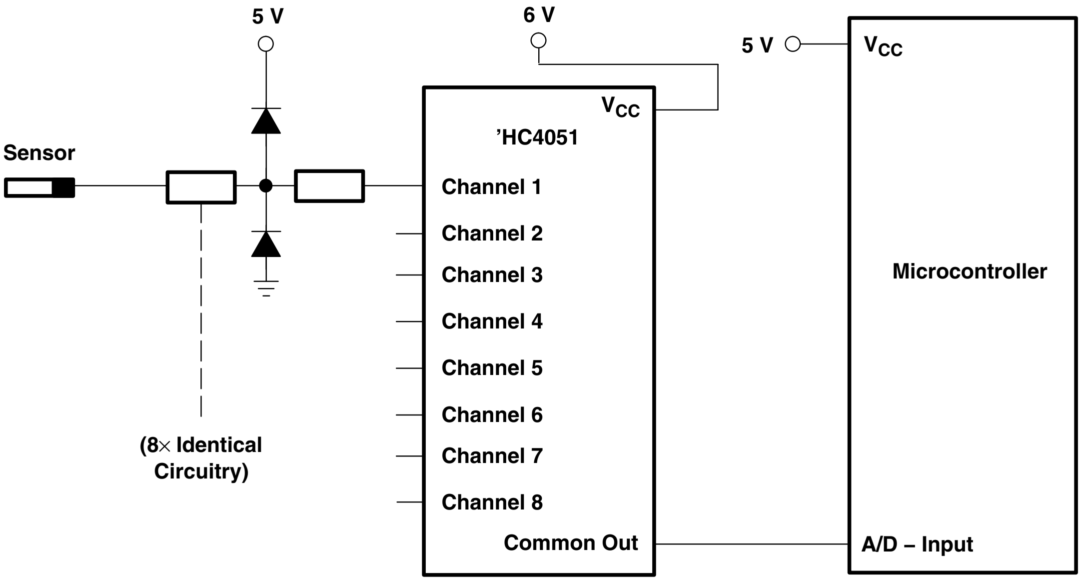


Figure 2. Alternate Solution Requires 32 Passive Components and One Extra 6-V Regulator to Suppress Injection Current Into a Standard 'HC4051 Multiplexer

APPLICATION INFORMATION

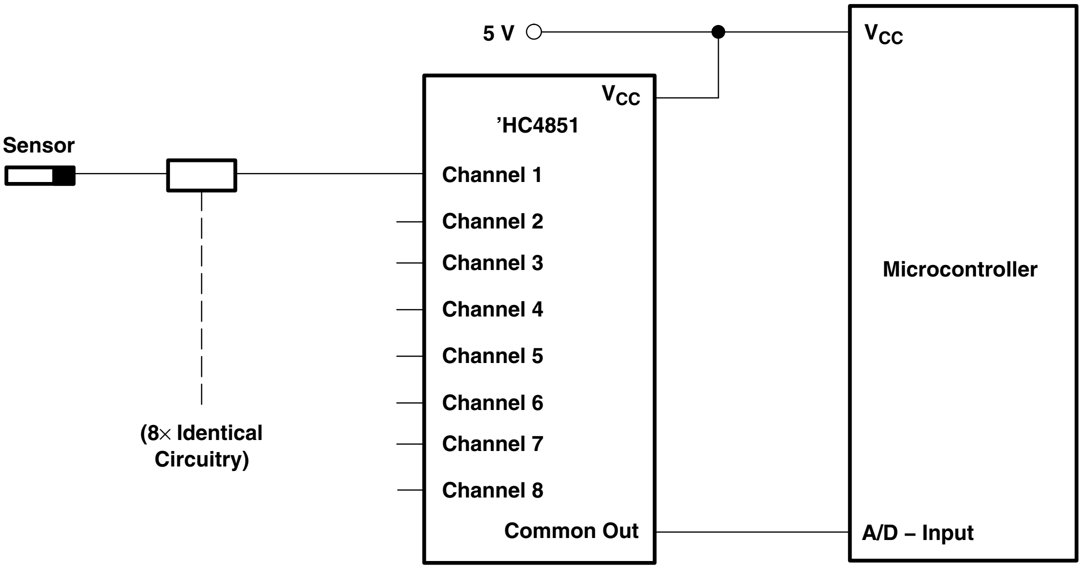


Figure 3. Solution by Applying the ’HC4851 Multiplexer

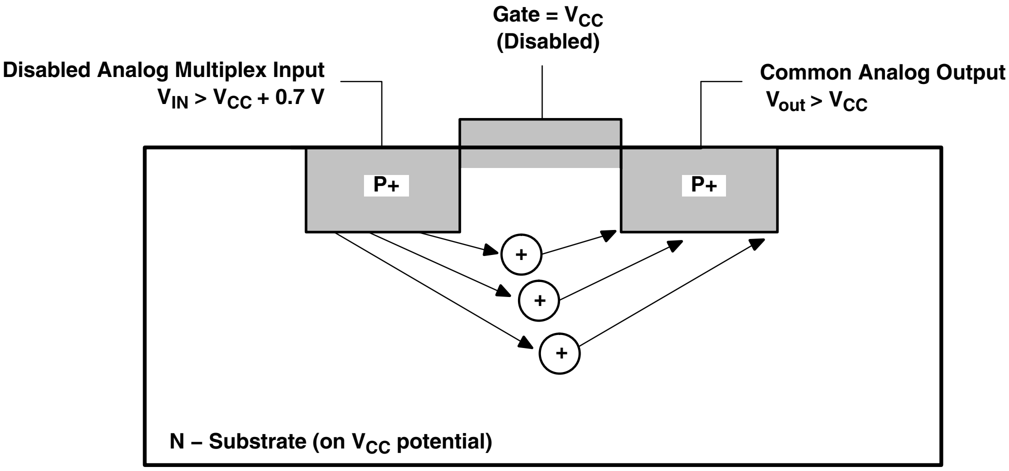
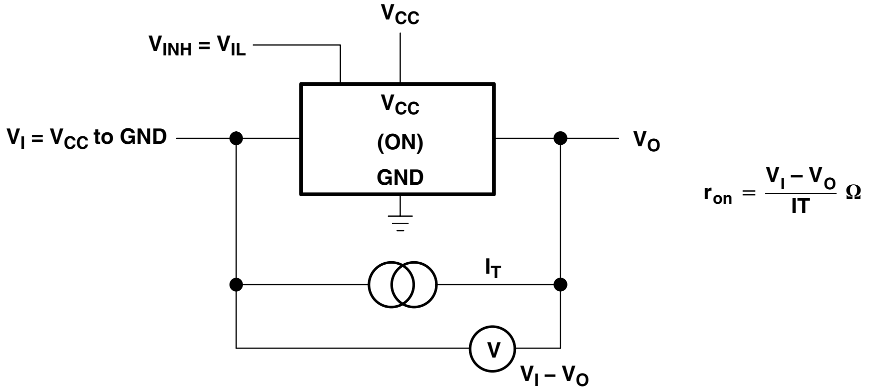


Figure 4. Diagram of Bipolar Coupling Mechanism
(Appears if V_{IN} Exceeds V_{CC}, Driving Injection Current Into the Substrate)

PARAMETER MEASUREMENT INFORMATION



$$r_{on} = \frac{V_I - V_O}{IT}\ \Omega$$

Figure 5. On-State-Resistance Test Circuit

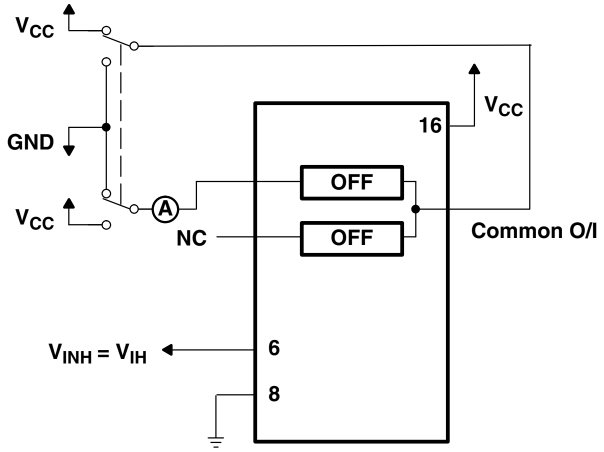


Figure 6. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup

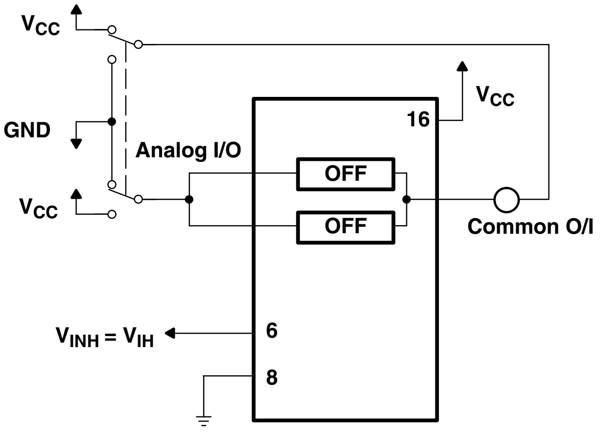


Figure 7. Maximum Off-Channel Leakage Current, Common Channel, Test Setup

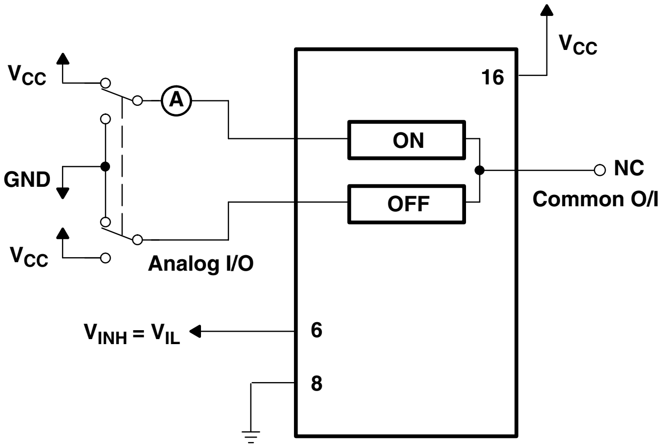


Figure 8. Maximum On-Channel Leakage Current, Channel to Channel, Test Setup

PARAMETER MEASUREMENT INFORMATION

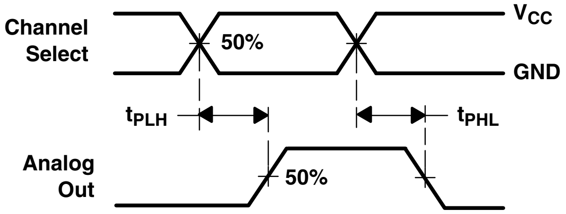
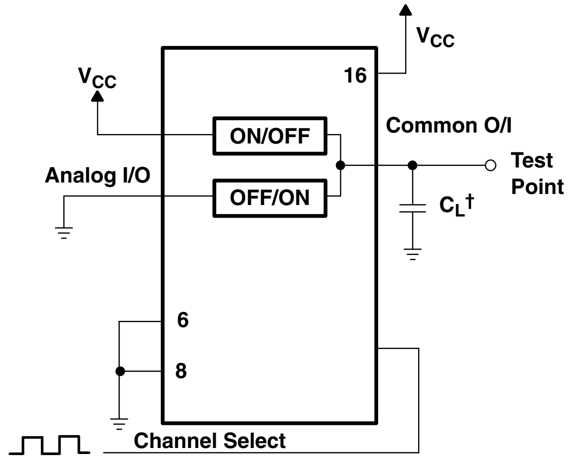


Figure 9. Propagation Delays, Channel Select to Analog Out



† Includes all probe and jig capacitance

Figure 10. Propagation-Delay Test Setup, Channel Select to Analog Out

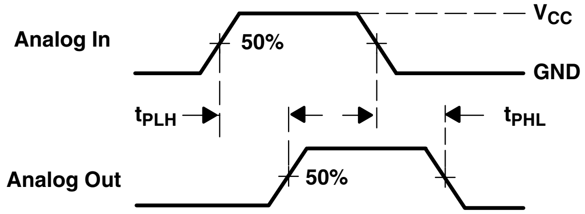
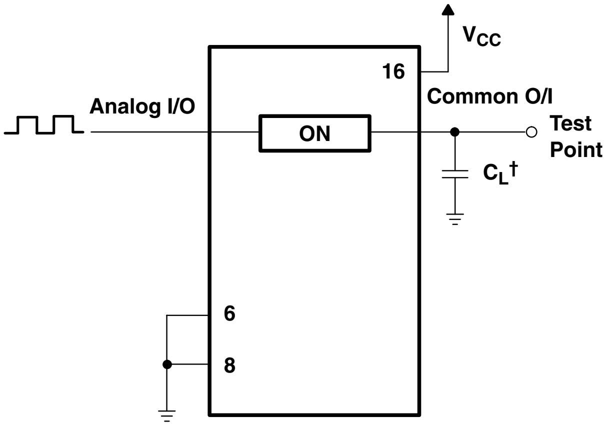


Figure 11. Propagation Delays, Analog In to Analog Out



† Includes all probe and jig capacitance

Figure 12. Propagation-Delay Test Setup, Analog In to Analog Out

PARAMETER MEASUREMENT INFORMATION

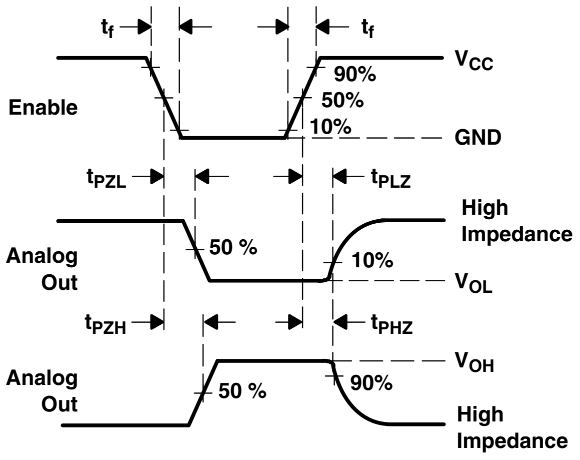


Figure 13. Propagation Delays, Enable to Analog Out

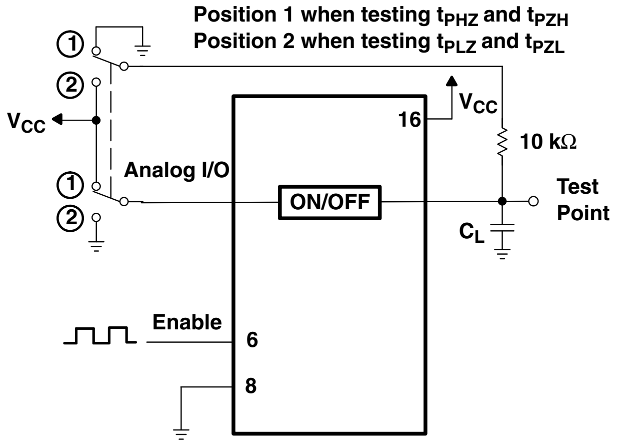


Figure 14. Propagation-Delay Test Setup, Enable to Analog Out

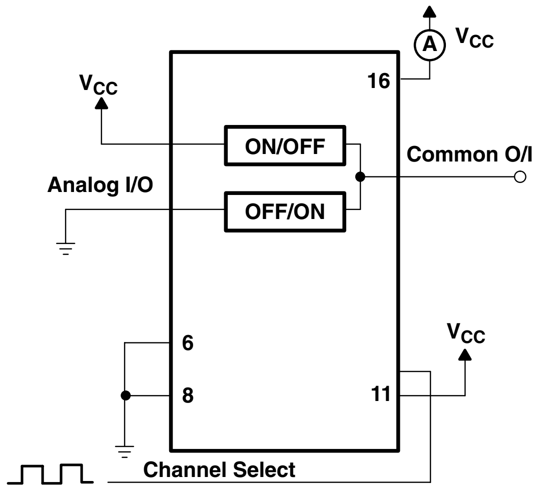


Figure 15. Power-Dissipation Capacitance Test Setup

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74HC4851QDRG4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4851QDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4851QPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC4851QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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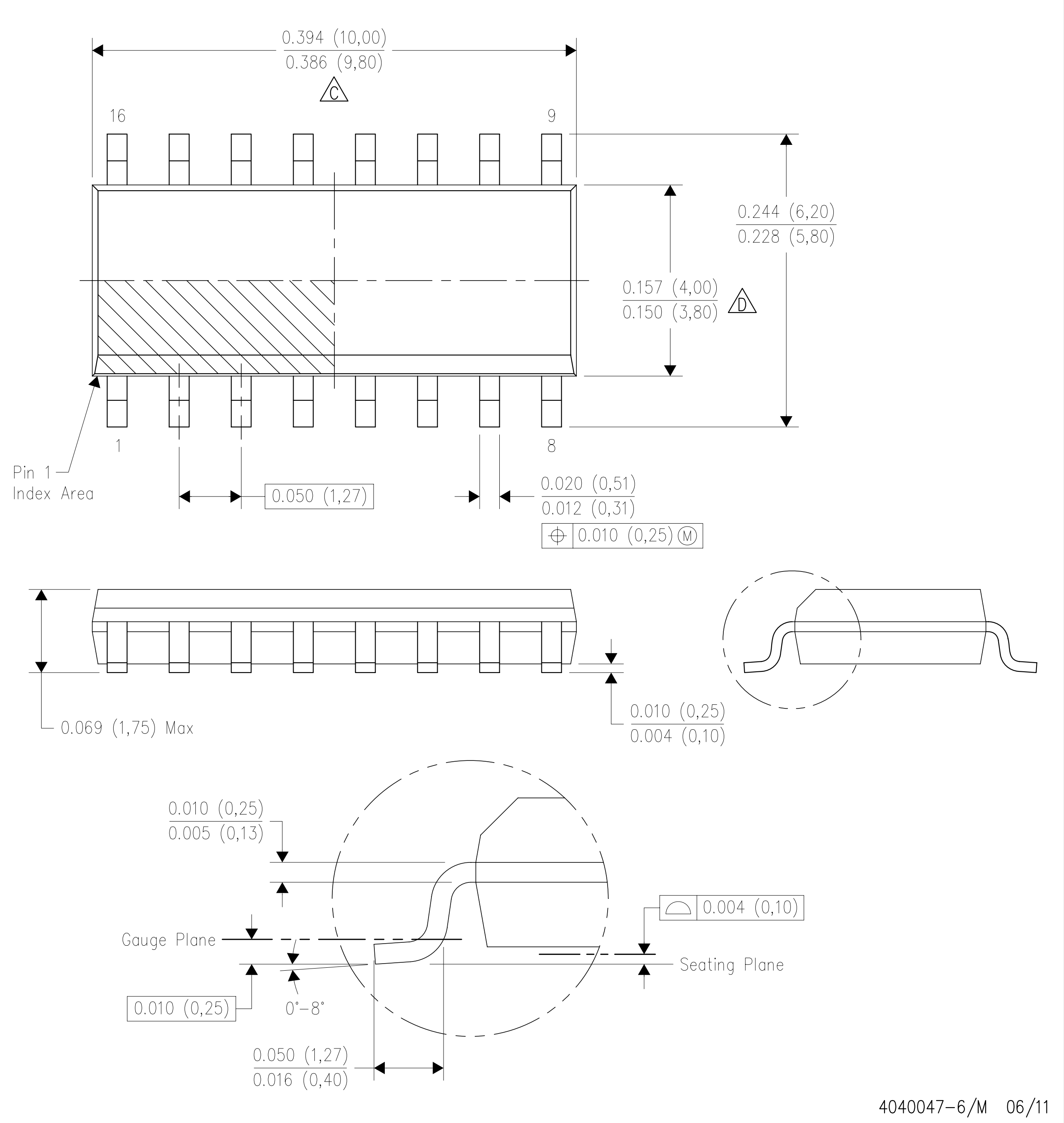
OTHER QUALIFIED VERSIONS OF SN74HC4851-Q1 :

- Catalog: SN74HC4851

NOTE: Qualified Version Definitions:

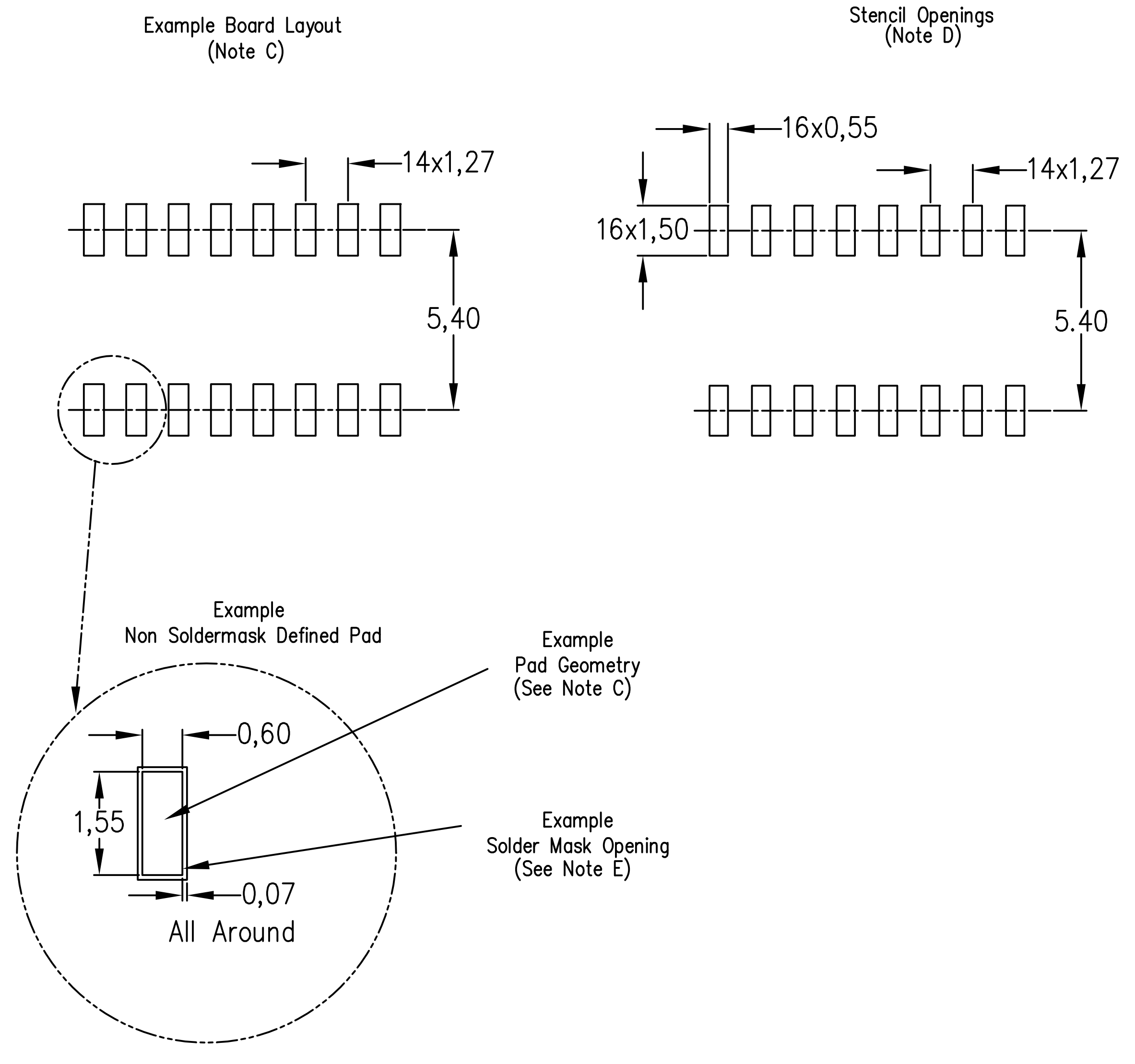
  - Catalog - TI's standard catalog product

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



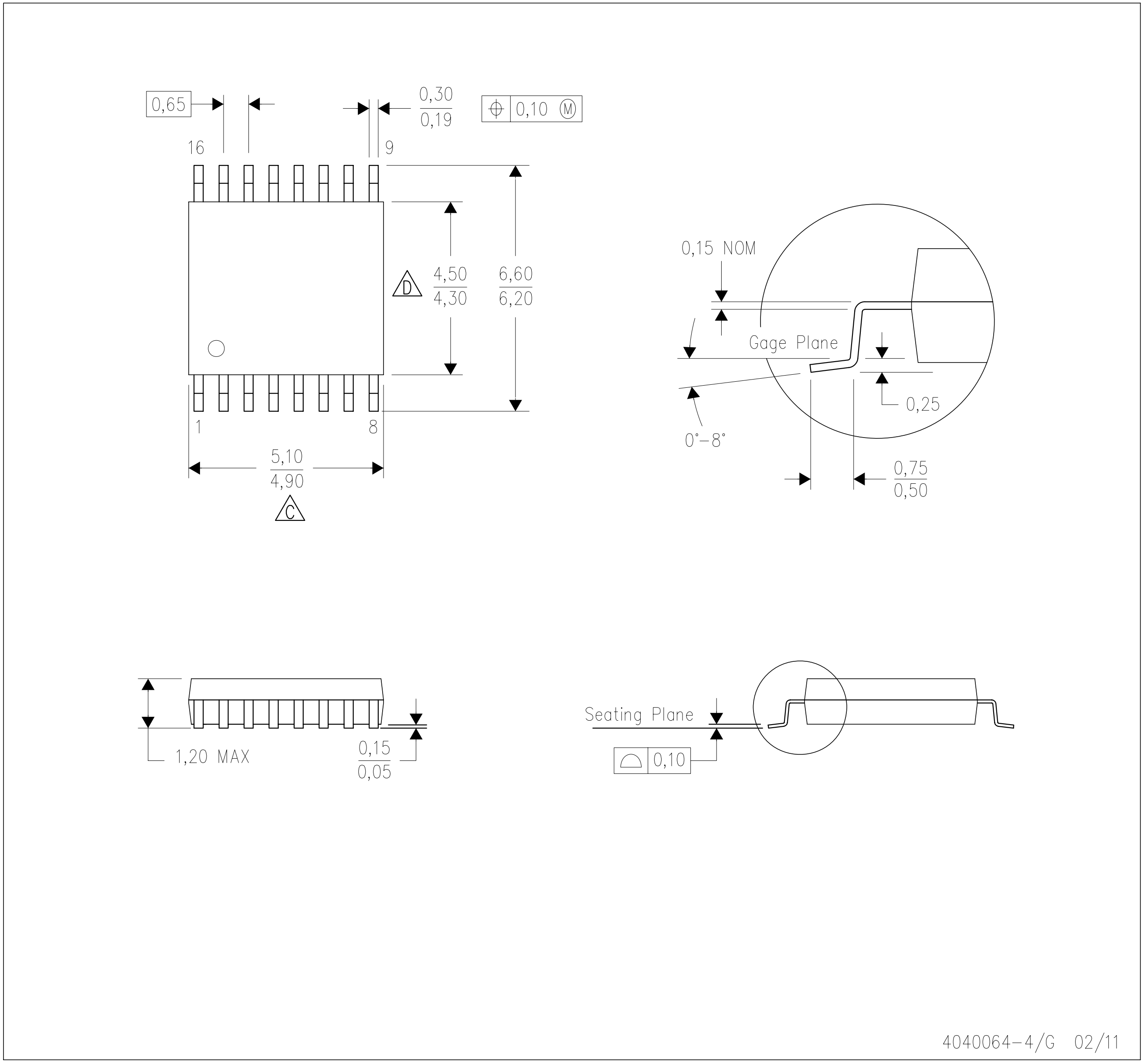
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



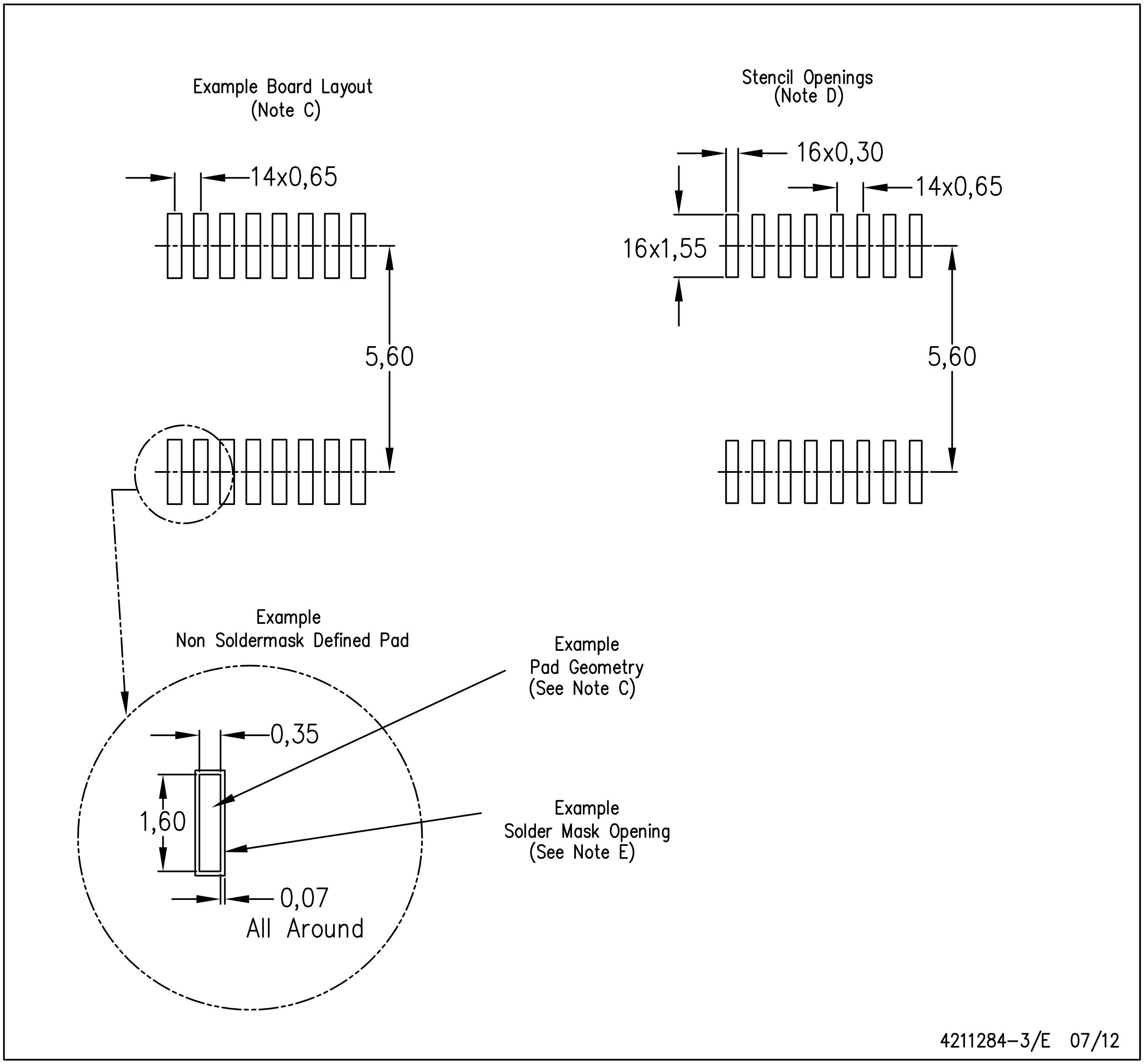
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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