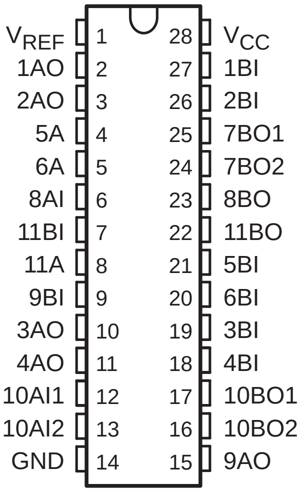
SN74GTL2006
13-BIT GTL-/GTL/GTL+ TO LVTTL TRANSLATOR

SCES619 – DECEMBER 2004

- **Operates as GTL-/GTL/GTL+ to LVTTL or LVTTL to GTL-/GTL/GTL+ Translator**
- **Series Termination on TTL Outputs of 30 Ω**
- **Latch-Up Testing to JEDEC Standard JESD 78 Exceeds 500 mA**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

PW PACKAGE
(TOP VIEW)



description

The SN74GTL2006 is a 13-bit translator to interface between the 3.3-V LVTTL chipset I/O and the Xeon™ processor GTL-/GTL/GTL+ I/O. The device is designed for platform health management in dual-processor applications.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	V_{REF}	GTL reference voltage
2–6, 8, 10–13, 15	nAn	Data inputs/outputs (LVTTL)
7, 9, 16, 17–27	nBn	Data inputs/outputs (GTL−/GTL/GTL+)
14	GND	Ground (0 V)
28	V_{CC}	Positive supply voltage

ORDERING INFORMATION

T_A	PACKAGE[†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	TSSOP − PW	Tube	SN74GTL2006PW	GK2006
		Tape and reel	SN74GTL2006PWR	GK2006

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design, guidelines are available at www.ti.com/sc/package.

Function Tables

INPUTS 1BI/2BI/3BI/4BI/9BI	OUTPUTS 1AO/2AO/3AO/4AO/9AO
L	L
H	H

INPUT 8AI	OUTPUT 8BO
L	L
H	H

INPUTS		OUTPUTS
10AI1/10AI2	9BI	10BO1/10BO2
L	L	L
L	H	L
H	L	L
H	H	H

INPUTS 5BI/6BI	INPUTS/OUTPUTS 5A/6A (OPEN DRAIN)	OUTPUTS 7BO1/7BO2
L	L	H[†]
H	L[‡]	L
H	H	H

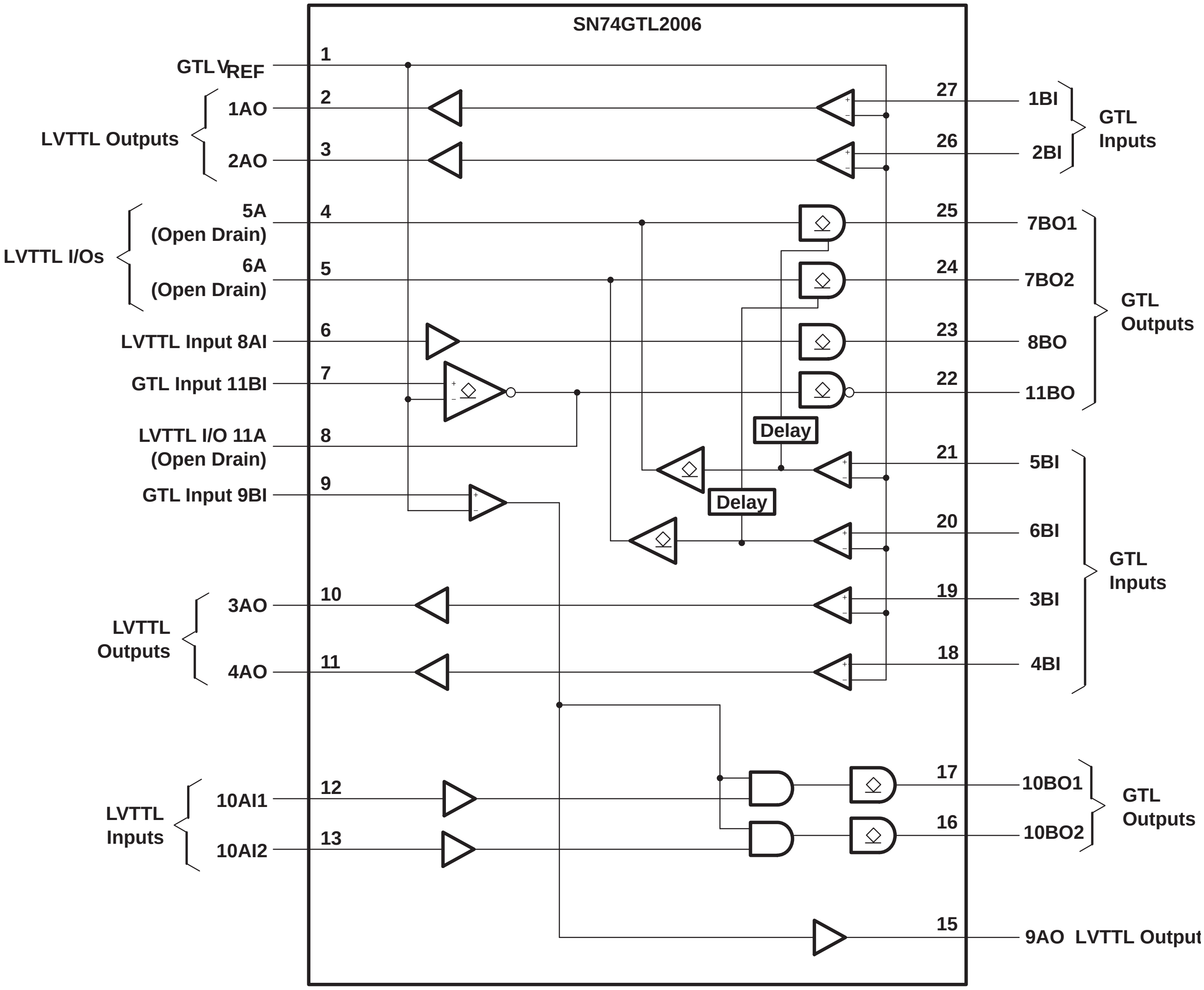
[†] The enable on 7BO1/7BO2 includes a delay that prevents a transient condition (when 5BI/6BI goes from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

[‡] Open-drain input/output terminal is driven to a logic-low state by an external driver.

INPUT 11BI	INPUT/OUTPUT 11A (OPEN DRAIN)	OUTPUT 11BO
L	H	L
L	L[‡]	H
H	L	H

[‡] Open-drain input/output terminal is driven to a logic-low state by an external driver.

logic symbol



NOTE A: The enable on 7BO1/7BO2 includes a delay that prevents a transient conditon (where 5BI/6BI go from low to high, and the low to high on 5A/6A lags up to 100 ns) from causing a low glitch on the 7BO1/7BO2 outputs.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Supply voltage range, V_{CC}	−0.5 to 4.6 V
Input voltage range, V_I (see Note 2): A port (LVTTL)	−0.5 to 4.6 V
B port (GTL)	−0.5 to 4.6 V
Output voltage range, V_O (output in OFF or HIGH state)(see Note 2): A port	−0.5 to 4.6 V
B port	−0.5 to 4.6 V
Input diode current, I_{IK} ($V_I < 0$)	−50 mA
Output diode current, I_{OK} ($V_O < 0$)	−50 mA
Current into any output in the LOW state: A port	32 mA
B port	30 mA
Current into any output in the HIGH state, A port	−32 mA
Storage temperature range, T_{stg}	−60 to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Voltages are referenced to GND (ground = 0 V).

NOTES: 1. The performance capability of a high-performance integrated circuit, in conjunction with its thermal environment, can create junction temperatures that are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.

2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{TT}	Termination voltage	GTL−	0.85	0.9	0.95	V
		GTL	1.14	1.2	1.26	
		GTL+	1.35	1.5	1.65	
V_{REF}	Reference voltage	Overall	0.5	2/3 V_{TT}	1.8	V
		GTL−	0.5	0.6	0.63	
		GTL	0.76	0.8	0.84	
		GTL+	0.87	1	1.1	
V_I	Input voltage	A port	0	3.3	3.6	V
		B port	0	V_{TT}	3.6	
V_{IH}	High-level input voltage	A port	2			V
		B port	V_{REF} + 50 mV			
V_{IL}	Low-level input voltage	A port			0.8	V
		B port			V_{REF} − 50 mV	
I_{OH}	High-level output current	A port			−16	mA
I_{OL}	Low-level output current	A port			16	mA
		B port			15	
T_A	Operating free-air temperature range		−40		85	°C

electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS		–40°C TO 85°C			UNIT
				MIN	TYP[†]	MAX	
V_{OH}[‡]	A port	V_{CC} = 3 V to 3.6 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 3 V,	I_{OH} = –16 mA	2.1			
V_{OL}[‡]	A port	V_{CC} = 3 V,	I_{OL} = 16 mA			0.8	V
	B port	V_{CC} = 3 V,	I_{OL} = 15 mA			0.4	
I_I	A port	V_{CC} = 3.6 V	V_I = V_{CC}			±1	µA
			V_I = 0 V			±1	
	B port	V_{CC} = 3.6 V,	V_I = V_{TT} or GND			±1	
I_{CC}	A or B port	V_{CC} = 3.6 V,	V_I = V_{CC} or GND, I_O = 0			12	mA
ΔI_{CC}[§]	A port or control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} – 0.6 V			500	µA
C_{IO}	A port	V_O = 3 V or 0,	V_O = 3 V or 0		5		pF
	B port	V_O = V_{TT} or 0,	V_O = V_{TT} or 0		4		

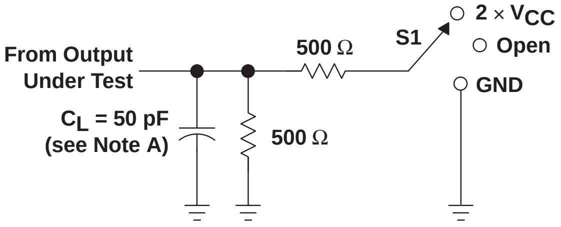
[†] All typical values are measured at V_{CC} = 3.3 V and T_A = 25°C.
[‡] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[§] This is the increase in supply current for each input that is at the specified LVTTL voltage, rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range

PARAMETER		WAVEFORM	GTL−			GTL			GTL+			UNIT
			V_{CC} = 3.3 V ± 0.3 V, V_{REF} = 0.6 V			V_{CC} = 3.3 V ± 0.3 V, V_{REF} = 0.8 V			V_{CC} = 3.3 V ± 0.3 V, V_{REF} = 1 V			
			MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
t_{PLH}	An to Bn	1	2	4	8	2	4	8	2	4	8	ns
t_{PHL}			2	5.5	10	2	5.5	10	2	5.5	10	
t_{PLH}	Bn to An	2	2	5.5	10	2	5.5	10	2	5.5	10	ns
t_{PHL}			2	5.5	10	2	5.5	10	2	5.5	10	
t_{PLH}	9BI to 10BOn	3	2	6	11	2	6	11	2	6	11	ns
t_{PHL}			2	6	11	2	6	11	2	6	11	
t_{PLH}	11BI to 11BO	3	2	8	13	2	8	13	2	8	13	ns
t_{PHL}[¶]			2	14	21	2	14	21	2	14	21	
t_{PLH}	Bn to Bn	3	4	7	11	4	7	11	4	7	11	ns
t_{PHL}			120	205	350	120	205	350	120	205	350	
t_{PLZ}	Bn to An (I/O)	4	2	5	10	2	5	10	2	5	10	ns
t_{PZL}			2	5	10	2	5	10	2	5	10	

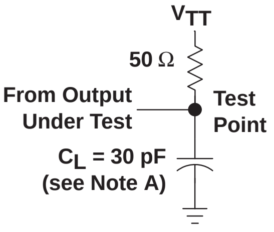
[†] All typical values are measured at V_{CC} = 3.3 V and T_A = 25°C.
[¶] Includes ~7.6-ns RC rise time of test-load pullup on 11-A, 1.5-kΩ pullup, and 21-pF load on 11 A has approximately 23-ns RC rise time.

PARAMETER MEASUREMENT INFORMATION
V_{TT} = 1.2 V, V_{REF} = 0.8 V FOR GTL AND V_{TT} = 1.5 V, V_{REF} = 1 V FOR GTL+

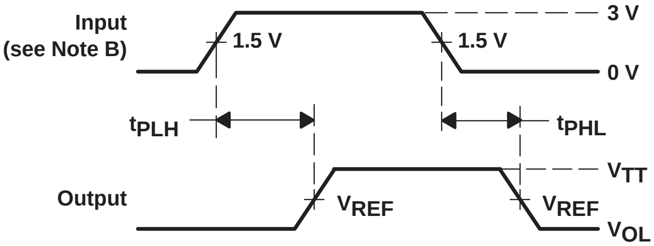


LOAD CIRCUIT FOR A OUTPUTS

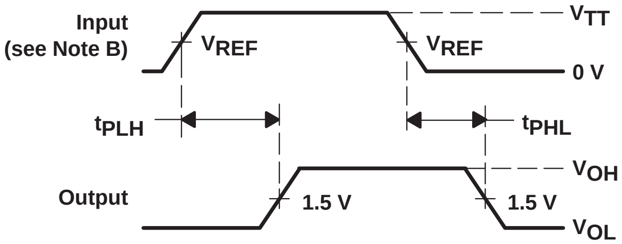
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}



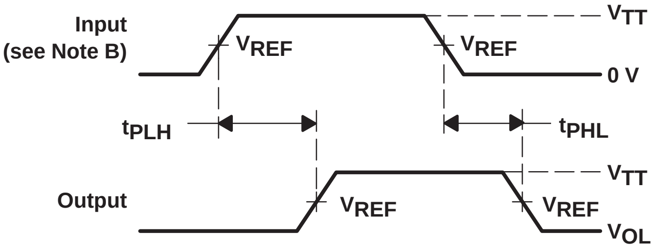
LOAD CIRCUIT FOR B OUTPUTS



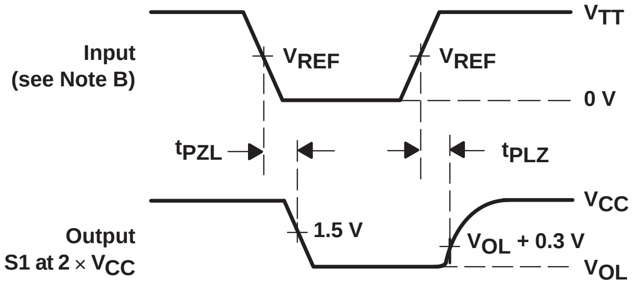
VOLTAGE WAVEFORM 1
PROPAGATION DELAY TIMES
(A port to B port)†



VOLTAGE WAVEFORM 2
PROPAGATION DELAY TIMES
(B port to A port)†



VOLTAGE WAVEFORM 3
PROPAGATION DELAY TIMES
(B port to B port)†



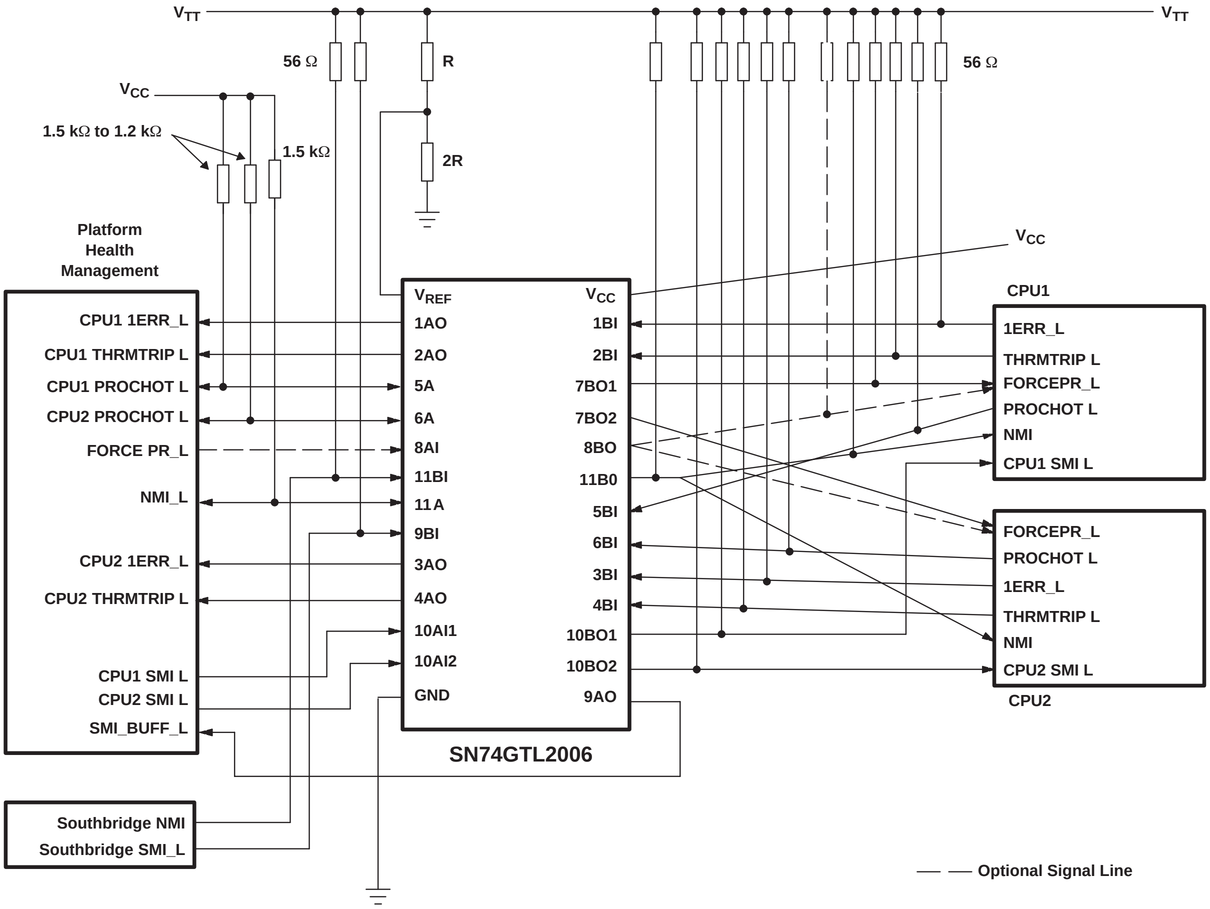
VOLTAGE WAVEFORM 4
PROPAGATION DELAY TIMES
(B port to A (I/O) port)†

† All control inputs are LVTTL levels.

NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

APPLICATION INFORMATION



frequently asked questions

Question 1: On SN74GTL2006 LVTTL inputs, specifically 10AI1 and 10AI2, when the device is powered down, these inputs may be pulled up to 3.3 V, and we want to ensure that there is no leakage path to the power rail under this condition. Are the LVTTL inputs high impedance when the device is powered down, and will there be any leakage?

Answer 1: When the device is powered down, the LVTTL inputs are in a high-impedance state and do not leak to V_{DD} if they are pulled high while the device is powered down.

Question 2: Do all the LVTTL inputs have the same powered-down characteristic?

Answer 2: Yes

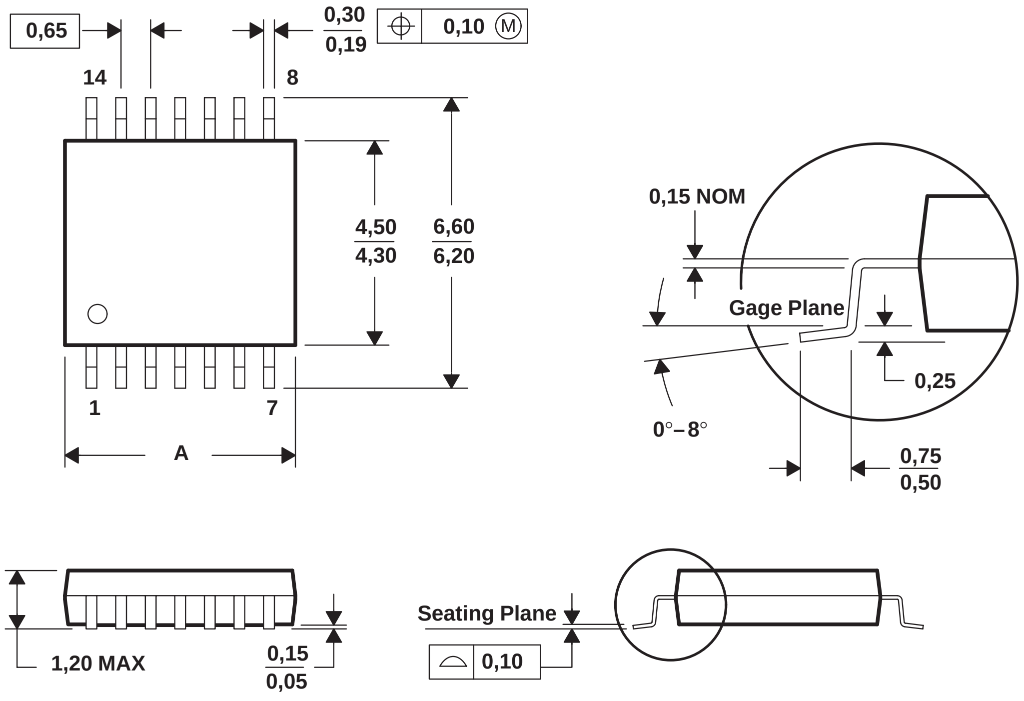
Question 3: What is the condition of the other GTL I/O and LVTTL output pins when the device is powered down?

Answer 3: The open-drain outputs, both GTL and LVTTL, do not leak to the power supply if they are pulled high while the device is powered down. The GTL inputs also do not leak to the power supply under the same conditions. The LVTTL totem-pole outputs, however, are not open-drain type outputs, and there will be current flow on these pins if they are pulled high when V_{DD} is at ground.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2004, Texas Instruments Incorporated