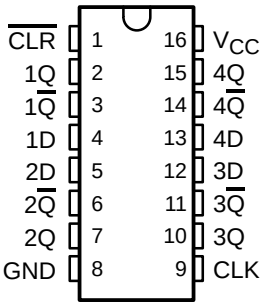
- **Contains Four Flip-Flops With Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  - **Buffer/Storage Registers**
  - **Shift Registers**
  - **Pattern Generators**

D, N, OR NS PACKAGE
(TOP VIEW)



description

This positive-edge-triggered flip-flop utilizes TTL circuitry to implement D-type flip-flop logic with a direct clear ($\overline{CLR}$) input. Information at the data (D) inputs meeting setup-time requirements is transferred to outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

ORDERING INFORMATION

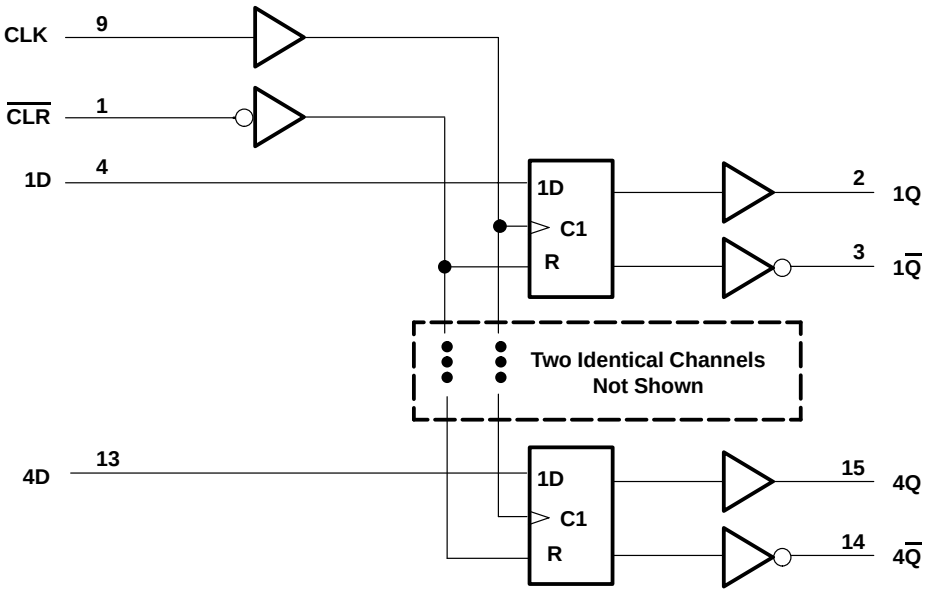
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74F175N	SN74F175N
	SOIC – D	Tube	SN74F175D	F175
		Tape and reel	SN74F175DR	
	SOP – NS	Tape and reel	SN74F175NSR	74F175

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . –30 mA to 5 mA
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 73°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded if the input current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –1 mA	2.5	3.4		V
	V_{CC} = 4.75 V,	I_{OH} = –1 mA	2.7			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.6	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	–60		–150	mA
I_{CC}	V_{CC} = 5.5 V,	See Note 4		22.5	34	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 4: I_{CC} is measured with outputs open, with 4.5 V applied to all data inputs after a momentary ground, followed by 4.5 V applied to CLK.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

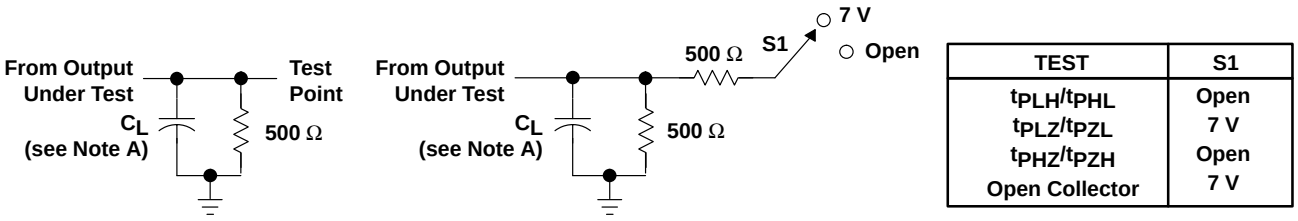
			V_{CC} = 5 V, T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency			100		100	MHz
t_w	Pulse duration	CLK high	4		4		ns
		CLK low	5		5		
		$\overline{CLR}$ low	5		5		
t_{su}	Setup time, data before CLK↑	High or low	3		3		ns
	Setup time, inactive state, data before CLK↑§	$\overline{CLR}$ high	5		5		
t_h	Hold time, data after CLK↑	High or low	1		1		ns

§ Inactive-state setup time also is referred to as recovery time.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
f_{max}			100	140		100		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3.2	4.6	6.5	3.2	7.5	ns
t_{PHL}			3.2	6.1	8.5	3.2	9.5	
t_{PLH}	$\overline{CLR}$	$\overline{Q}$	3.2	6.1	8.5	3.2	9	ns
t_{PHL}		Q	3.7	8.6	11.5	3.7	13	

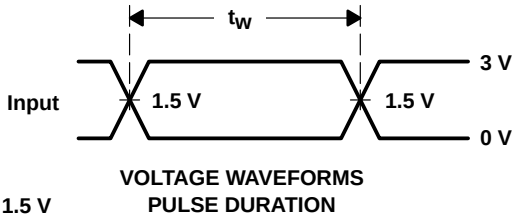
PARAMETER MEASUREMENT INFORMATION



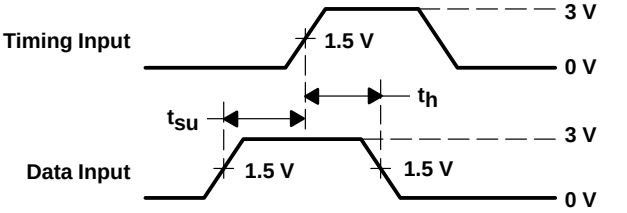
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open
Open Collector	7 V

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

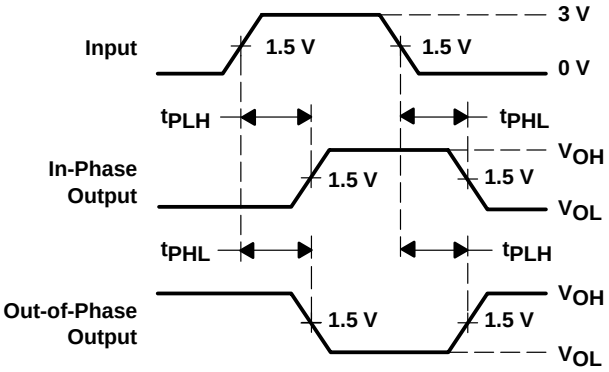


VOLTAGE WAVEFORMS PULSE DURATION

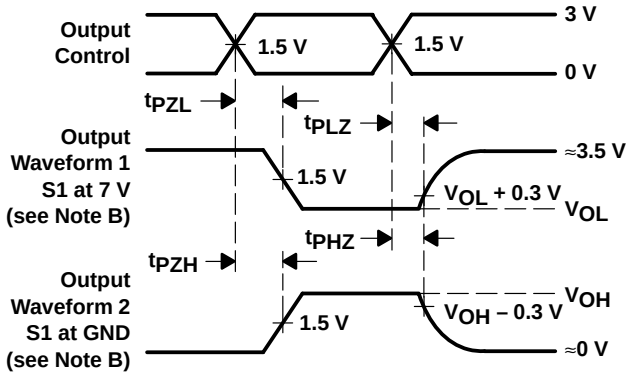


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

1.5 V



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns, duty cycle = 50%.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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