

SN74CBTD3384C

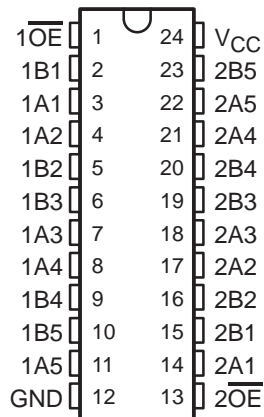
10-BIT FET BUS SWITCH WITH LEVEL SHIFTING

5-V BUS SWITCH WITH –2-V UNDERSHOOT PROTECTION

SCDS133A – SEPTEMBER 2003 – REVISED OCTOBER 2003

- Undershoot Protection for Off-Isolation on A and B Ports Up To –2 V
- Integrated Diode to V_{CC} Provides 5-V Input Down To 3.3-V Output Level Shift
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low ON-State Resistance (r_{on}) Characteristics ($r_{on} = 3\ \Omega$ Typical)
- Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)} = 5\text{ pF}$ Typical)
- Data and Control Inputs Provide Undershoot Clamp Diodes
- V_{CC} Operating Range From 4.5 V to 5.5 V
- Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)
- Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- Supports Both Digital and Analog Applications: Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating

DB, DBQ, DGV, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74CBTD3384CDW	CBTD3384C
		Tape and reel	SN74CBTD3384CDWR	
	SSOP – DB	Tube	SN74CBTD3384CDB	CC384C
		Tape and reel	SN74CBTD3384CDBR	
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBTD3384CDBQR	CBTD3384C
	TSSOP – PW	Tube	SN74CBTD3384CPW	CC384C
		Tape and reel	SN74CBTD3384CPWR	
	TVSOP – DGV	Tape and reel	SN74CBTD3384CDGVR	CC384C

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
INSTRUMENTS**

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description/ordering information (continued)

The SN74CBTD3384C is a high-speed TTL-compatible FET bus switch with low ON-state resistance (r_{on}), allowing for minimal propagation delay. This device features an integrated diode in series with V_{CC} to provide level shifting for 5-V input down to 3.3-V output levels. Active Undershoot-Protection Circuitry on the A and B ports of the SN74CBTD3384C provides protection for undershoot up to –2 V by sensing an undershoot event and ensuring that the switch remains in the proper OFF state.

The SN74CBTD3384C is organized as two 5-bit bus switches with separate output-enable ($1\overline{OE}$, $2\overline{OE}$) inputs. It can be used as two 5-bit bus switches or as one 10-bit bus switch. When \overline{OE} is low, the associated 5-bit bus switch is ON, and the A port is connected to the B port, allowing bidirectional data flow between ports. When \overline{OE} is high, the associated 5-bit bus switch is OFF, and a high-impedance state exists between the A and B ports.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

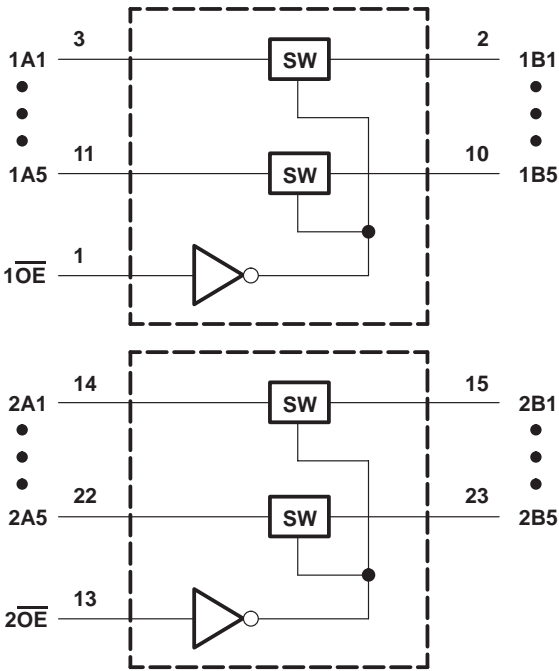
To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

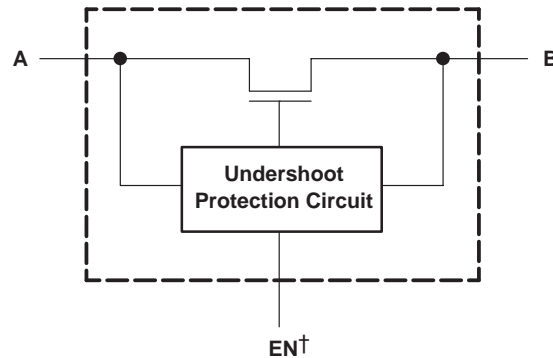
(each 5-bit bus switch)

INPUT \overline{OE}	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	–0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2)	–0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3)	–0.5 V to 7 V
Control input clamp current, I_{IK} ($V_{IN} < 0$)	–50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O} < 0$)	–50 mA
ON-state switch current, $I_{I/O}$ (see Note 4)	±128 mA
Continuous current through V_{CC} or GND terminals	±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DB package	63°C/W
DBQ package	61°C/W
DGV package	86°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to ground unless otherwise specified.
 2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
 4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 6 and 7)

	MIN	MAX	UNIT
V_{CC} Supply voltage	4.5	5.5	V
V_{IH} High-level control input voltage	2	5.5	V
V_{IL} Low-level control input voltage	0	0.8	V
$V_{I/O}$ Data input/output voltage	0	5.5	V
T_A Operating free-air temperature	–40	85	°C

- NOTES:
6. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
 7. In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Control inputs	$V_{CC} = 4.5\text{ V}$,	$I_{IN} = -18\text{ mA}$			–1.8	V
V_{IKU}	Data inputs	$V_{CC} = 5\text{ V}$,	$0\text{ mA} > I_I \geq -50\text{ mA}$, $V_{IN} = V_{CC}$ or GND, Switch OFF			–2	V
V_{OH}		See Figures 4 and 5					
I_{IN}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_{IN} = V_{CC}$ or GND			± 1	μA
I_{OZ}^\ddagger		$V_{CC} = 5.5\text{ V}$,	$V_O = 0$ to 5.5 V , $V_I = 0$, Switch OFF, $V_{IN} = V_{CC}$ or GND			± 10	μA
I_{off}		$V_{CC} = 0$,	$V_O = 0$ to 5.5 V , $V_I = 0$			10	μA
I_{CC}		$V_{CC} = 5.5\text{ V}$,	$I_{I/O} = 0$, $V_{IN} = V_{CC}$ or GND, Switch ON or OFF			1.5	mA
ΔI_{CC}^\S	Control inputs	$V_{CC} = 5.5\text{ V}$,	One input at 3.4 V , Other inputs at V_{CC} or GND			2.5	mA
C_{in}	Control inputs	$V_{IN} = 3\text{ V}$ or 0				3.5	pF
$C_{io(OFF)}$		$V_{I/O} = 3\text{ V}$ or 0 ,	Switch OFF, $V_{IN} = V_{CC}$ or GND			5	pF
$C_{io(ON)}$		$V_{I/O} = 3\text{ V}$ or 0 ,	Switch ON, $V_{IN} = V_{CC}$ or GND			12.5	pF
r_{on}^\P		$V_{CC} = 4.5\text{ V}$	$V_I = 0$	$I_O = 64\text{ mA}$	3	6	Ω
				$I_O = 30\text{ mA}$	3	6	
			$V_I = 2.4\text{ V}$,	$I_O = -15\text{ mA}$	8	20	

 V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.† All typical values are at $V_{CC} = 5\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.§ This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	
$t_{pd}^\#$	A or B	B or A		0.15	ns
t_{en}	\overline{OE}	A or B	1.5	4.8	ns
t_{dis}	\overline{OE}	A or B	1.5	4.8	ns

The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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undershoot characteristics (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OUTU}	$V_{CC} = 5.5 \text{ V}$, Switch OFF, $V_{IN} = V_{CC}$ or GND	2	$V_{OH} - 0.3$		V

† All typical values are at $V_{CC} = 5 \text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

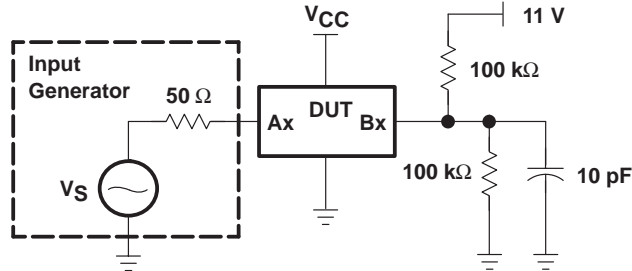


Figure 1. Device Test Setup

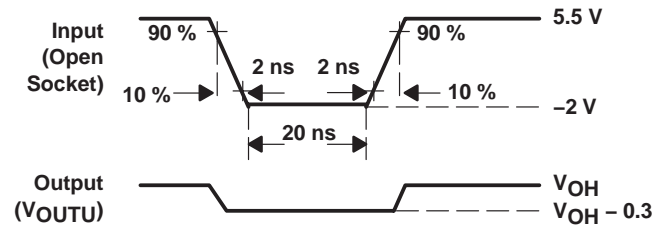


Figure 2. Transient Input Voltage (V_I) and Output Voltage (V_{OUTU}) Waveforms (Switch OFF)

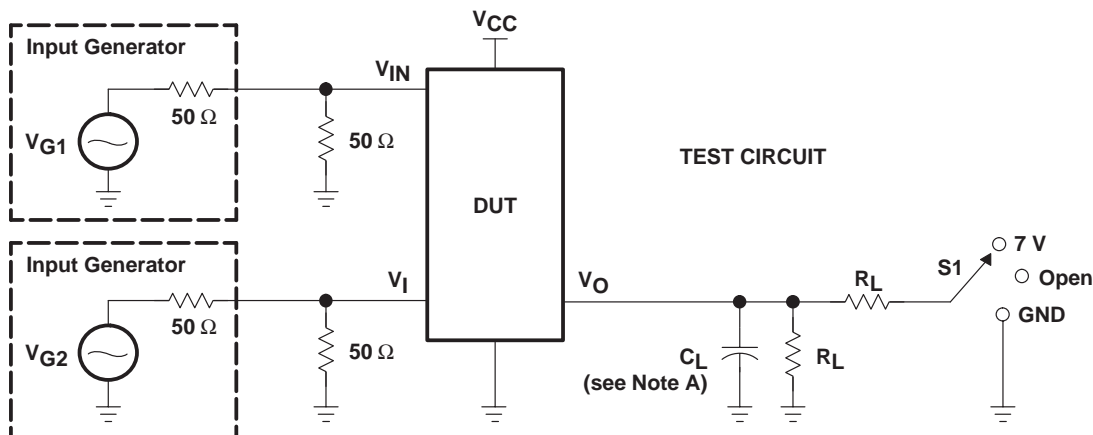
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10-BIT FET BUS SWITCH WITH LEVEL SHIFTING

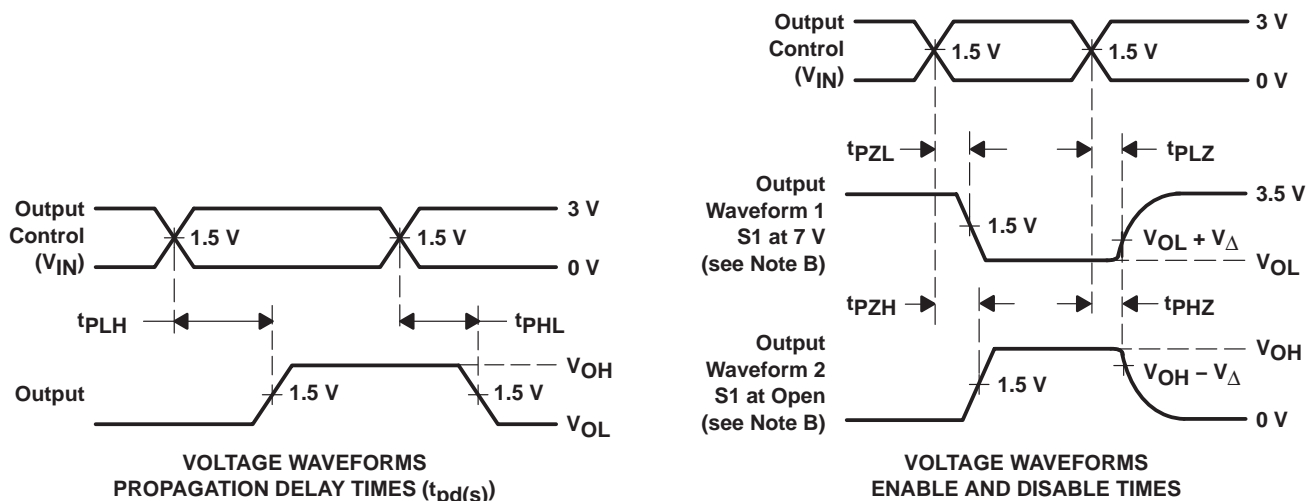
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PARAMETER MEASUREMENT INFORMATION FOR LEVEL SHIFTER



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd} (s)	5 V ± 0.5 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	5 V ± 0.5 V	7 V	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	5 V ± 0.5 V	Open	500 Ω	V _{CC}	50 pF	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd}(s). The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

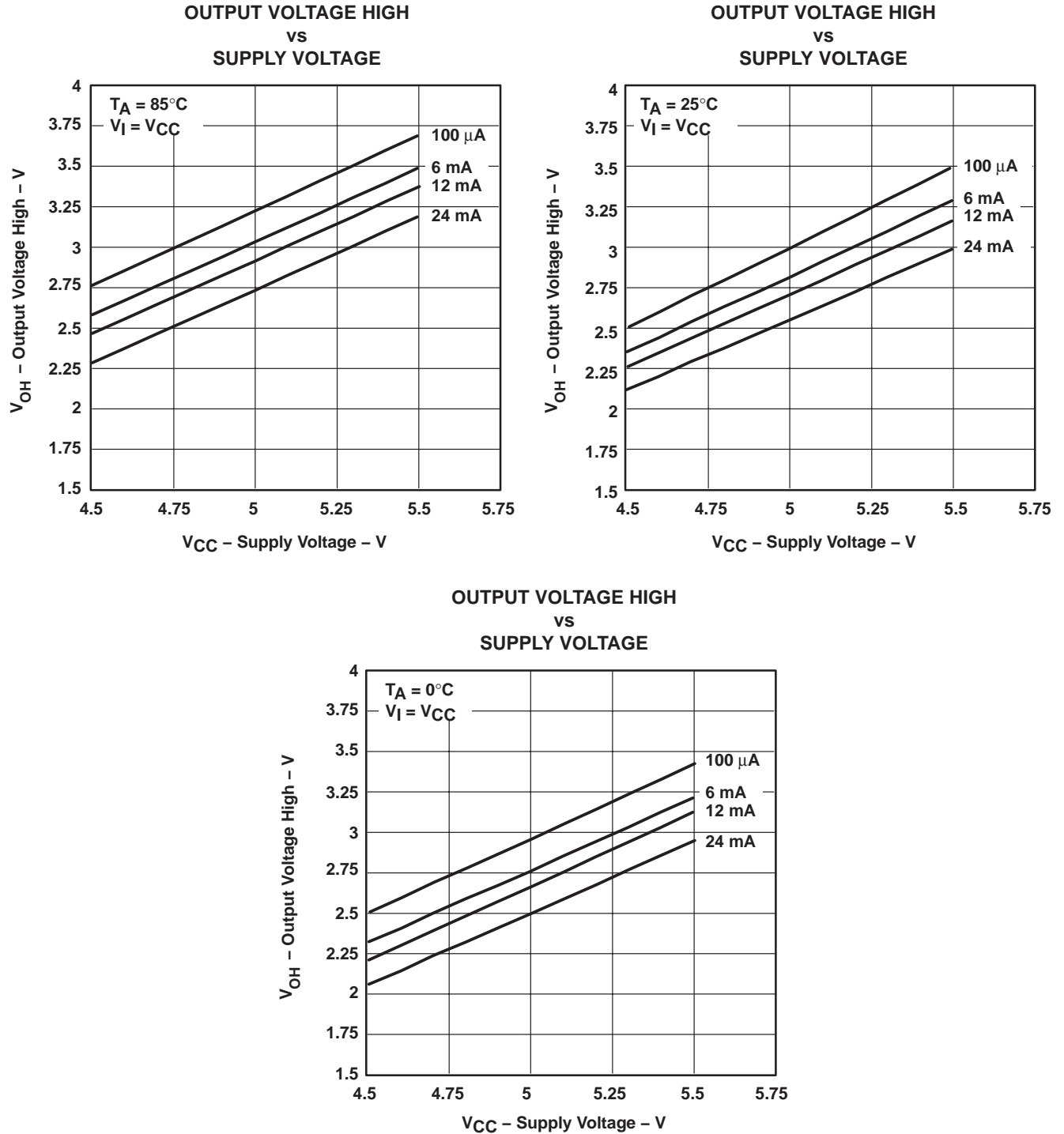


Figure 4. V_{OH} Values

TYPICAL CHARACTERISTICS (continued)

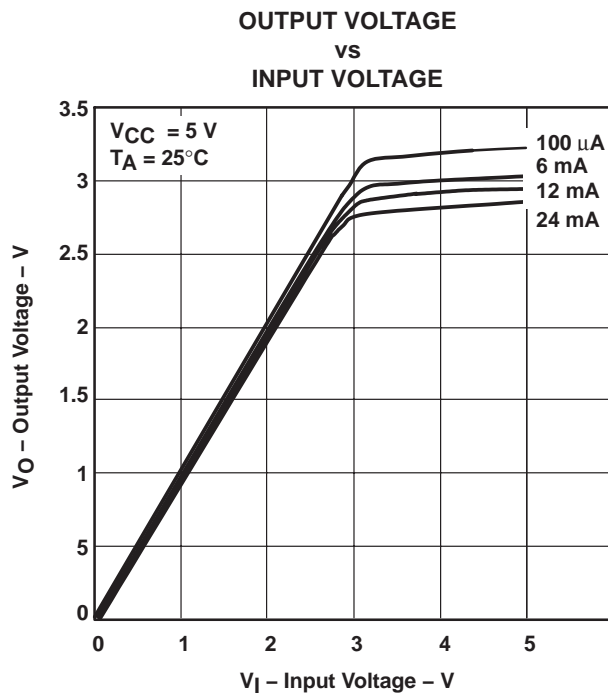
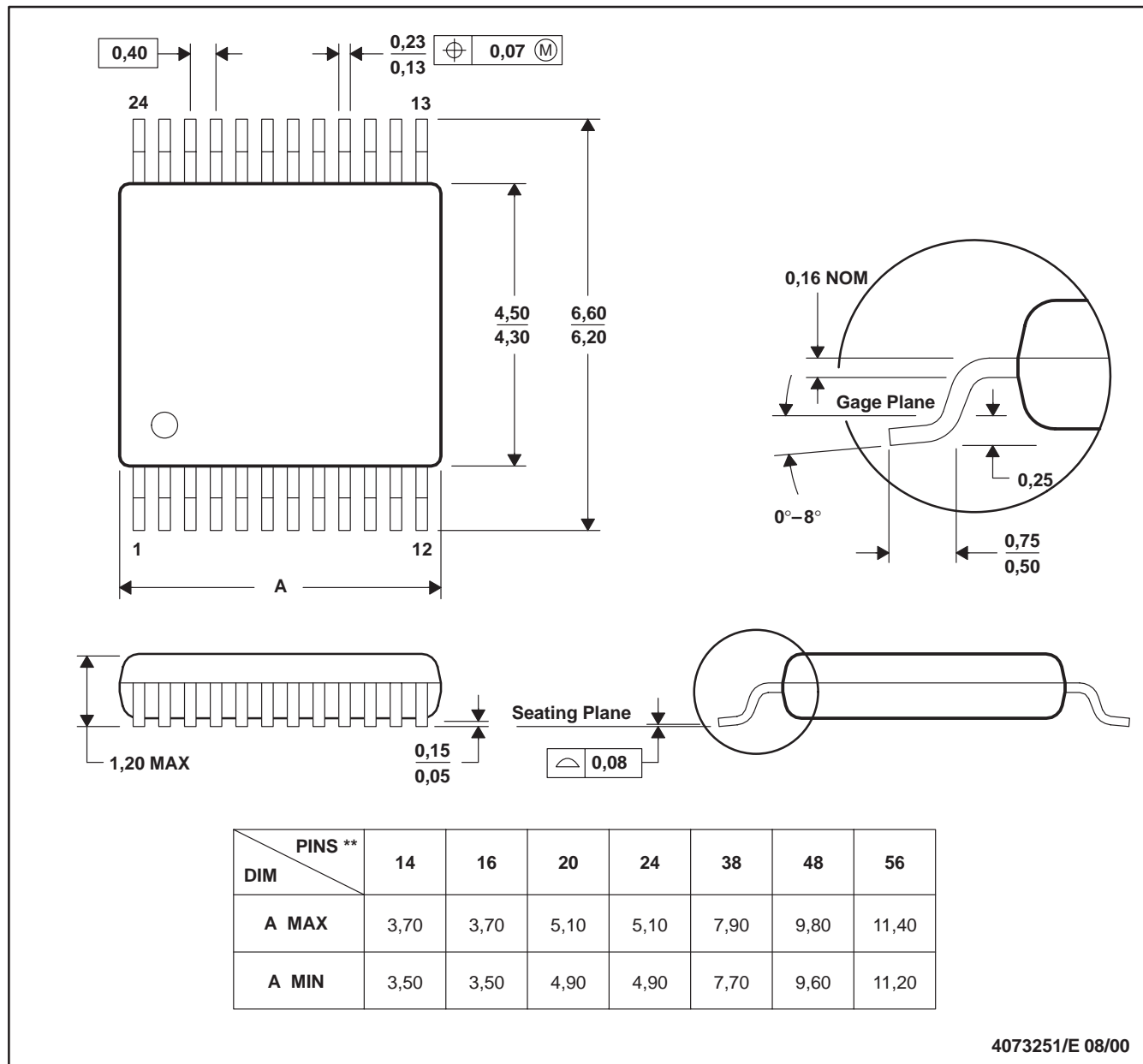


Figure 5. Data Output Voltage vs Data Input Voltage

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

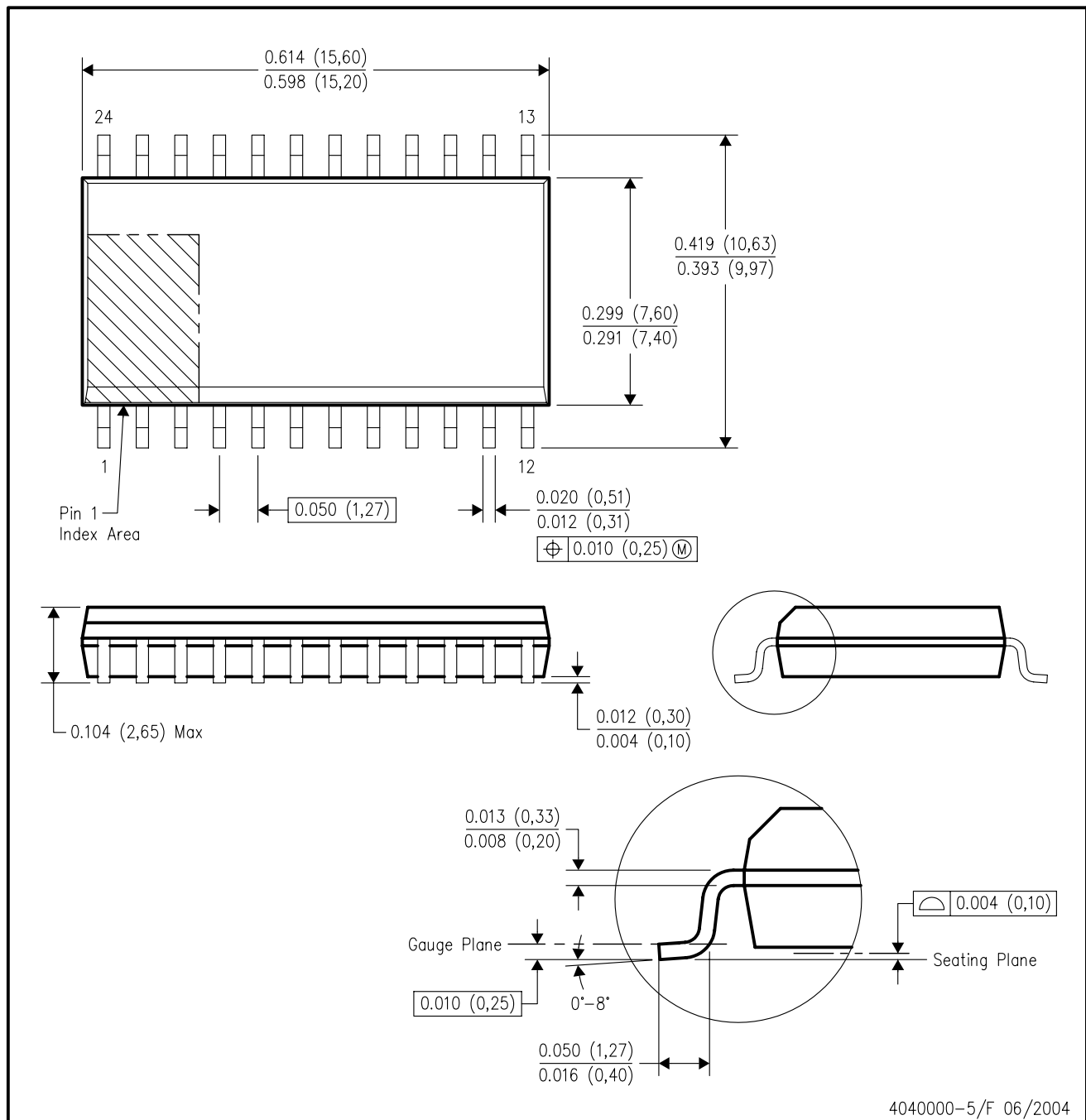
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G24)

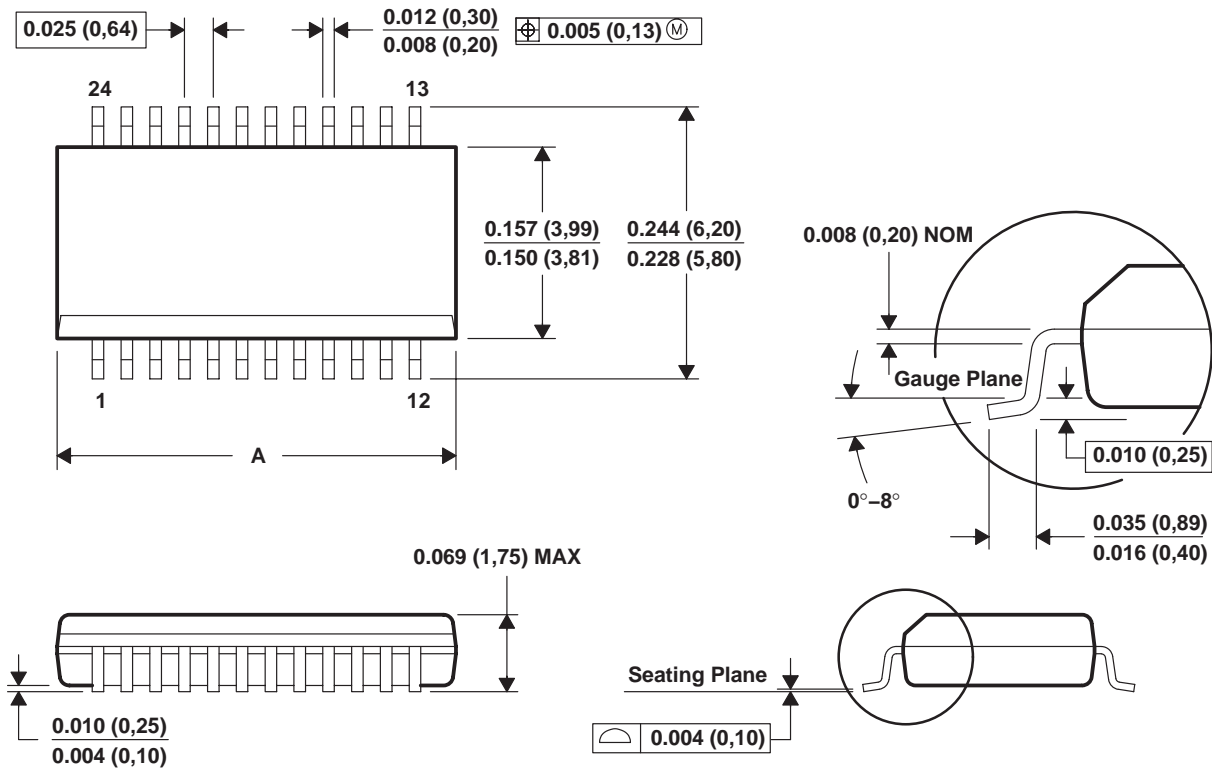
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE



PINS **	16	20	24	28
DIM				
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
MO-137 VARIATION	AB	AD	AE	AF

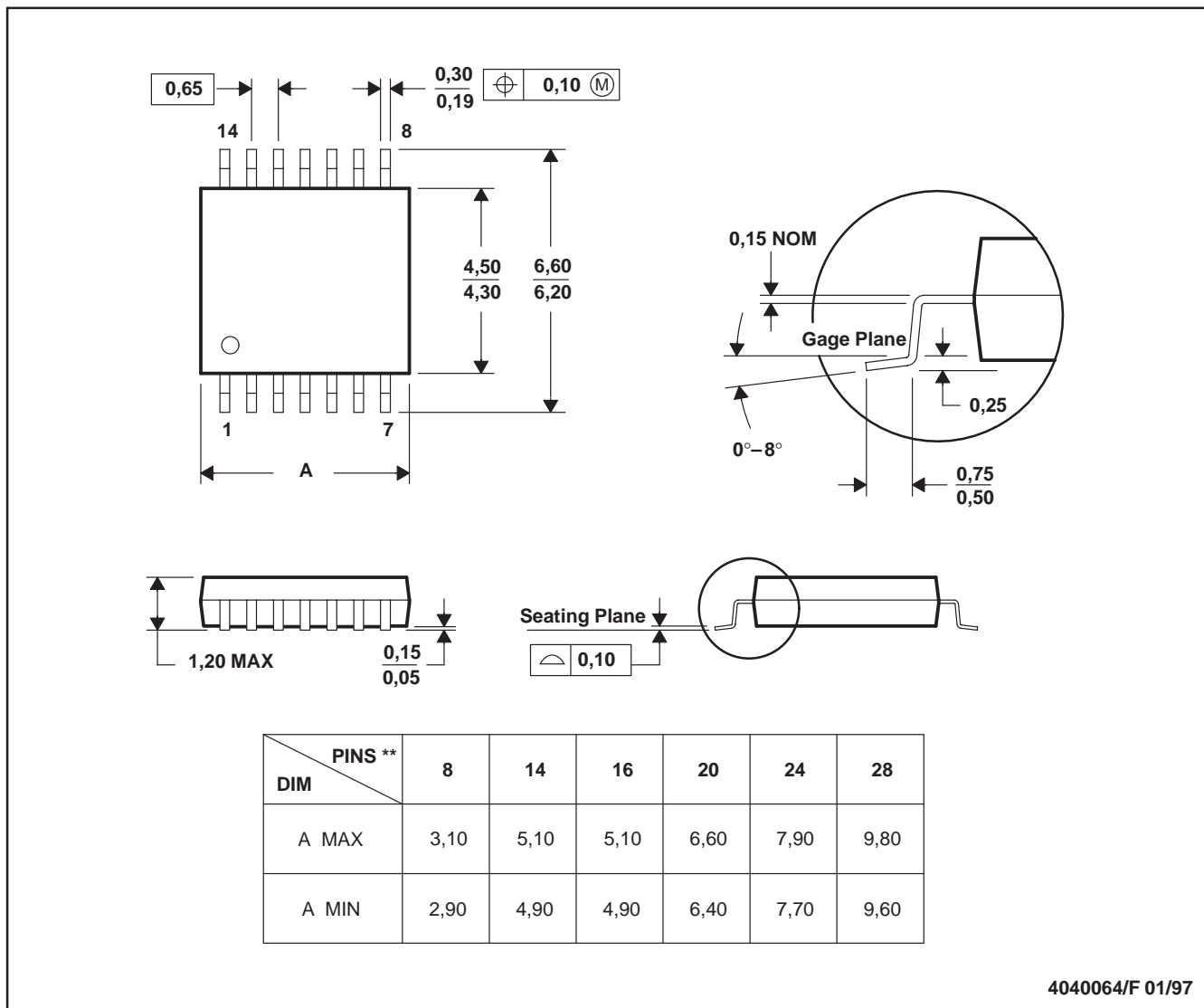
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- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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