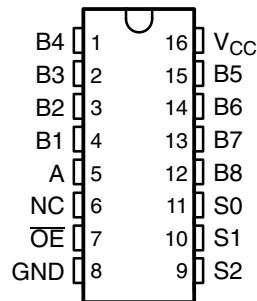


# SN74CBT3251 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

SCDS019L – MAY 1995 – REVISED JANUARY 2004

## ● 5-Ω Switch Connection Between Two Ports

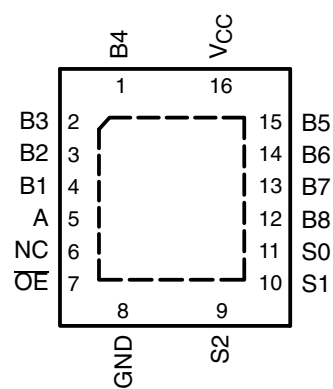
D, DB, DBQ, OR PW PACKAGE  
(TOP VIEW)



NC – No internal connection

## ● TTL-Compatible Input Levels

RGY PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN74CBT3251 is a 1-of-8 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

When output enable ( $\overline{OE}$ ) is low, the SN74CBT3251 is enabled. S0, S1, and S2 select one of the B outputs for the A-input data.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74CBT3251RGYR	CU251
	SOIC – D	Tube	SN74CBT3251D	CBT3251
		Tape and reel	SN74CBT3251DR	
	SSOP – DB	Tape and reel	SN74CBT3251DBR	CU251
	SSOP (QSOP) – DBQ	Tape and reel	SN74CBT3251DBQR	CU251
	TSSOP – PW	Tube	SN74CBT3251PW	CU251
		Tape and reel	SN74CBT3251PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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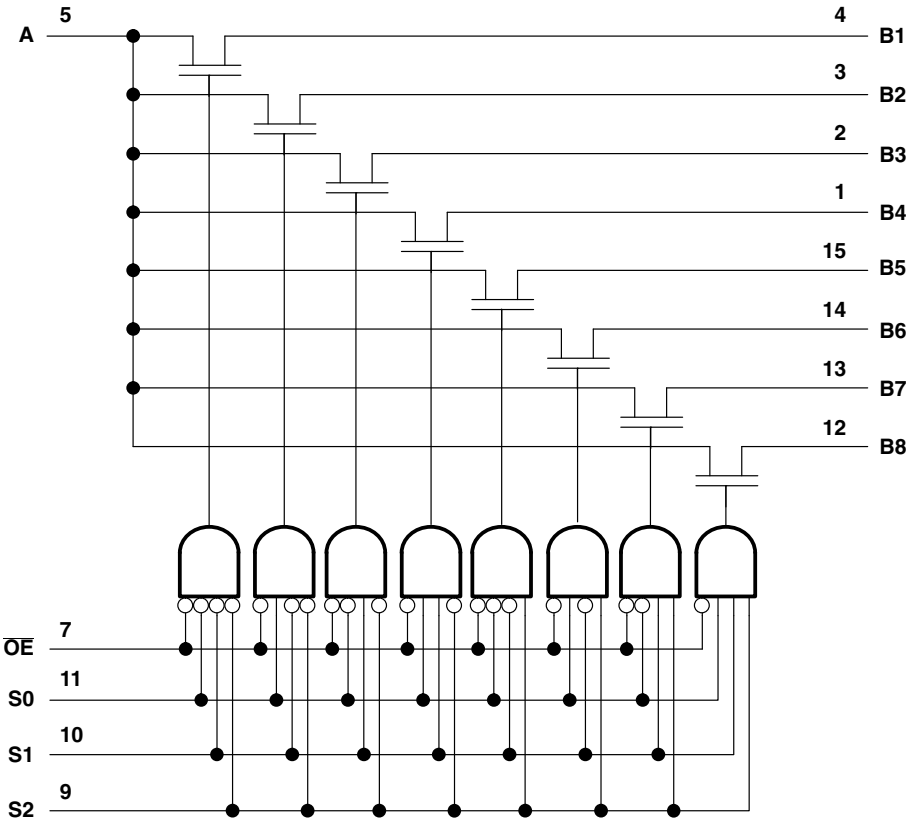
SN74CBT3251  
1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

SCDS019L – MAY 1995 – REVISED JANUARY 2004

FUNCTION TABLE  
(each multiplexer/demultiplexer)

INPUTS				FUNCTION
OE	S2	S1	S0	
L	L	L	L	A port = B1 port
L	L	L	H	A port = B2 port
L	L	H	L	A port = B3 port
L	L	H	H	A port = B4 port
L	H	L	L	A port = B5 port
L	H	L	H	A port = B6 port
L	H	H	L	A port = B7 port
L	H	H	H	A port = B8 port
H	X	X	X	Disconnect

logic diagram (positive logic)



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, $I_K$ ( $V_{I/O} < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
(see Note 2): DB package	82°C/W
(see Note 2): DBQ package	90°C/W
(see Note 2): PW package	108°C/W
(see Note 3): RGY package	39°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.  
3. The package thermal impedance is calculated in accordance with JESD 51-5.

**recommended operating conditions (see Note 4)**

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4	5.5	V
$V_{IH}$ High-level control input voltage	2		V
$V_{IL}$ Low-level control input voltage		0.8	V
$T_A$ Operating free-air temperature	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>‡</sup>	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.5$ V, $I_I = -18$ mA			–1.2	V
$I_I$	$V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND			±1	μA
$I_{CC}$	$V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND			3	μA
$\Delta I_{CC}$ <sup>§</sup>	Control inputs $V_{CC} = 5.5$ V, One input at 3.4 V, Other inputs at $V_{CC}$ or GND			2.5	mA
$C_i$	Control inputs $V_I = 3$ V or 0			3.5	pF
$C_{io(OFF)}$	A port			17.5	pF
	B port			4	
$r_{on}$ <sup>¶</sup>	$V_{CC} = 4$ V, TYP at $V_{CC} = 4$ V	$V_I = 2.4$ V,	$I_I = 15$ mA	14	Ω
	$V_{CC} = 4.5$ V	$V_I = 0$	$I_I = 64$ mA	5	
			$I_I = 30$ mA	5	
		$V_I = 2.4$ V,	$I_I = 15$ mA	10	

<sup>‡</sup> All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

<sup>§</sup> This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

<sup>¶</sup> Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

# SN74CBT3251

## 1-OF-8 FET MULTIPLEXER/DEMULTIPLEXER

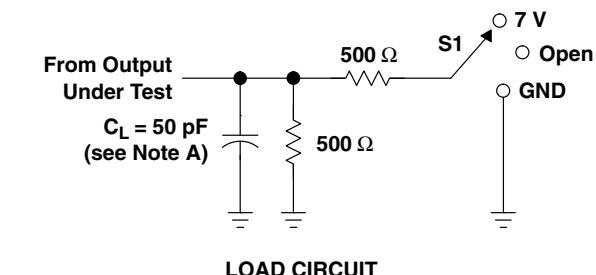
SCDS019L – MAY 1995 – REVISED JANUARY 2004

switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

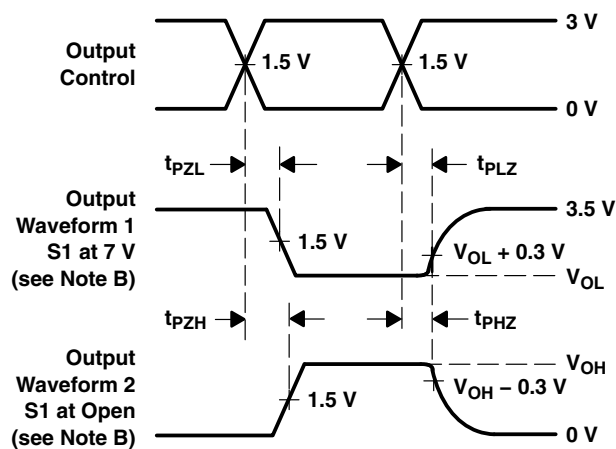
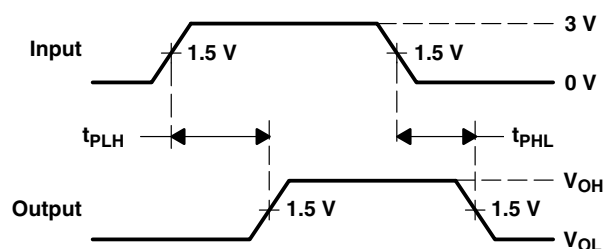
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub> <sup>†</sup>	A or B	B or A	0.35		0.25		ns
t <sub>pd</sub>	S	A	6		2	5.5	ns
t <sub>en</sub>	S	B	6.4		1.5	5.6	ns
	OE	A or B	6.4		1.6	5.8	
t <sub>dis</sub>	S	B	6.8		1.9	6.4	ns
	OE	A or B	6		2.3	6.2	

$^\dagger$  The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

### PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50$   $\Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - The outputs are measured one at a time with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CBT3251D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3251	<a href="#">Samples</a>
SN74CBT3251DBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI	-40 to 85		
SN74CBT3251DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU251	<a href="#">Samples</a>
SN74CBT3251DBQRG4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU251	<a href="#">Samples</a>
SN74CBT3251DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251	<a href="#">Samples</a>
SN74CBT3251DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3251	<a href="#">Samples</a>
SN74CBT3251DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBT3251	<a href="#">Samples</a>
SN74CBT3251PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251	<a href="#">Samples</a>
SN74CBT3251PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		
SN74CBT3251PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251	<a href="#">Samples</a>
SN74CBT3251PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CU251	<a href="#">Samples</a>
SN74CBT3251RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CU251	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBT3251DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74CBT3251DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBT3251PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBT3251RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBT3251DBR	SSOP	DB	16	2000	367.0	367.0	38.0
SN74CBT3251DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74CBT3251PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CBT3251RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

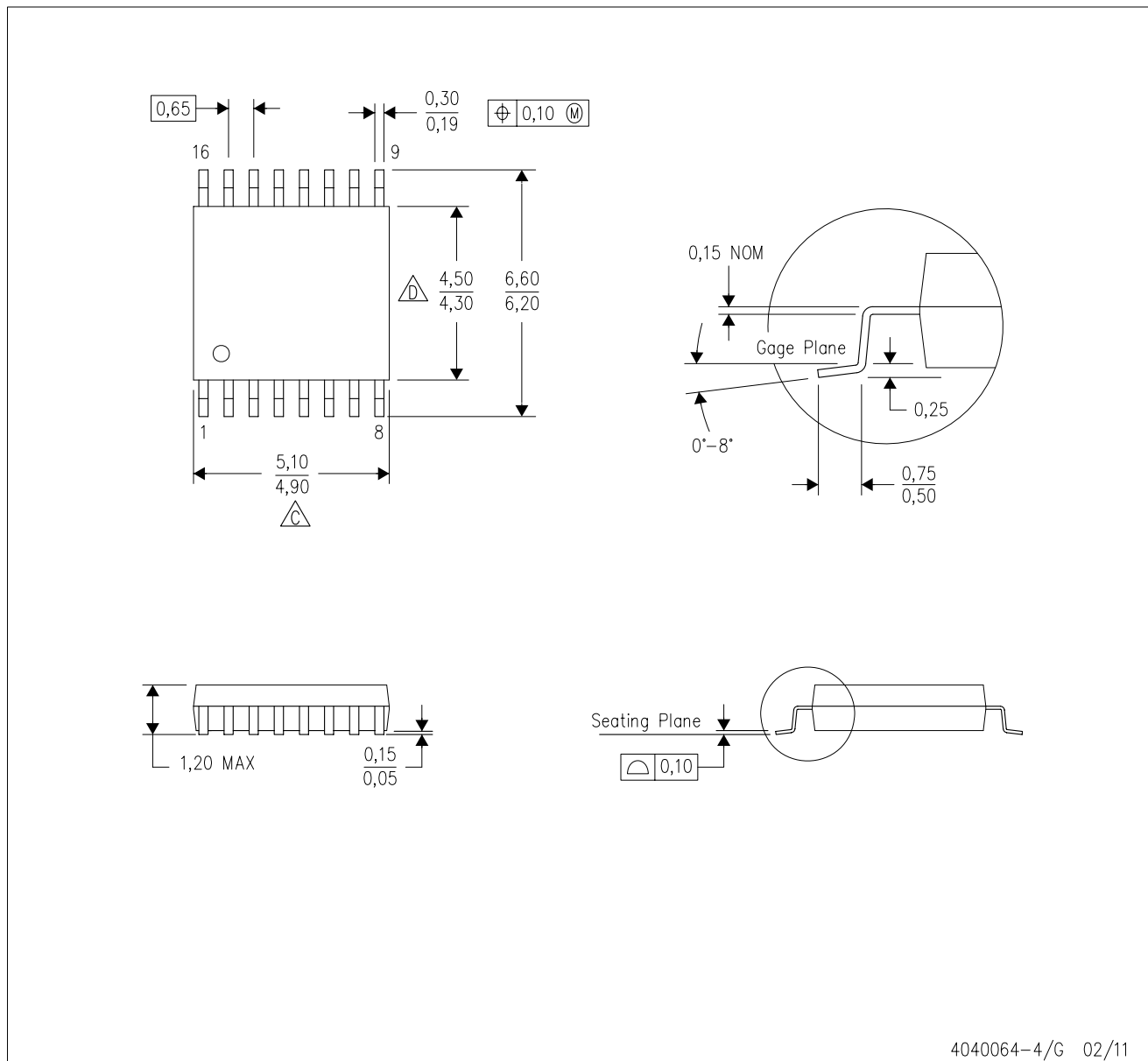
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

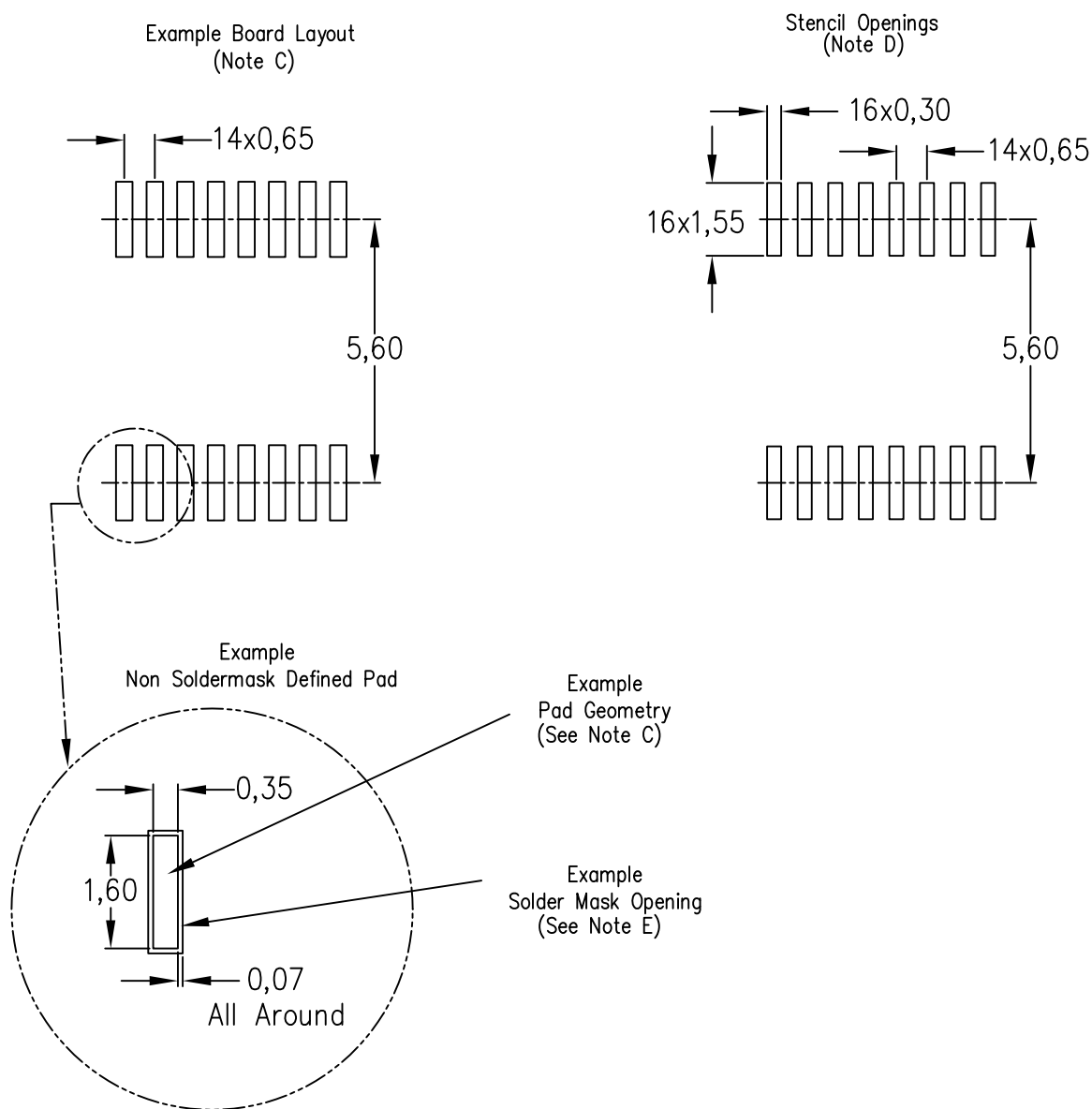
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F** Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

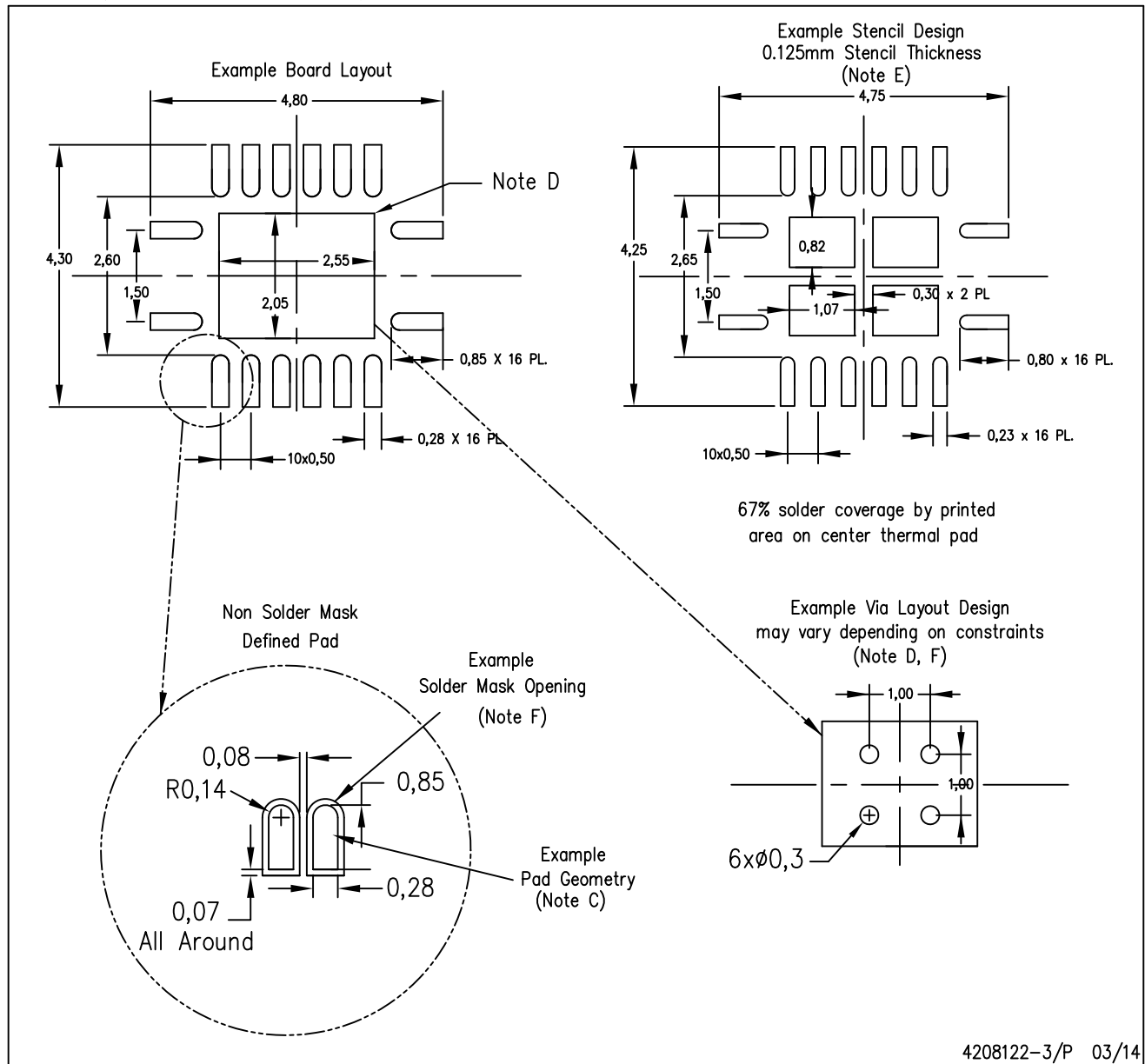
Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



DBQ (R-PDSO-G16)

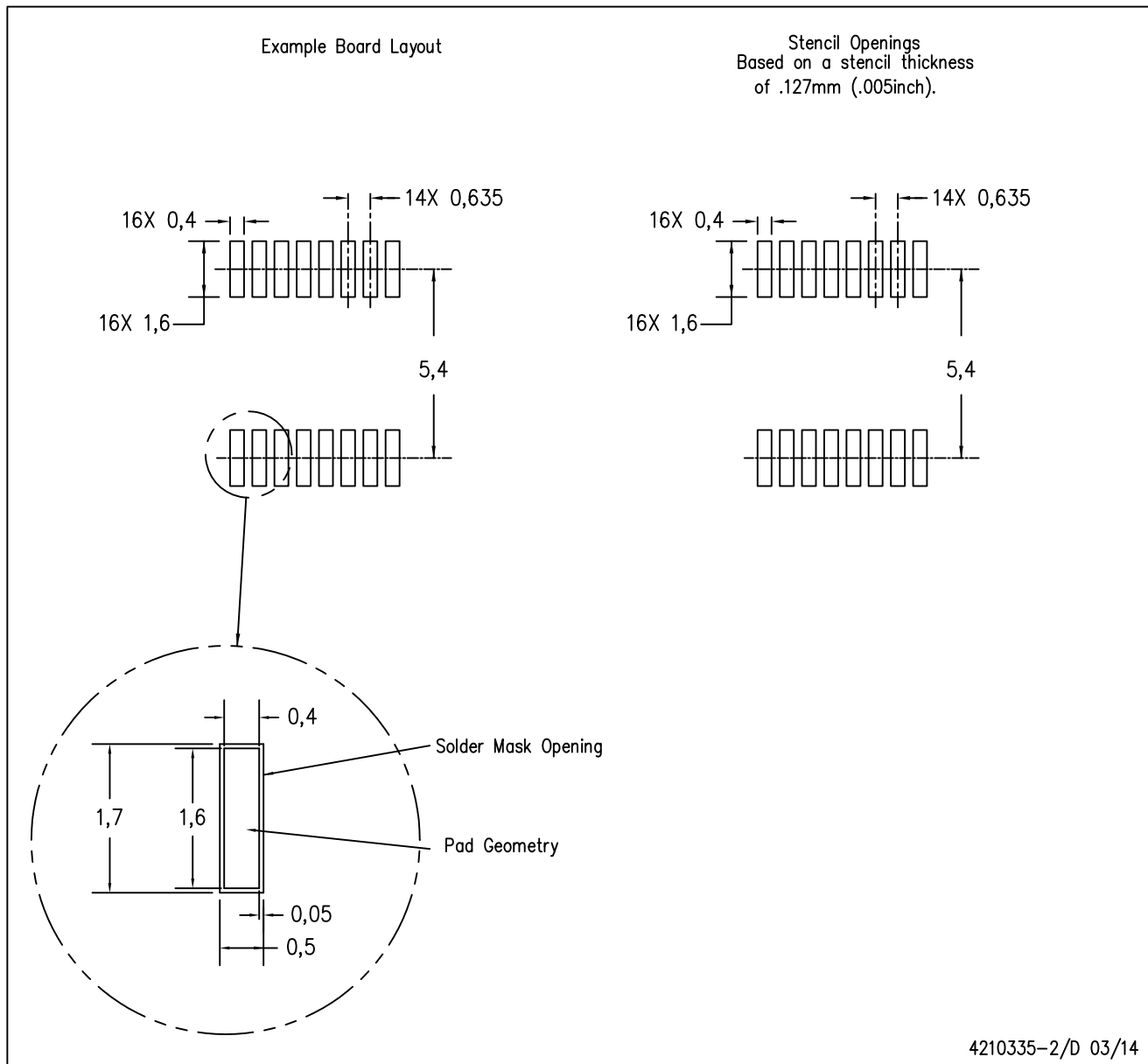
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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