

SN74CBT16232

SYNCHRONOUS 16-BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER

SCDS009M – MAY 1995 – REVISED NOVEMBER 2001

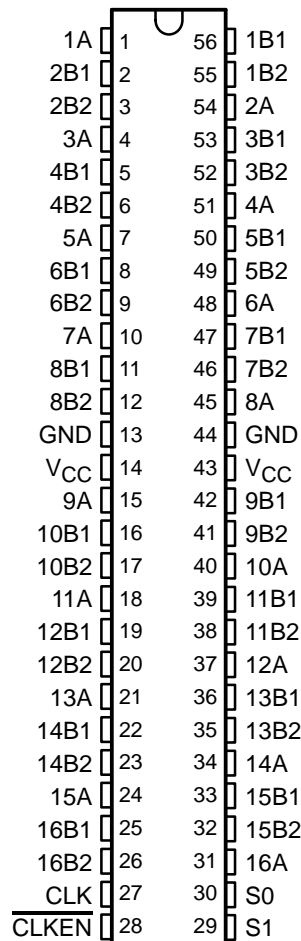
- Member of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input and Output Levels

description

The SN74CBT16232 is a synchronous 16-bit 1-of-2 FET multiplexer/demultiplexer used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single path.

Two select (S0 and S1) inputs control the data flow. A clock (CLK) and a clock enable (CLKEN) synchronize the device operation. When CLKEN is high, the bus switch remains in the last clocked function.

DGG OR DL PACKAGE (TOP VIEW)



ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74CBT16232DL	CBT16232
		Tape and reel	SN74CBT16232DLR	
	TSSOP – DGG	Tape and reel	SN74CBT16232DGGR	CBT16232

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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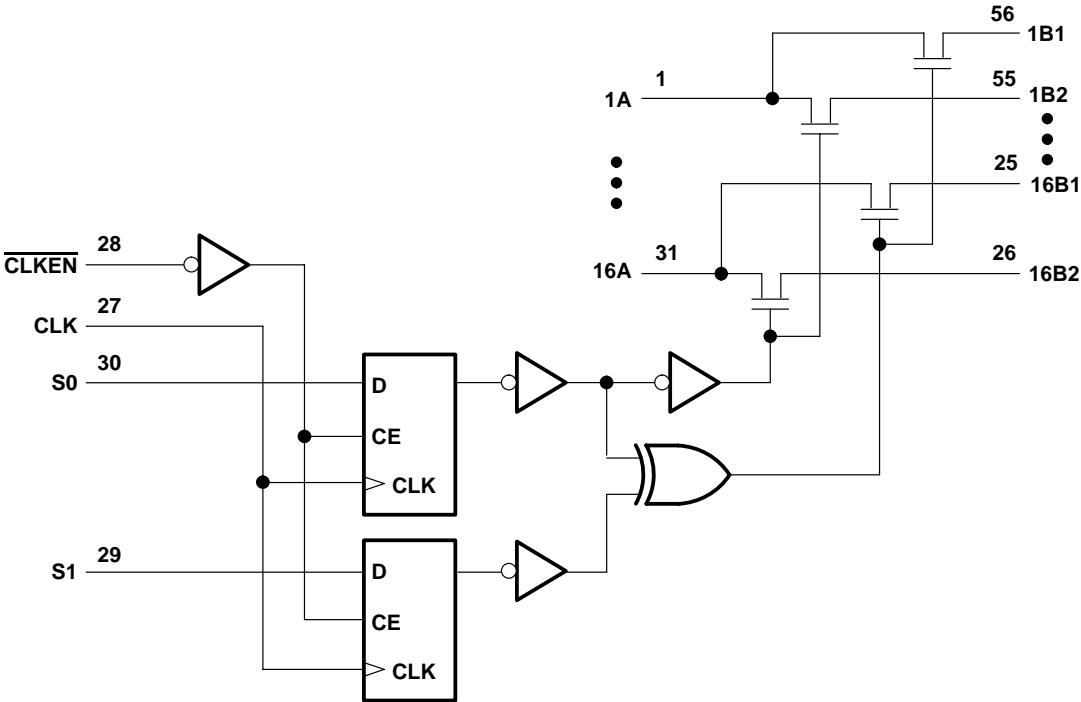
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FUNCTION TABLE				
INPUTS				FUNCTION
S1	S0	CLK	CLKEN	
X	X	X	H	Last state
L	L	↑	L	Disconnect
L	H	↑	L	A = B1 and A = B2
H	L	↑	L	A = B1
H	H	↑	L	A = B2

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	−50 mA
Package thermal impedance, θ_{JA} (see Note 2): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
V _{CC} Supply voltage	4	5.5	V
V _{IH} High-level control input voltage	2		V
V _{IL} Low-level control input voltage		0.8	V
T _A Operating free-air temperature	–40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA		–1.2		V
I _I		V _{CC} = 5.5 V, V _I = 5.5 V or GND		±1		μA
I _{CC}		V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND		3		μA
ΔI _{CC} ‡	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND		2.5		mA
C _i	Control inputs	V _I = 3 V or 0		4.5		pF
C _{io} (OFF)	A port	V _O = 3 V or 0, $\overline{\text{CLKEN}} = 0$, S0 and S1 = GND		6.5		pF
	B port			4		
r _{on} §	V _{CC} = 4 V, TYP at V _{CC} = 4 V	V _I = 2.4 V, I _I = 15 mA		14	20	Ω
		V _I = 0, I _I = 64 mA		5	7	
	V _{CC} = 4.5 V	I _I = 30 mA		5	7	
		V _I = 2.4 V, I _I = 15 mA		10	15	

† All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V _{CC} = 4 V		V _{CC} = 5 V ± 0.5 V		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		150		150	MHz
t _w	Pulse duration		CLK high or low	3.3	3.3	ns
t _{su}	Setup time		S0, S1 before CLK↑	2.2	1.9	ns
			$\overline{\text{CLKEN}}$ before CLK↑	2.4	1.9	
t _h	Hold time		S0, S1 after CLK↑	0.5	1	ns
			$\overline{\text{CLKEN}}$ after CLK↑	1.9	1.8	



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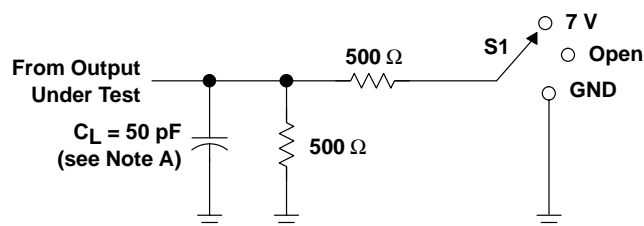
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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4$ V		$V_{CC} = 5$ V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			150		150		MHz
t_{pd}^\dagger	A or B	B or A	0.35		0.25		ns
t_{pd}	CLK	A or B	6.1		2	5.8	ns
t_{en}	CLK	A, B1, B2	6.8		1.8	6.2	ns
		B1 and B2	8.5		3.1	7.9	
t_{dis}	CLK	A or B	5.8		1.9	6.2	ns

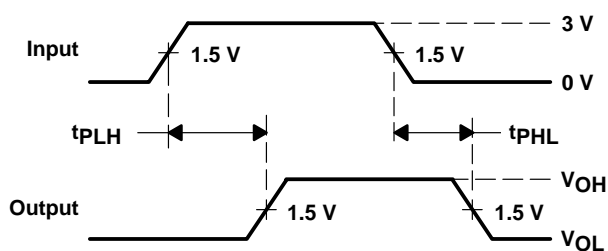
[†] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

PARAMETER MEASUREMENT INFORMATION

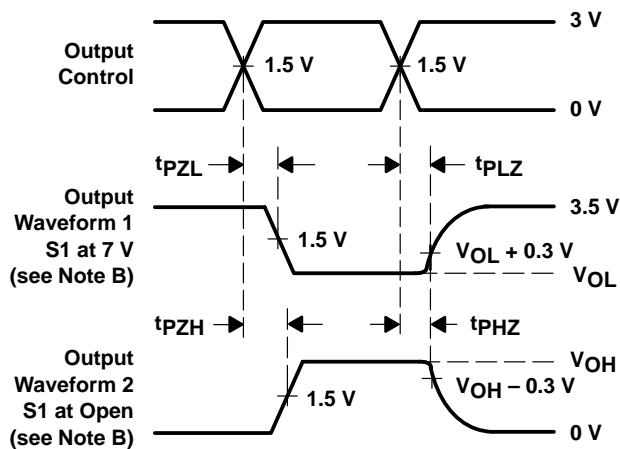


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 - The outputs are measured one at a time with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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