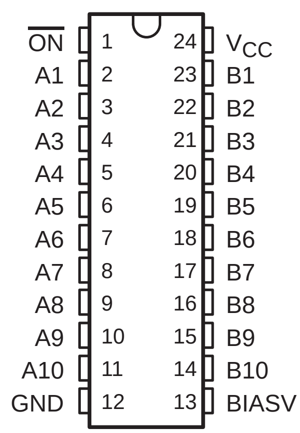
- **High-Bandwidth Data Path (Up To 500 MHz†)**
- **5-V Tolerant I/Os with Device Powered-Up or Powered-Down**
- **Low and Flat ON-State Resistance (r_{on}) Characteristics Over Operating Range (r_{on} = 4.5 Ω Typical)**
- **Rail-to-Rail Switching on Data I/O Ports**
  - **0- to 5-V Switching With 3.3-V V_{CC}**
  - **0- to 3.3-V Switching With 2.5-V V_{CC}**
- **B-Port Outputs Are Precharged by Bias Voltage (BIASV) to Minimize Signal Distortion During Live Insertion and Hot-Plugging**
- **Supports PCI Hot Plug**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low Input/Output Capacitance Minimizes Loading and Signal Distortion ($C_{io(OFF)}$ = 3.5 pF Typical)**
- **Fast Switching Frequency ($f_{\overline{ON}}$ = 20 MHz Max)**

† For additional information regarding the performance characteristics of the CB3Q family, refer to the TI application report, *CBT-C, CB3T, and CB3Q Signal-Switch Families*, literature number SCDA008.

- **Data and Control Inputs Provide Undershoot Clamp Diodes**
- **Low Power Consumption (I_{CC} = 0.75 mA Typical)**
- **V_{CC} Operating Range From 2.3 V to 3.6 V**
- **Data I/Os Support 0 to 5-V Signaling Levels (0.8-V, 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V)**
- **Control Inputs Can be Driven by TTL or 5-V/3.3-V CMOS Outputs**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Supports Both Digital and Analog Applications: PCI Interface, Differential Signal Interface, Memory Interleaving, Bus Isolation, Low-Distortion Signal Gating**

DBQ, DGV, OR PW PACKAGE
(TOP VIEW)



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description/ordering information

The SN74CB3Q6800 is a high-bandwidth FET bus switch utilizing a charge pump to elevate the gate voltage of the pass transistor, providing a low and flat ON-state resistance (r_{on}). The low and flat ON-state resistance allows for minimal propagation delay and supports rail-to-rail switching on the data input/output (I/O) ports. The device also features low data I/O capacitance to minimize capacitive loading and signal distortion on the data bus. Specifically designed to support high-bandwidth applications, the SN74CB3Q6800 provides an optimized interface solution ideally suited for broadband communications, networking, and data-intensive computing systems.

The SN74CB3Q6800 is a 10-bit bus switch with a single output-enable ($\overline{ON}$) input. When $\overline{ON}$ is low, the 10-bit bus switch is ON and the A port is connected to the B port, allowing bidirectional data flow between ports. When $\overline{ON}$ is high, the 10-bit bus switch is OFF and a high-impedance state exists between the A and B ports. The B port is precharged to bias voltage (BIASV) through the equivalent of a 10-kΩ resistor when $\overline{ON}$ is high, or if the device is powered down (V_{CC} = 0 V).

During insertion (or removal) of a card into (or from) an active bus, the card's output voltage may be close to GND. When the connector pins make contact, the card's parasitic capacitance tries to force the bus signal to GND, creating a possible glitch on the active bus. This glitching effect can be reduced by using a bus switch with precharged bias voltage (BIASV) of the bus switch equal to the input threshold voltage level of the receivers on the active bus. This method will ensure that any glitch produced by insertion (or removal) of the card will not cross the input threshold region of the receivers on the active bus, minimizing the effects of live-insertion noise.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry prevents damaging current backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{ON}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

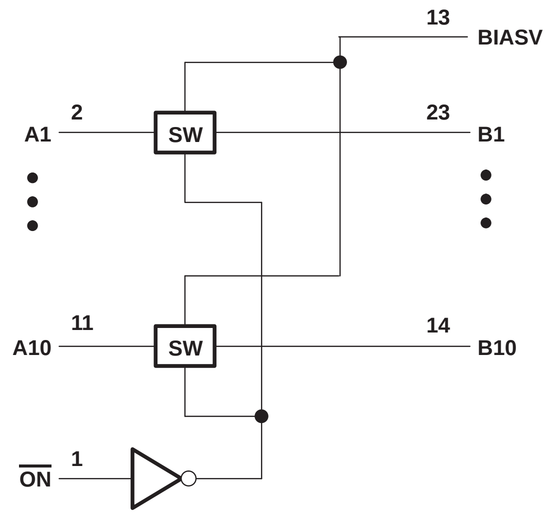
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP (QSOP) − DBQ	Tape and reel	SN74CB3Q6800DBQR	CB3Q6800
	TSSOP − PW	Tube	SN74CB3Q6800PW	BY800
		Tape and reel	SN74CB3Q6800PWR	
	TVSOP − DGV	Tape and reel	SN74CB3Q6800DGVR	BY800

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

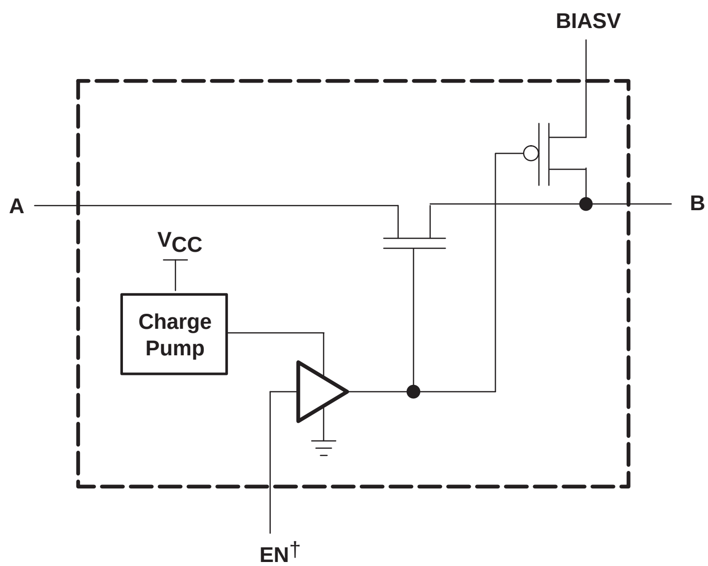
FUNCTION TABLE

INPUT $\overline{ON}$	INPUT/OUTPUT A	FUNCTION
L	B	A port = B port
H	Z	Disconnect B port = BIASV

logic diagram (positive logic)



simplified schematic, each FET switch (SW)



† EN is the internal enable signal applied to the switch.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V
BIAS supply voltage range, BIASV . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0) . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . ±64 mA
Continuous current through V_{CC} or GND terminals . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): DBQ package . . . . 61°C/W
DGV package . . . . 86°C/W
PW package . . . . 88°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltages are with respect to ground unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 6)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
BIASV	Bias supply voltage		0	5	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	5.5	V
		V_{CC} = 2.7 V to 3.6 V	2	5.5	
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V	0	0.7	V
		V_{CC} = 2.7 V to 3.6 V	0	0.8	
$V_{I/O}$	Data input/output voltage		0	5.5	V
T_A	Operating free-air temperature		−40	85	°C

NOTE 6: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004. BIASV is a supply voltage, not a control input.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 3.6 V,	I_I = −18 mA				−1.8	V
I_{IN}	Control inputs	V_{CC} = 3.6 V,	V_{IN} = 0 to 5.5 V				±1	μA
I_O	B port	V_{CC} = 3.V,	BIASV = 2.4 V, V_O = 0,	Switch OFF, V_{IN} = V_{CC} or GND		0.2		mA
I_{OZ}‡		V_{CC} = 3.6 V,	V_O = 0 to 5.5 V, V_I = 0,	Switch OFF, V_{IN} = V_{CC} or GND			±1	μA
I_{off}		V_{CC} = 0,	V_O = 0 to 5.5 V,	V_I = 0			1	μA
I_{CC}		V_{CC} = 3.6 V,	$I_{I/O}$ = 0, Switch ON or OFF,	V_{IN} = V_{CC} or GND		0.75	2	mA
ΔI_{CC}§	Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND			30	μA
I_{CCD}¶	Per control input	V_{CC} = 3.6 V, Control input switching at 50% duty cycle	A and B ports open,			0.38	0.45	mA/MHz
C_{in}	Control inputs	V_{CC} = 3.3 V,	V_{IN} = 5.5 V, 3.3 V, or 0			2.5	3.5	pF
$C_{io(OFF)}$	A port	V_{CC} = 3.3 V,	Switch OFF, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		3.5	5	pF
$C_{io(ON)}$		V_{CC} = 3.3 V,	Switch ON, V_{IN} = V_{CC} or GND,	$V_{I/O}$ = 5.5 V, 3.3 V, or 0		9	11	pF
r_{on}#		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0,	I_O = 30 mA		4.5	8	Ω
			V_I = 1.7 V,	I_O = −15 mA		4.8	9	
		V_{CC} = 3 V	V_I = 0,	I_O = 30 mA		4.5	6	
			V_I = 2.4 V,	I_O = −15 mA		4.6	8	

V_{IN} and I_{IN} refer to control inputs. V_I, V_O, I_I, and I_O refer to data pins.
† All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
¶ This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see Figure 2).
# Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	TEST CONDITIONS	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	
$f_{\overline{ON}}$‖		$\overline{ON}$	A or B		10		20	MHz
t_{pd}☆		A or B	B or A		0.135		0.225	ns
t_{PZH}	BIASV = GND	$\overline{ON}$	A or B	1.5	8.5	1.5	6.7	ns
t_{PZL}	BIASV = 3 V			1.5	8.5	1.5	6.7	
t_{PHZ}	BIASV = GND	$\overline{ON}$	A or B	1	5	1	5	ns
t_{PLZ}	BIASV = 3 V			1	6.9	1	6.9	

‖ Maximum switching frequency for control input (V_O > V_{CC}, V_I = 5 V, R_L ≥ 1 MΩ, C_L = 0).
☆ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

TYPICAL r_{on}
vs
V_I

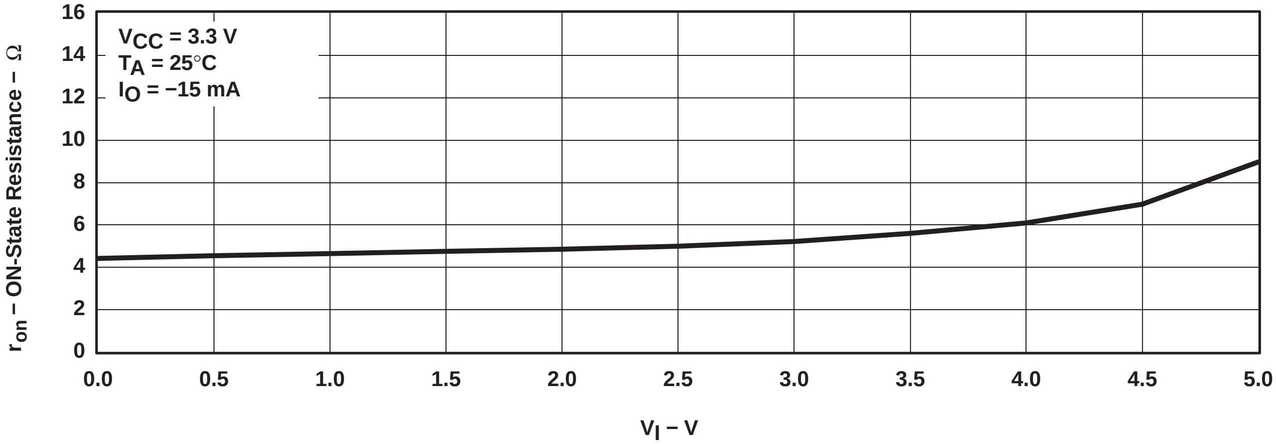


Figure 1. Typical r_{on} vs V_I, V_{CC} = 3.3 V and I_O = −15 mA

TYPICAL I_{CC}
vs
$\overline{\text{ON}}$ SWITCHING FREQUENCY

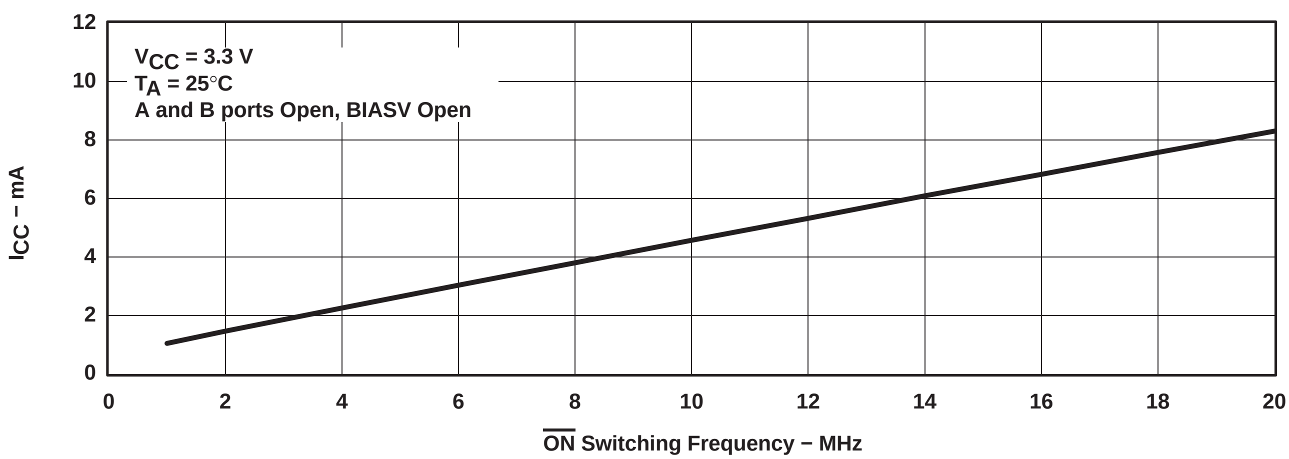
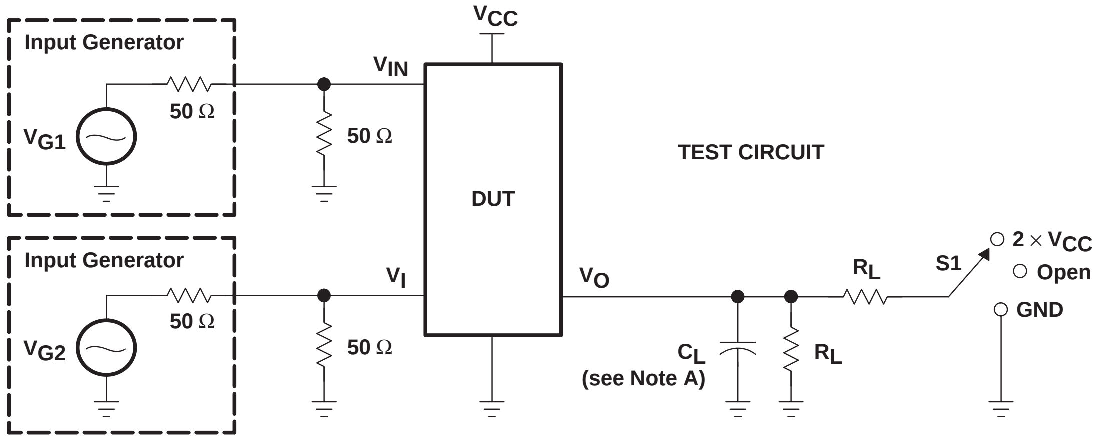
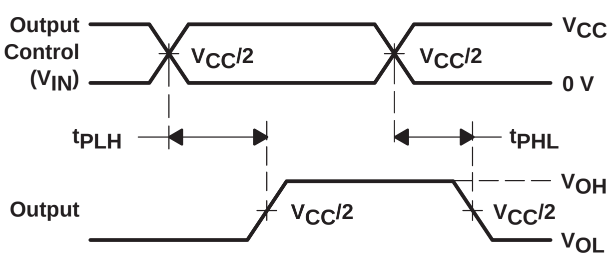


Figure 2. Typical I_{CC} vs $\overline{\text{ON}}$ Switching Frequency, V_{CC} = 3.3 V

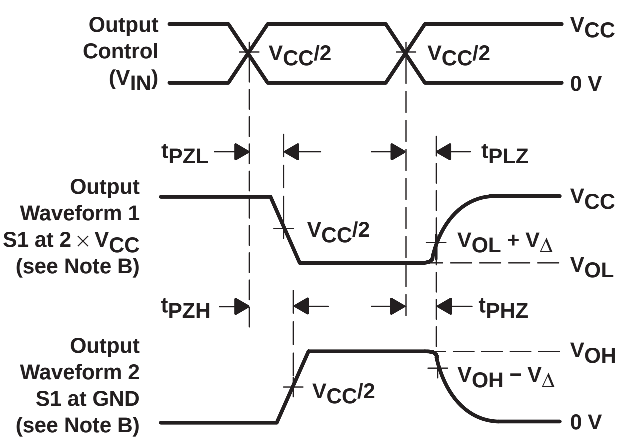
PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	S1	R_L	V_I	C_L	V_Δ
$t_{pd(s)}$	2.5 V ± 0.2 V 3.3 V ± 0.3 V	Open Open	500 Ω 500 Ω	V_{CC} or GND V_{CC} or GND	30 pF 50 pF	
t_{PLZ}/t_{PZL}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	2 × V_{CC} 2 × V_{CC}	500 Ω 500 Ω	GND GND	30 pF 50 pF	0.15 V 0.3 V
t_{PHZ}/t_{PZH}	2.5 V ± 0.2 V 3.3 V ± 0.3 V	GND GND	500 Ω 500 Ω	V_{CC} V_{CC}	30 pF 50 pF	0.15 V 0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES ($t_{pd(s)}$)



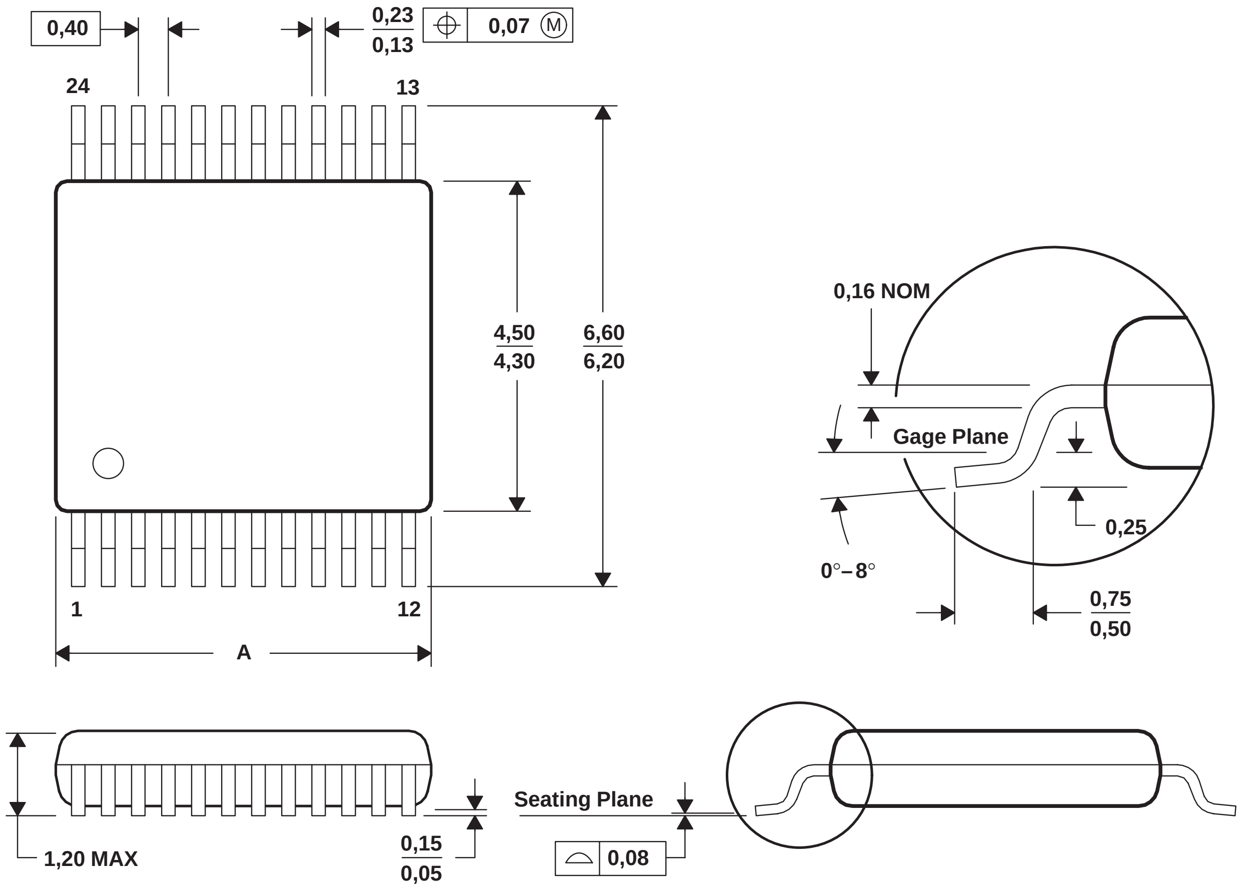
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as $t_{pd(s)}$. The tpd propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Test Circuit and Voltage Waveforms

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

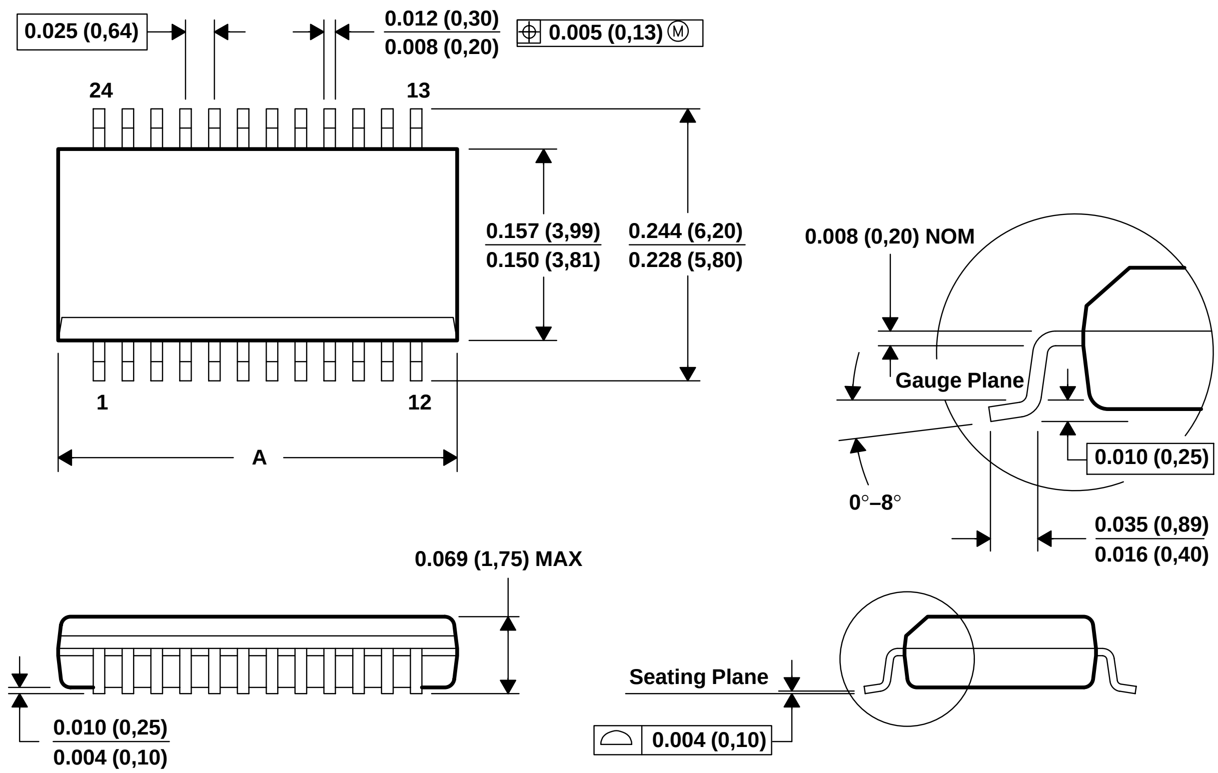


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DBQ (R–PDSO–G)** **PLASTIC SMALL–OUTLINE PACKAGE**



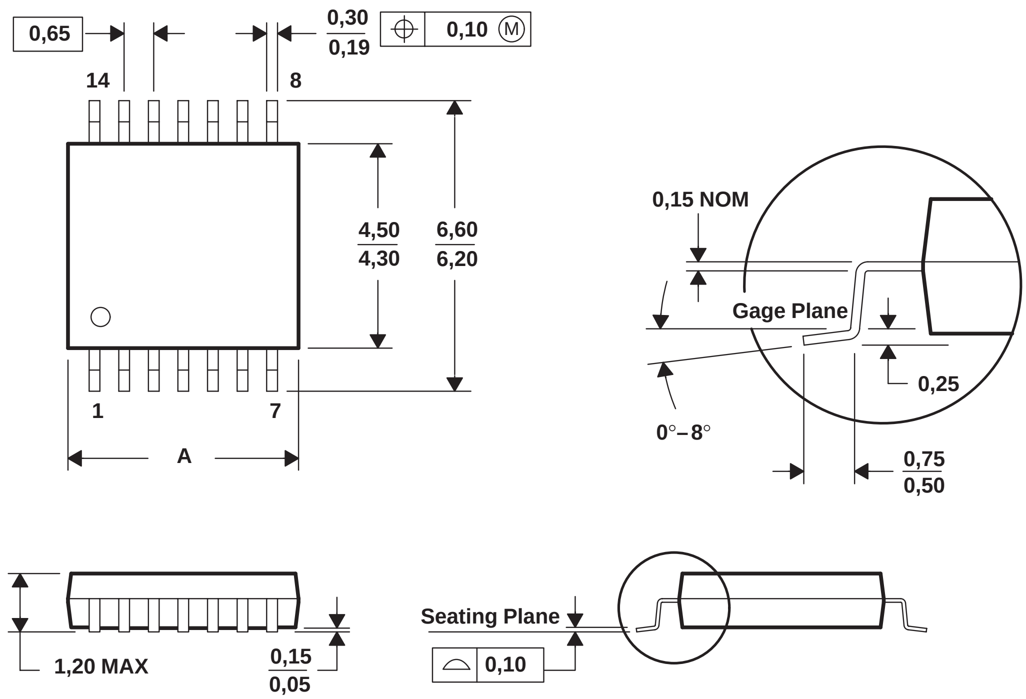
PINS ** / DIM	16	20	24	28
A MAX	0.197 (5,00)	0.344 (8,74)	0.344 (8,74)	0.394 (10,01)
A MIN	0.189 (4,80)	0.337 (8,56)	0.337 (8,56)	0.386 (9,80)
D M0–137 VARIATION	AB	AD	AE	AF

4073301/F 02/02

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–137.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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