SN54BCT543, SN74BCT543
OCTAL REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

SCBS026C – NOVEMBER 1988 – REVISED APRIL 1994

- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **3-State True Outputs**
- **Back-to-Back Registers for Storage**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic Small-Outline Packages (DW), Ceramic Chip Carriers (FK) and Flatpacks (W), and Plastic and Ceramic 300-mil DIPs (JT, NT)**
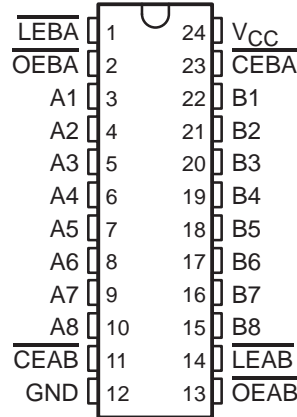
description

The ′BCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.
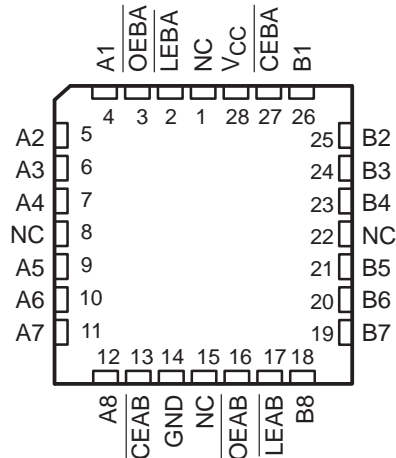
The A-to-B enable ($\overline{CEAB}$) input must be low in order to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

The SN54BCT543 is characterized for operation over the full military temperature range of $-55°C$ to $125°C$. The SN74BCT543 is characterized for operation from $0°C$ to $70°C$.

SN54BCT543 . . . JT OR W PACKAGE
SN74BCT543 . . . DW OR NT PACKAGE
(TOP VIEW)

$\overline{LEBA}$	1	24	V_{CC}
$\overline{OEBA}$	2	23	$\overline{CEBA}$
A1	3	22	B1
A2	4	21	B2
A3	5	20	B3
A4	6	19	B4
A5	7	18	B5
A6	8	17	B6
A7	9	16	B7
A8	10	15	B8
$\overline{CEAB}$	11	14	$\overline{LEAB}$
GND	12	13	$\overline{OEAB}$

SN54BCT543 . . . FK PACKAGE
(TOP VIEW)

NC – No internal connection

FUNCTION TABLE[†]

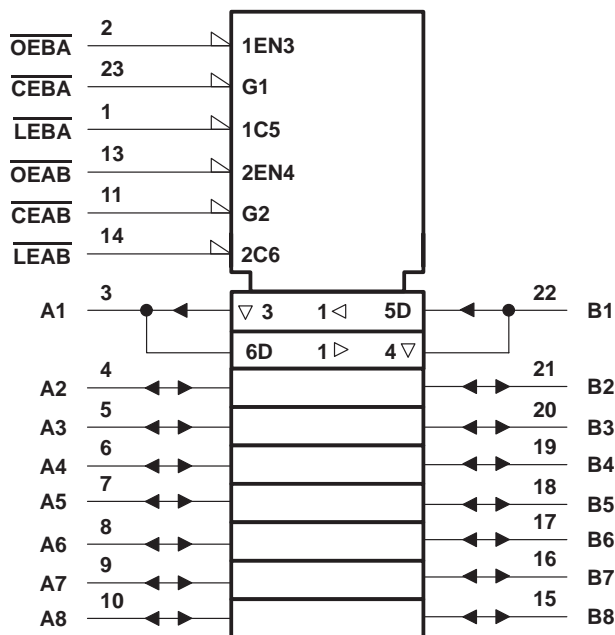| INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0[‡]
L	L	L	L	L
L	L	L	H	H

[†] A-to-B data flow is shown; B-to-A flow control is the same except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

[‡] Output level before the indicated steady-state input conditions were established.

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logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

To Seven Other Channels
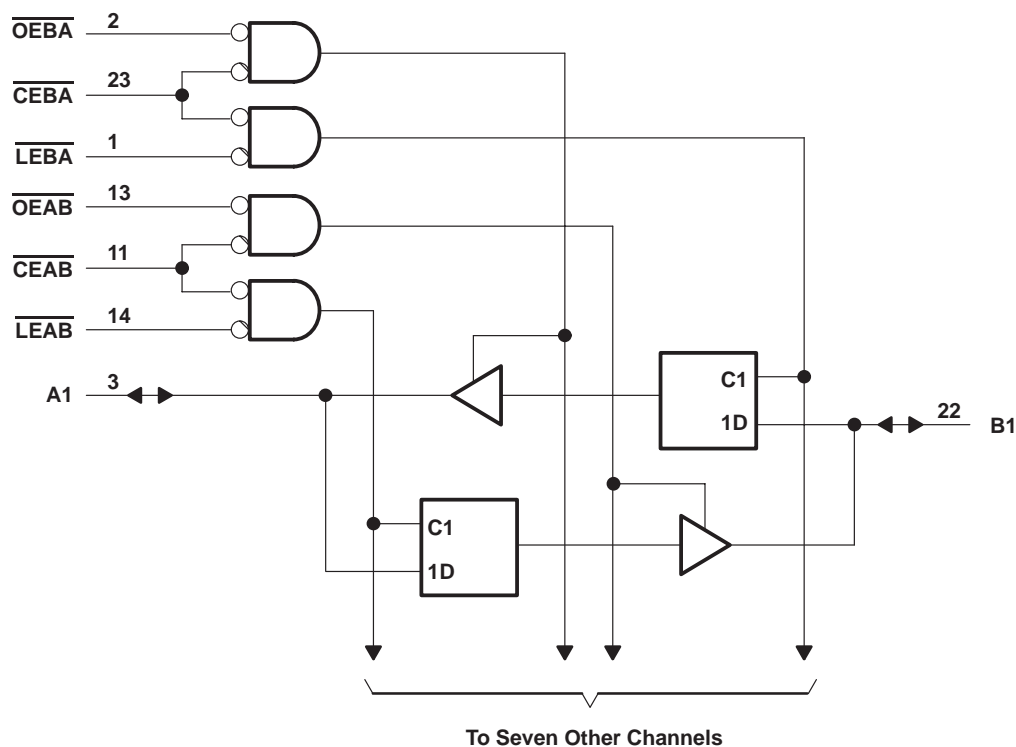
Pin numbers shown are for the DW, JT, NT, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range: Control inputs (see Note 1)	-0.5 V to 7 V
I/O ports (see Note 1)	-0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O	-0.5 V to 7 V
Voltage range applied to any output in the high state, V_O	-0.5 V to V_{CC}
Input clamp current, I_{IK}	-30 mA
Current into any output in the low state: SN54BCT543	96 mA
SN74BCT543	128 mA
Operating free-air temperature range: SN54BCT543	$-55°C$ to $125°C$
SN74BCT543	$0°C$ to $70°C$
Storage temperature range	$-65°C$ to $150°C$

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:   The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT543			SN74BCT543			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-12			-15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54BCT543 MIN	SN54BCT543 TYP†	SN54BCT543 MAX	SN74BCT543 MIN	SN74BCT543 TYP†	SN74BCT543 MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V	I_{OH} = −3 mA	2.4	3.3		2.4	3.3		V
			I_{OH} = −12 mA	2	3.2					
			I_{OH} = −15 mA				2	3.1		
V_{OL}		V_{CC} = 4.5 V	I_{OL} = 48 mA		0.38	0.55				V
			I_{OL} = 64 mA					0.42	0.55	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			0.4			0.4	mA
I_{IH}‡	A or B port	V_{CC} = 5.5 V,	V_I = 2.7 V			70			70	µA
	Control input					20			20	
I_{IL}‡	A or B port	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.65			−0.65	mA
	Control input					−0.6			−0.6	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0	−100		−225	−100		−225	mA
I_{CCL}	A or B port	V_{CC} = 5.5 V			45	71		45	71	mA
I_{CCH}	A or B port	V_{CC} = 5.5 V			5	8		5	8	mA
I_{CCZ}	A or B port	V_{CC} = 5.5 V			9	15		9	15	mA
C_i	Control input	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6			6		pF
C_{io}	A or B port	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		16			16		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C MIN	V_{CC} = 5 V, T_A = 25°C MAX	SN54BCT543 MIN	SN54BCT543 MAX	SN74BCT543 MIN	SN74BCT543 MAX	UNIT
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low		7		8		7		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$↑	High or low	4.5		5.5		4.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$↑	High or low	1.5		1.5		1.5		ns

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switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX[†]				UNIT
			′BCT543			SN54BCT543		SN74BCT543		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	5.7	7.5	2	9.9	2	8.8	ns
t_{PHL}	A or B	B or A	2	6.3	8.2	2	9.7	2	9.6	ns
t_{PLH}	$\overline{LE}$	A or B	2	8.2	10.3	2	13.9	2	12.9	ns
t_{PHL}	$\overline{LE}$	A or B	2	8.5	10.6	2	13.2	2	12.7	ns
t_{PZH}	$\overline{OE}$	A or B	1	6.8	8.6	1	11.4	1	10.7	ns
t_{PZL}	$\overline{OE}$	A or B	1	8.7	10.8	1	12.8	1	12.3	ns
t_{PHZ}	$\overline{OE}$	A or B	1	5.5	7.2	1	8.8	1	8.1	ns
t_{PLZ}	$\overline{OE}$	A or B	1	4.7	6.4	1	8.1	1	7.2	ns
t_{PZH}	$\overline{CE}$	A or B	1	7.6	9.8	1	12.8	1	12	ns
t_{PZL}	$\overline{CE}$	A or B	1	9.5	11.6	1	13.8	1	13.5	ns
t_{PHZ}	CE	A or B	1	5.8	7.5	1	9.3	1	8.5	ns
t_{PLZ}	CE	A or B	1	4.8	6.7	1	8.4	1	7.6	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
NOTE 2:   Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9087001M3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9087001MKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type
5962-9087001MLA	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SN74BCT543DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT543DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT543DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT543DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT543DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT543DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT543NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74BCT543NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54BCT543FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54BCT543JT	ACTIVE	CDIP	JT	24	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54BCT543W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74BCT543DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS
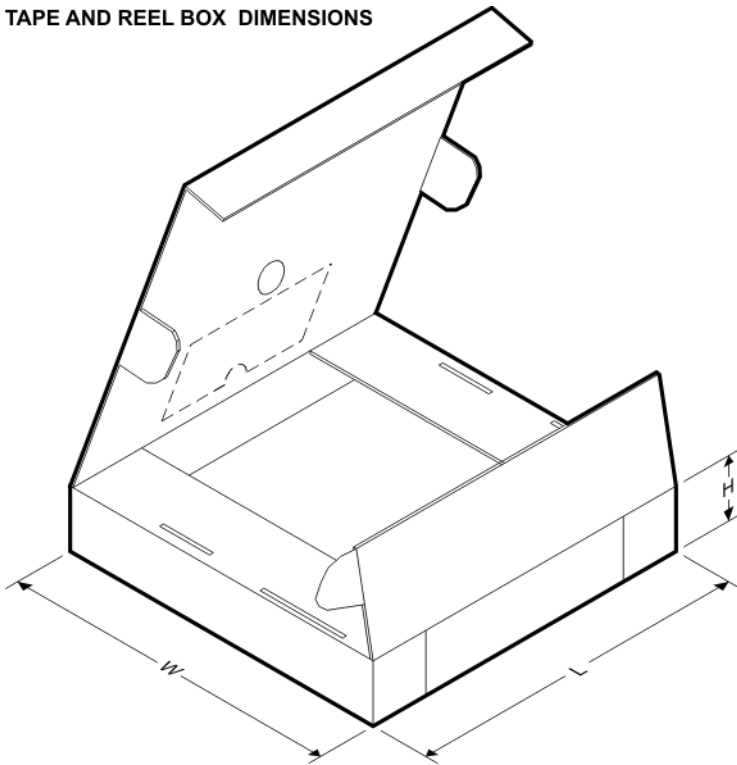
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74BCT543DWR	SOIC	DW	24	2000	346.0	346.0	41.0

FK (S-CQCC-N**)   LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

0.020 (0,51) / 0.010 (0,25)

0.020 (0,51) / 0.010 (0,25)

0.080 (2,03) / 0.064 (1,63)

0.055 (1,40) / 0.045 (1,14)

0.045 (1,14) / 0.035 (0,89)

0.028 (0,71) / 0.022 (0,54)

0.045 (1,14) / 0.035 (0,89)

0.050 (1,27)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package can be hermetically sealed with a metal lid.
        D. The terminals are gold plated.
        E. Falls within JEDEC MS-004

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN
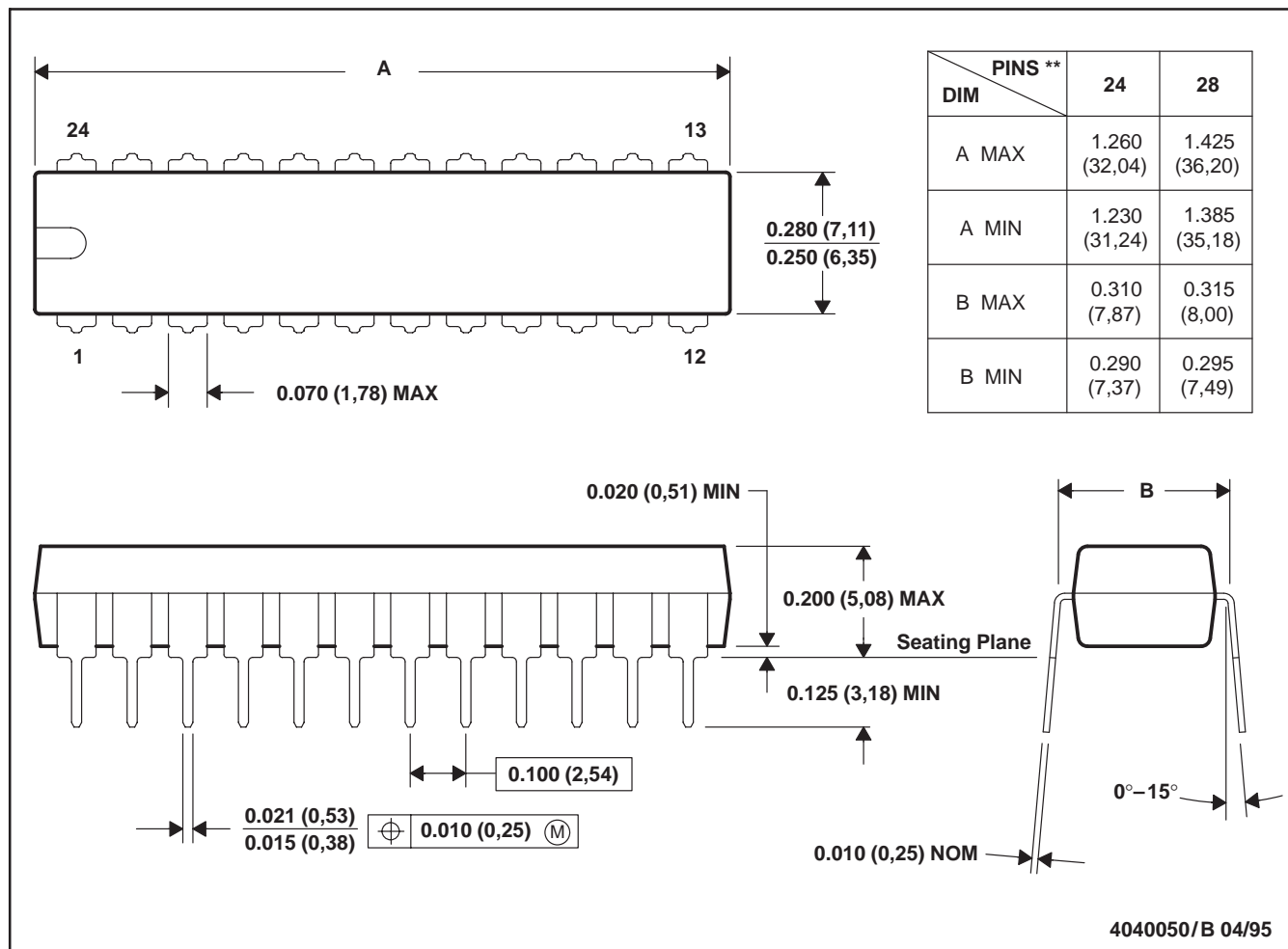
PINS ** DIM	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

A

24   13

0.280 (7,11)
0.250 (6,35)

1   12

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

B

0°–15°

0.021 (0,53)
0.015 (0,38)   ⊕ | 0.010 (0,25) Ⓜ

0.010 (0,25) NOM

4040050/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.

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W (R-GDFP-F24)   **CERAMIC DUAL FLATPACK**
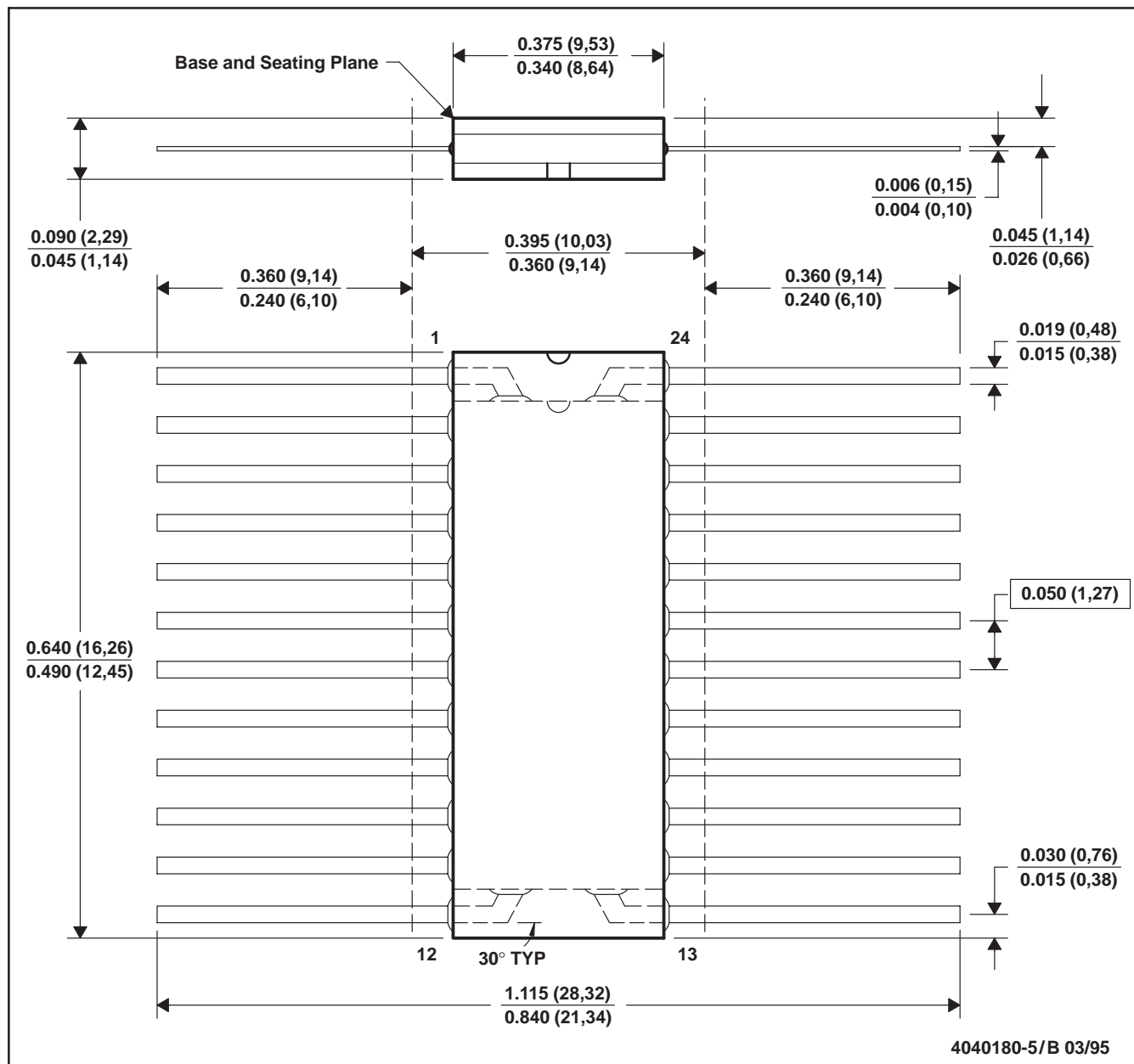
Base and Seating Plane

$\dfrac{0.375\ (9,53)}{0.340\ (8,64)}$

$\dfrac{0.006\ (0,15)}{0.004\ (0,10)}$

$\dfrac{0.090\ (2,29)}{0.045\ (1,14)}$

$\dfrac{0.395\ (10,03)}{0.360\ (9,14)}$

$\dfrac{0.045\ (1,14)}{0.026\ (0,66)}$

$\dfrac{0.360\ (9,14)}{0.240\ (6,10)}$

$\dfrac{0.360\ (9,14)}{0.240\ (6,10)}$

$\dfrac{0.019\ (0,48)}{0.015\ (0,38)}$

1   24

$\dfrac{0.640\ (16,26)}{0.490\ (12,45)}$

0.050 (1,27)

$\dfrac{0.030\ (0,76)}{0.015\ (0,38)}$

12   30° TYP   13

$\dfrac{1.115\ (28,32)}{0.840\ (21,34)}$

4040180-5 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
       B. This drawing is subject to change without notice.
       C. This package can be hermetically sealed with a ceramic lid using glass frit.
       D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
       E. Index point is provided on cap for terminal identification only.

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DW (R−PDSO−G24) PLASTIC SMALL−OUTLINE PACKAGE

0.614 (15,60) / 0.598 (15,20)

24 13

0.419 (10,63) / 0.393 (9,97)

0.299 (7,60) / 0.291 (7,40)

1 12

Pin 1 Index Area

0.050 (1,27)

0.020 (0,51) / 0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30) / 0.004 (0,10)

0.013 (0,33) / 0.008 (0,20)

Gauge Plane

⌂ 0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27) / 0.016 (0,40)

4040000−5/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS−013 variation AD.

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN
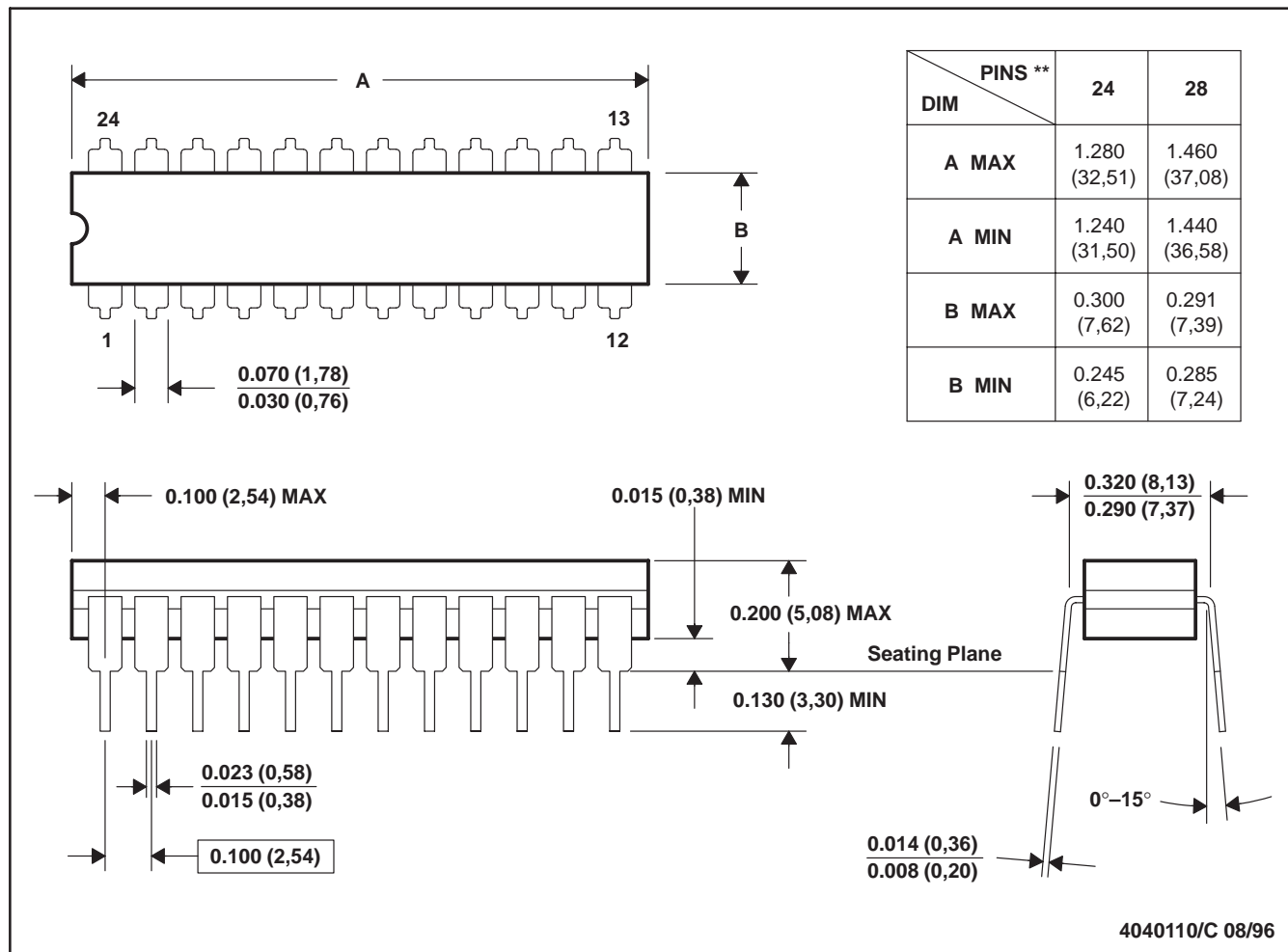
PINS ** DIM	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

0.070 (1,78)
0.030 (0,76)

0.100 (2,54) MAX

0.015 (0,38) MIN

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.023 (0,58)
0.015 (0,38)

0.100 (2,54)

0.320 (8,13)
0.290 (7,37)

0°–15°

0.014 (0,36)
0.008 (0,20)

4040110/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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