SCBS035D - SEPTEMBER 1988 - REVISED MARCH 2003

 Operating Voltage Range of 4.5 V to 5.5 V State-of-the-Art BiCMOS Design 	DW, N OR NS PACKAGE (TOP VIEW)
Significantly Reduces I _{CCZ}	10E [1 20] V _{CC}
 Output Ports Have Equivalent 33-Ω Series 	1A1 2 19 2OE
Resistors, So No External Resistors Are	2Y4 [3 18] 1Y1
Required	1A2 [] 4
 3-State Outputs Drive Bus Lines or Buffer 	2Y3 [5 16] 1Y2
Memory Address Registers	1A3 [] 6 15 [] 2A3
 ESD Protection Exceeds JESD 22 	2Y2 [] 7 14] 1Y3
- 2000-V Human-Body Model (A114-A)	1A4 [] 8 13 [] 2A2
, , ,	2Y1 🛛 9 12 🗍 1Y4
scription/ordering information	GND [] 10 11 [] 2A1

This SN74BCT2241 is designed specifically to improve both the performance and density of

3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'BCT2240 and 'BCT2244 devices, this device provides the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable (\overline{OE}) inputs, and complementary \overline{OE} inputs. This device features high fan-out and improved fan-in.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The outputs, which are designed to source or sink up to 12 mA, include 33- Ω series resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74BCT2241N	SN74BCT2241N
0°C to 70°C	0010 5111	Tube	SN74BCT2241DW	DOT0044
	SOIC - DW	Tape and reel	SN74BCT2241DWR	BCT2241
	SOP - NS	Tape and reel	SN74BCT2241NSR	BCT2241

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLES

INPL	JTS	OUTPUT
1OE	1 A	1Y
L	Н	Н
L	L	L
Н	Χ	Z

INP	JTS	OUTPUT
20E	2A	2Y
Н	Н	Н
Н	L	L
L	X	Z

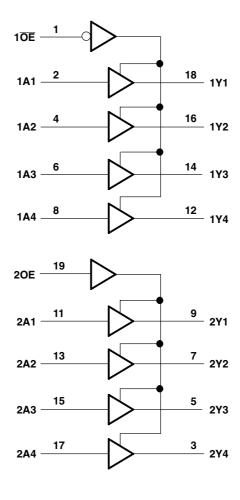


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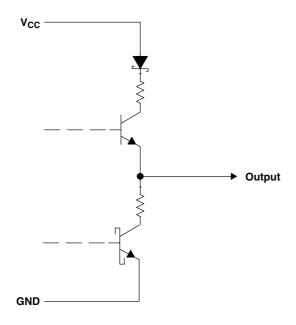


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logic diagram (positive logic)



schematic of Y outputs





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	-0.5	V to $7\ V$
Input voltage range, V _I (see Note 1)	-0.5	V to 7 V
Voltage range applied to any output in the disabled or power-off state, V _O	-0.5 V	to 5.5 V
Voltage range applied to any output in the high state, V _O	-0.5	V to V _{CC}
Input clamp current, I _{IK}		
Current into any output in the low state, I _O		. 24 mA
Package thermal impedance, θ _{JA} (see Note 2): DW package		58°C/W
N package		69°C/W
NS package		60°C/W
Storage temperature range, T _{sto} –	65°C t	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			8.0	V
I _{IK}	Input clamp current			-18	mA
I _{OH}	High-level output current			-12	mA
I _{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

SN74BCT2241 OCTAL BUFFER AND LINE/MOS DRIVER WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.5 V,$	I _I = −18 mA			-1.2	V
	V 45V	$I_{OH} = -1 \text{ mA}$	2.4	3.3		
V _{OH}	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -12 \text{ mA}$	2			V
	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -3 \text{ mA}$	2.7			
V	V 45V	I _{OL} = 1 mA		0.15	0.5	V
V _{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$		0.42	0.8	V
I _I	$V_{CC} = 5.5 V$,	V _I = 7 V			0.1	mA
I _{IH}	$V_{CC} = 5.5 V$,	V _I = 2.7 V			20	μΑ
I _{IL}	$V_{CC} = 5.5 V$,	V _I = 0.5 V			-1	mA
I _{OZH}	$V_{CC} = 5.5 V,$	$V_0 = 2.7 \text{ V}$			50	μΑ
I _{OZL}	$V_{CC} = 5.5 V$,	$V_{O} = 0.5 \text{ V}$			-50	μΑ
I _{OS} ‡	$V_{CC} = 5.5 V$,	V _O = 0	-100		-225	mA
Іссн	$V_{CC} = 5.5 V,$	Outputs open		23	37	mA
I _{CCL}	$V_{CC} = 5.5 V,$	Outputs open		48	76	mA
I _{CCZ}	$V_{CC} = 5.5 V,$	Outputs open		6	9	mA
C _i	$V_{CC} = 5 V$,	$V_1 = 2.5 \text{ V or } 0.5 \text{ V}$		6		pF
Co	$V_{CC} = 5 V$,	$V_0 = 2.5 \text{ V or } 0.5 \text{ V}$		11		pF

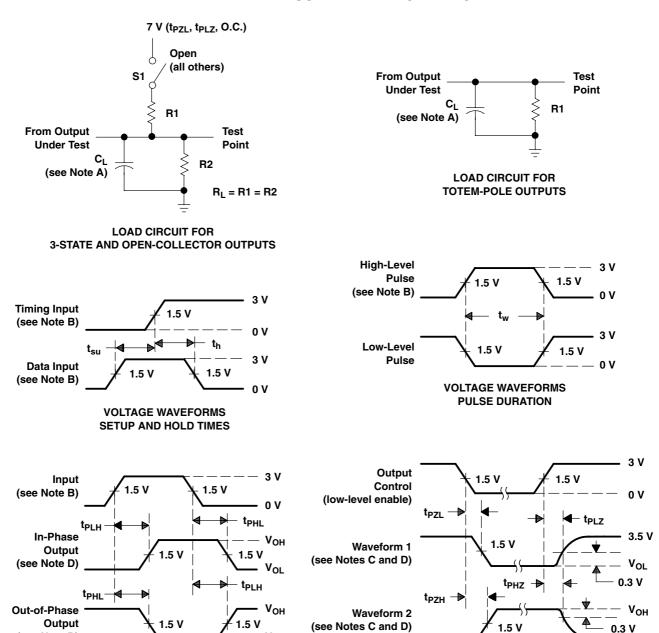
 $[\]dagger$ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO	V _{CC} = 5 V, T _A = 25°C			MIN	MAX	UNIT
	(INPUT)	(OUTPUT)	MIN	TYP	MAX			
t _{PLH}		V	1.1	3	4.4	1.1	4.9	
t _{PHL}	А	Y	2.9	4.9	6.6	2.9	6.9	ns
t _{PZH}	0F *** 0 F	V	2.7	6	7.8	2.7	8.9	
t _{PZL}	OE or OE	Y	4.1	7.7	9.4	4.1	10.3	ns
t _{PHZ}	0F or 0F	v	2.5	5.2	7.2	2.5	8.7	ns
t _{PLZ}	OE or OE	I	3.2	7.1	9.5	3.2	11.3	115

[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES (see Note D)

VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_I includes probe and jig capacitance.

(see Note D)

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $t_f = t_f \leq$ 2.5 ns, duty cycle = 50%.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

 v_{ol}

- E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
- F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



0 V

PACKAGE OPTION ADDENDUM

www.ti.com 11-Nov-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins I	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74BCT2241DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2241DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74BCT2241DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



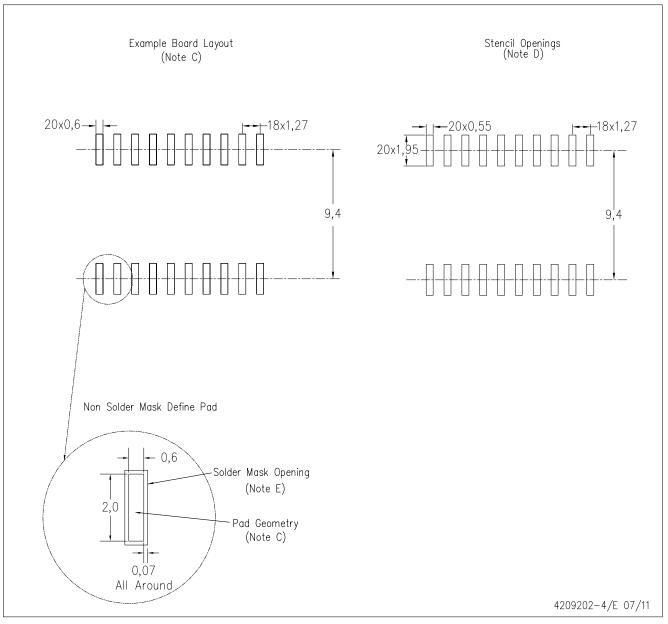
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC—7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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