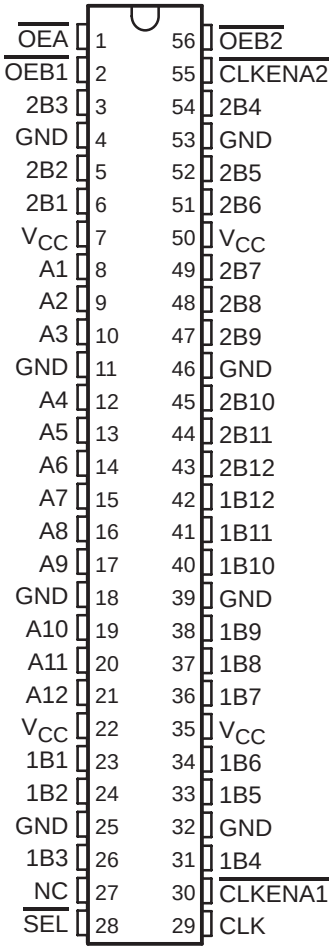
- **Member of the Texas Instruments Widebus™ Family**
- **Operates From 1.65 V to 3.6 V**
- **Max $t_{pd}$ of 5 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

**DGG OR DL PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## description/ordering information

This 12-bit to 24-bit registered bus exchanger is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

The SN74ALVCH16269 is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. The device is particularly suitable as an interface between synchronous DRAMs and high-speed microprocessors.

Data is stored in the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ($\overline{\text{CLKENA}}$) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B port. For data transfer in the B-to-A direction, a single storage register is provided. The select ($\overline{\text{SEL}}$) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ($\overline{\text{OEA}}$, $\overline{\text{OEB1}}$, $\overline{\text{OEB2}}$).

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | SSOP − DL | Tube | SN74ALVCH16269DL | ALVCH16269 |
| | | Tape and reel | SN74ALVCH16269DLR | |
| | TSSOP − DGG | Tape and reel | SN74ALVCH16269DGGR | ALVCH16269 |
| | VFBGA − GQL | Tape and reel | SN74ALVCH16269KR | VH269 |
| | VFBGA − ZQL (Pb-free) | | 74ALVCH16269ZQLR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

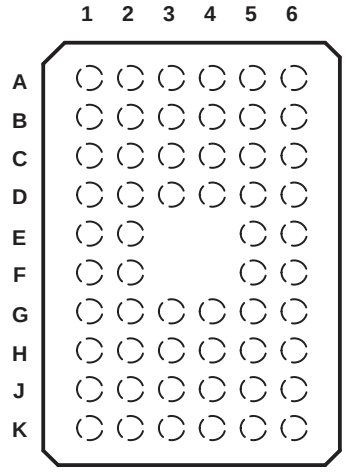
Widebus is a trademark of Texas Instruments.

## description/ordering information (continued)

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible, and $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to $\overline{OE}$ being routed through a register, the active state of the outputs cannot be determined before the arrival of the first clock pulse.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**GQL OR ZQL PACKAGE**
**(TOP VIEW)**




### terminal assignments

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | 2B3 | $\overline{OEB1}$ | $\overline{OEA}$ | $\overline{OEB2}$ | $\overline{CLKENA2}$ | 2B4 |
| B | 2B1 | 2B2 | GND | GND | 2B5 | 2B6 |
| C | A2 | A1 | $V_{CC}$ | $V_{CC}$ | 2B7 | 2B8 |
| D | A4 | A3 | GND | GND | 2B9 | 2B10 |
| E | A6 | A5 | | | 2B11 | 2B12 |
| F | A7 | A8 | | | 1B11 | 1B12 |
| G | A9 | A10 | GND | GND | 1B9 | 1B10 |
| H | A11 | A12 | $V_{CC}$ | $V_{CC}$ | 1B7 | 1B8 |
| J | 1B1 | 1B2 | GND | GND | 1B5 | 1B6 |
| K | 1B3 | NC | $\overline{SEL}$ | CLK | $\overline{CLKENA1}$ | 1B4 |

## Function Tables

**OUTPUT ENABLE**

| INPUTS | | | OUTPUTS | |
|---|---|---|---|---|
| CLK | $\overline{OEA}$ | $\overline{OEB}$ | A | 1B, 2B |
| ↑ | H | H | Z | Z |
| ↑ | H | L | Z | Active |
| ↑ | L | H | Active | Z |
| ↑ | L | L | Active | Active |

**A-TO-B STORAGE ($\overline{OEB}$ = L)**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{CLKENA1}$ | $\overline{CLKENA2}$ | CLK | A | 1B | 2B |
| L | H | ↑ | L | L | $2B_0$† |
| L | H | ↑ | H | H | $2B_0$† |
| L | L | ↑ | L | L | L |
| L | L | ↑ | H | H | H |
| H | L | ↑ | L | $1B_0$† | L |
| H | L | ↑ | H | $1B_0$† | H |
| H | H | X | X | $1B_0$† | $2B_0$† |

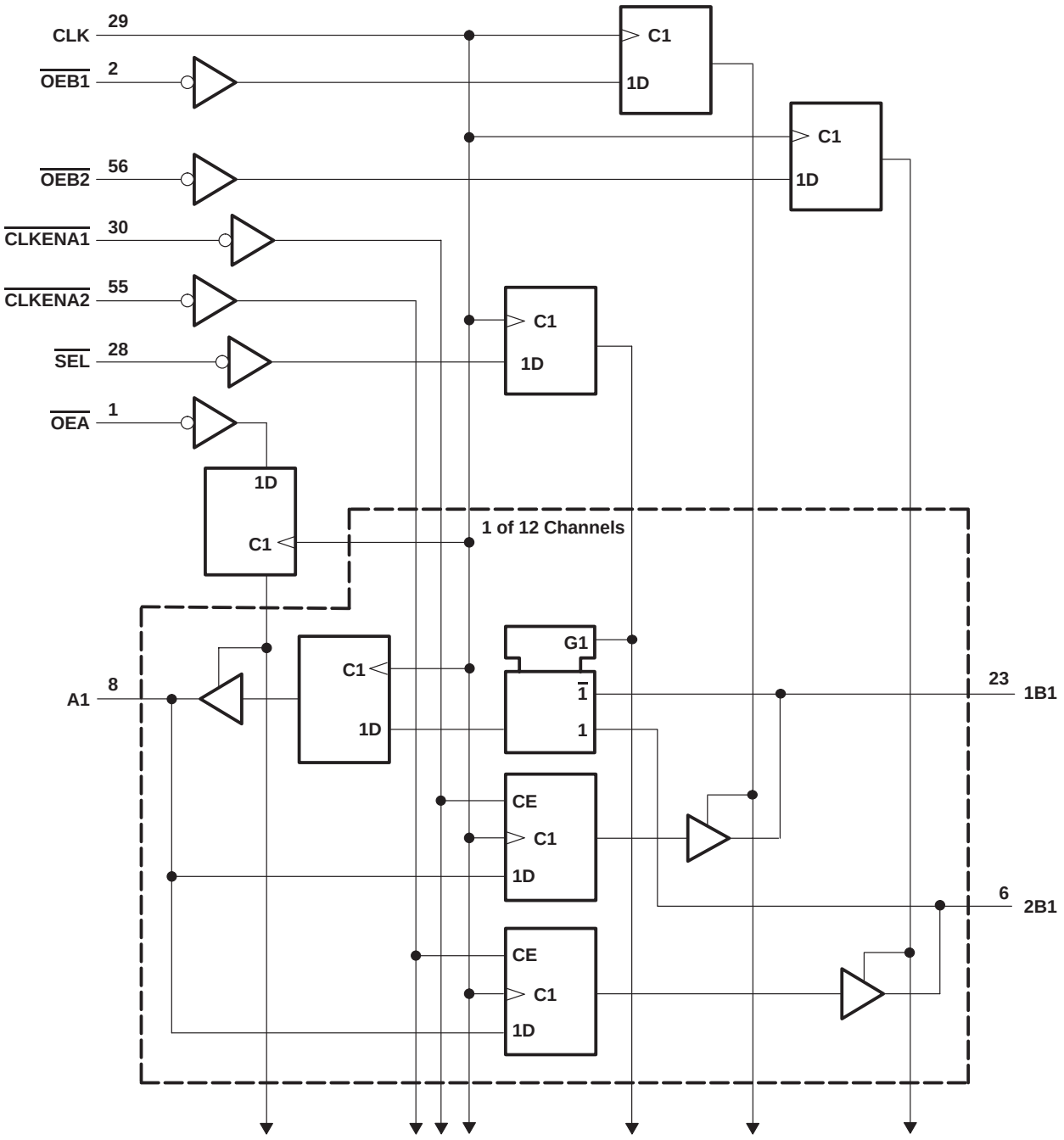
† Output level before the indicated steady-state input conditions were established

**B-TO-A STORAGE ($\overline{OEA}$ = L)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| CLK | $\overline{SEL}$ | 1B | 2B | A |
| X | H | X | X | $A_0$† |
| X | L | X | X | $A_0$† |
| ↑ | H | L | X | L |
| ↑ | H | H | X | H |
| ↑ | L | X | L | L |
| ↑ | L | X | H | H |

† Output level before the indicated steady-state input conditions were established

## logic diagram (positive logic)




Pin numbers shown are for the DGG and DL packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Input voltage range, $V_I$: Except I/O ports (see Note 1) . . . . . −0.5 V to 4.6 V
I/O ports (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . −50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . −50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package . . . . . 81°C/W
DL package . . . . . 74°C/W
GQL/ZQL package . . . . . 42°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | −4 | mA |
| | | $V_{CC}$ = 2.3 V | | −12 | |
| | | $V_{CC}$ = 2.7 V | | −12 | |
| | | $V_{CC}$ = 3 V | | −24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 12 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = −100 μA | | 1.65 V to 3.6 V | $V_{CC}$−0.2 | | | V |
| | | $I_{OH}$ = −4 mA | | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = −6 mA | | 2.3 V | 2 | | | |
| | | $I_{OH}$ = −12 mA | | 2.3 V | 1.7 | | | |
| | | | | 2.7 V | 2.2 | | | |
| | | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = −24 mA | | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 1.65 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 6 mA | | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 12 mA | | 2.3 V | | | 0.7 | |
| | | | | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | | 3.6 V | | | ±5 | μA |
| $I_{I(hold)}$ | | $V_I$ = 0.58 V | | 1.65 V | 25 | | | μA |
| | | $V_I$ = 1.07 V | | 1.65 V | −25 | | | |
| | | $V_I$ = 0.7 V | | 2.3 V | 45 | | | |
| | | $V_I$ = 1.7 V | | 2.3 V | −45 | | | |
| | | $V_I$ = 0.8 V | | 3 V | 75 | | | |
| | | $V_I$ = 2 V | | 3 V | −75 | | | |
| | | $V_I$ = 0 to 3.6 V‡ | | 3.6 V | | | ±500 | |
| $I_{OZ}$§ | | $V_O$ = $V_{CC}$ or GND | | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ − 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | μA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 3.5 | | pF |
| $C_{io}$ | A or B ports | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 9 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | | $V_{CC}$ = 1.8 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | † | | 135 | | 135 | | 135 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | † | | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time | A data before CLK↑ | † | | 2 | | 2 | | 1.7 | | ns |
| | | B data before CLK↑ | † | | 2.2 | | 2.1 | | 1.8 | | |
| | | $\overline{SEL}$ before CLK↑ | † | | 1.6 | | 1.6 | | 1.3 | | |
| | | $\overline{CLKENA1}$ or $\overline{CLKENA2}$ before CLK↑ | † | | 1 | | 1.2 | | 0.9 | | |
| | | $\overline{OE}$ before CLK↑ | † | | 1.5 | | 1.6 | | 1.3 | | |
| $t_h$ | Hold time | A data after CLK↑ | † | | 0.7 | | 0.6 | | 0.6 | | ns |
| | | B data after CLK↑ | † | | 0.7 | | 0.6 | | 0.6 | | |
| | | $\overline{SEL}$ after CLK↑ | † | | 1.1 | | 0.7 | | 0.7 | | |
| | | $\overline{CLKENA1}$ or $\overline{CLKENA2}$ after CLK↑ | † | | 1 | | 0.8 | | 1.1 | | |
| | | $\overline{OE}$ after CLK↑ | † | | 0.8 | | 0.8 | | 0.8 | | |

† This information was not available at the time of publication.

### switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | † | | 135 | | 135 | | 135 | | MHz |
| $t_{pd}$ | CLK | B | | † | 1 | 8.2 | | 7.3 | 1 | 6.2 | ns |
| | | A | | † | 1 | 6.4 | | 5.8 | 1 | 5 | |
| $t_{en}$ | CLK | B | | † | 1 | 7.9 | | 6.7 | 1 | 6.1 | ns |
| | | A | | † | 1 | 7.6 | | 6.2 | 1 | 5.9 | |
| $t_{dis}$ | CLK | B | | † | 1 | 8.1 | | 6.9 | 1 | 6.1 | ns |
| | | A | | † | 1 | 7.5 | | 6.8 | 1 | 5.6 | |

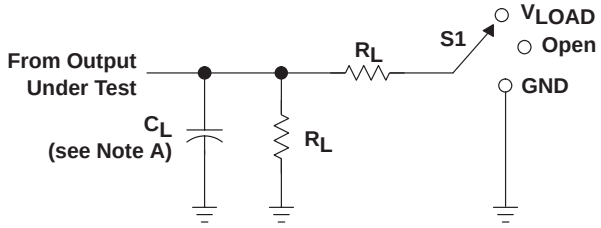
† This information was not available at the time of publication.

### operating characteristics, $T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance per exchanger | All outputs enabled | $C_L$ = 50 pF, f = 10 MHz | † | 87 | 120 | pF |
| | | All outputs disabled | | † | 80.5 | 118 | |

† This information was not available at the time of publication.

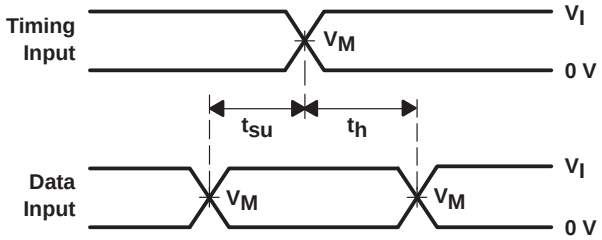
## PARAMETER MEASUREMENT INFORMATION



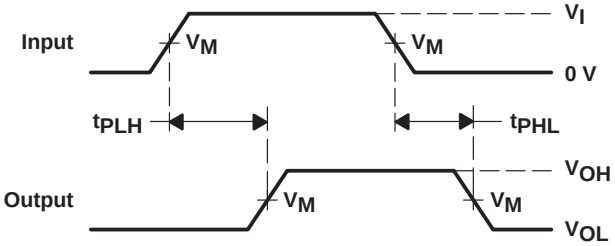

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

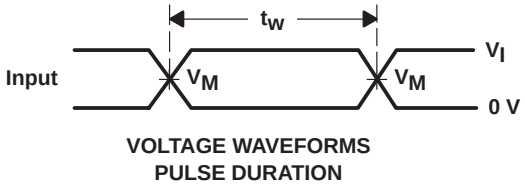
| $V_{CC}$ | INPUT | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



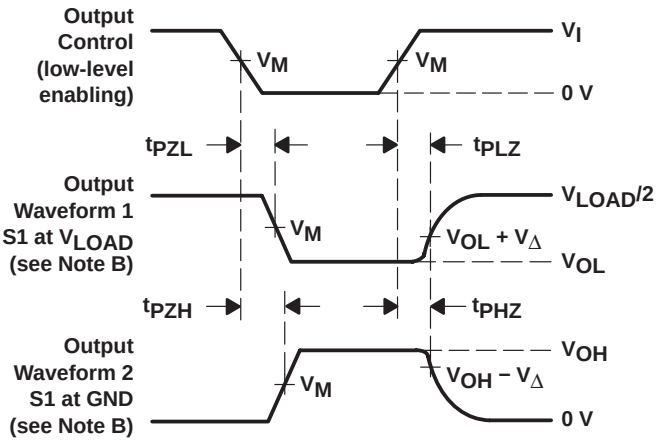

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

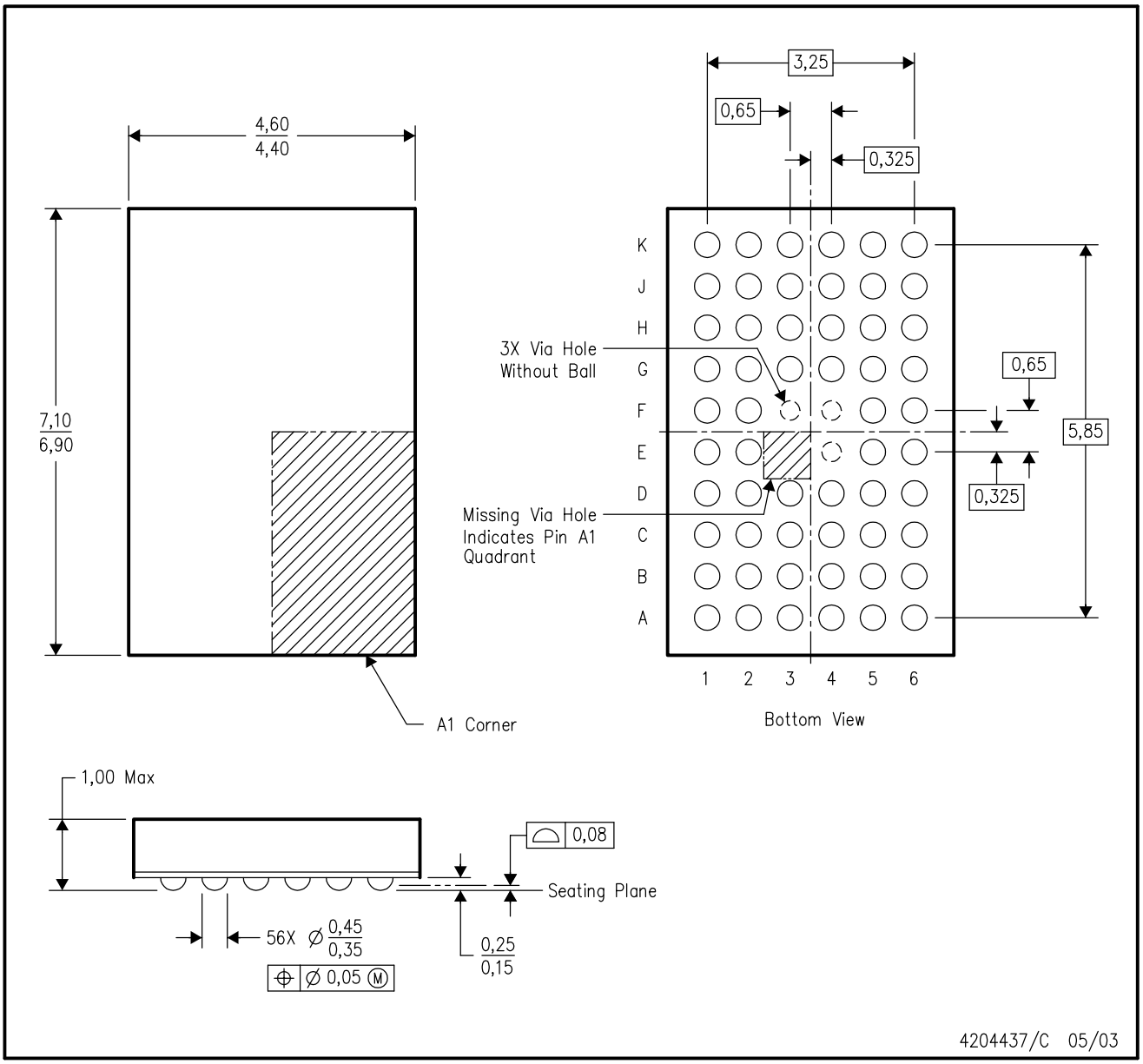



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

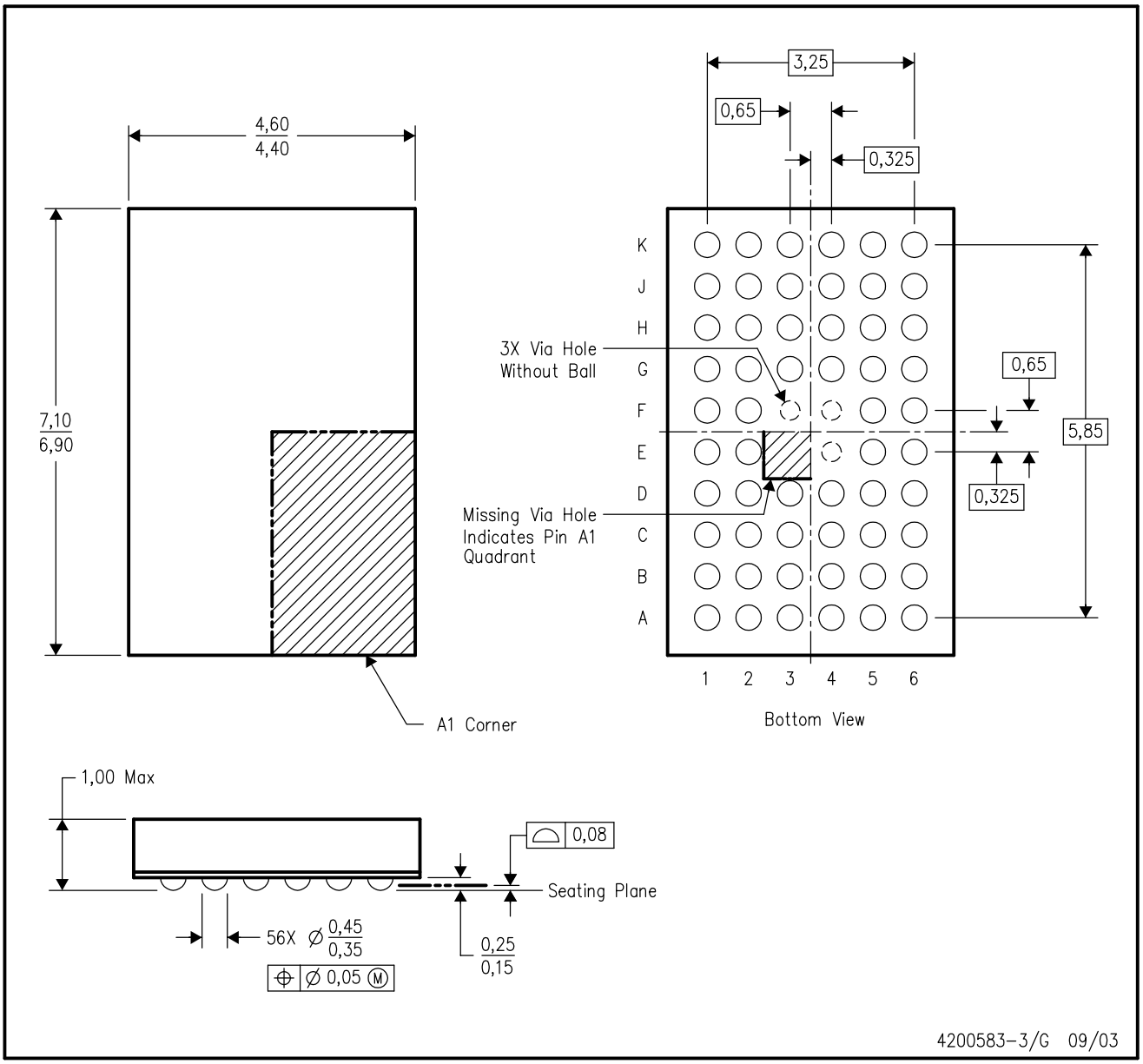
ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration.
D. Falls within JEDEC MO–225 variation BA.
E. This package is lead–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.

GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY

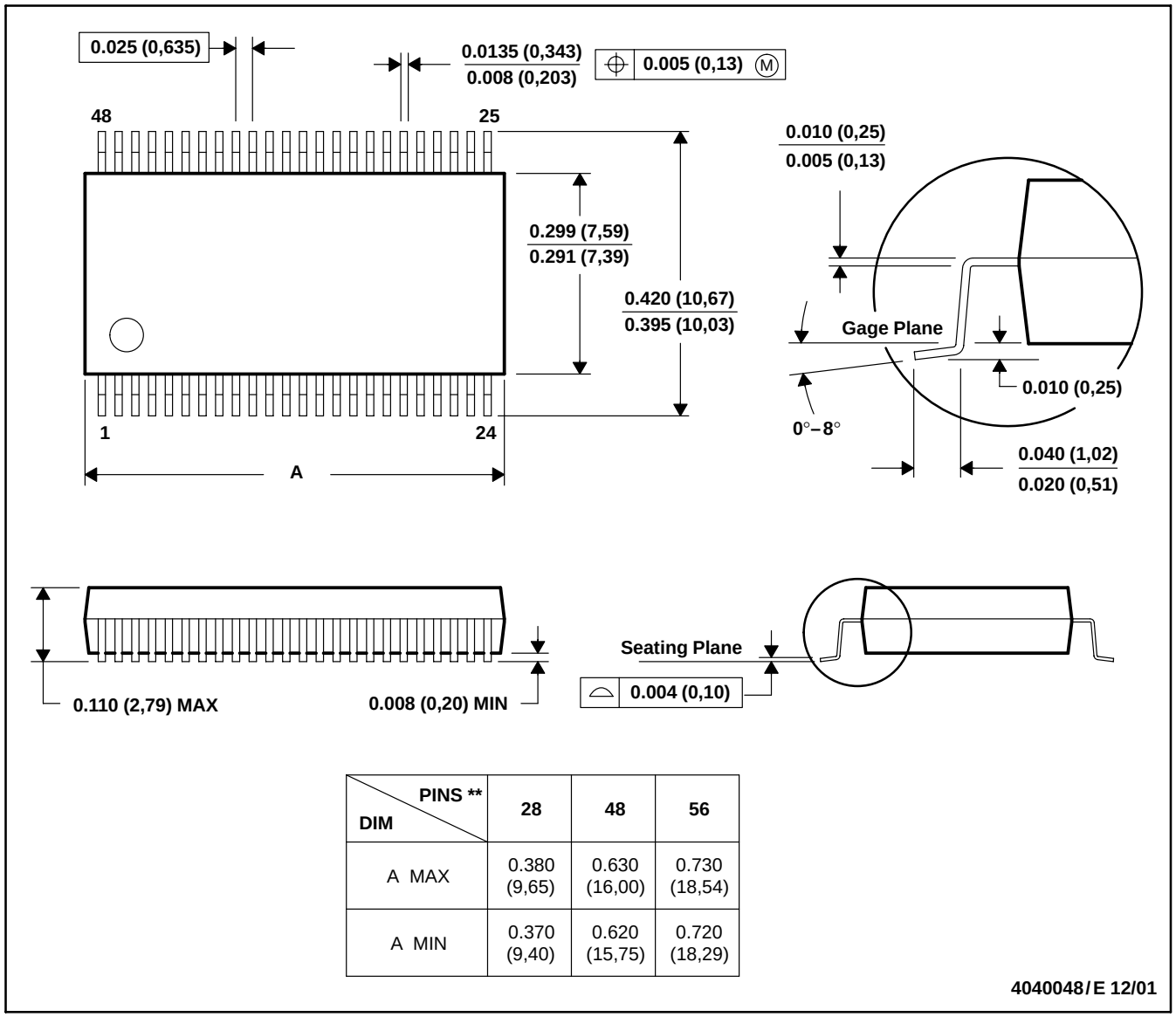



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration.
D. Falls within JEDEC MO–225 variation BA.
E. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

MicroStar Junior is a trademark of Texas Instruments.

**DL (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**



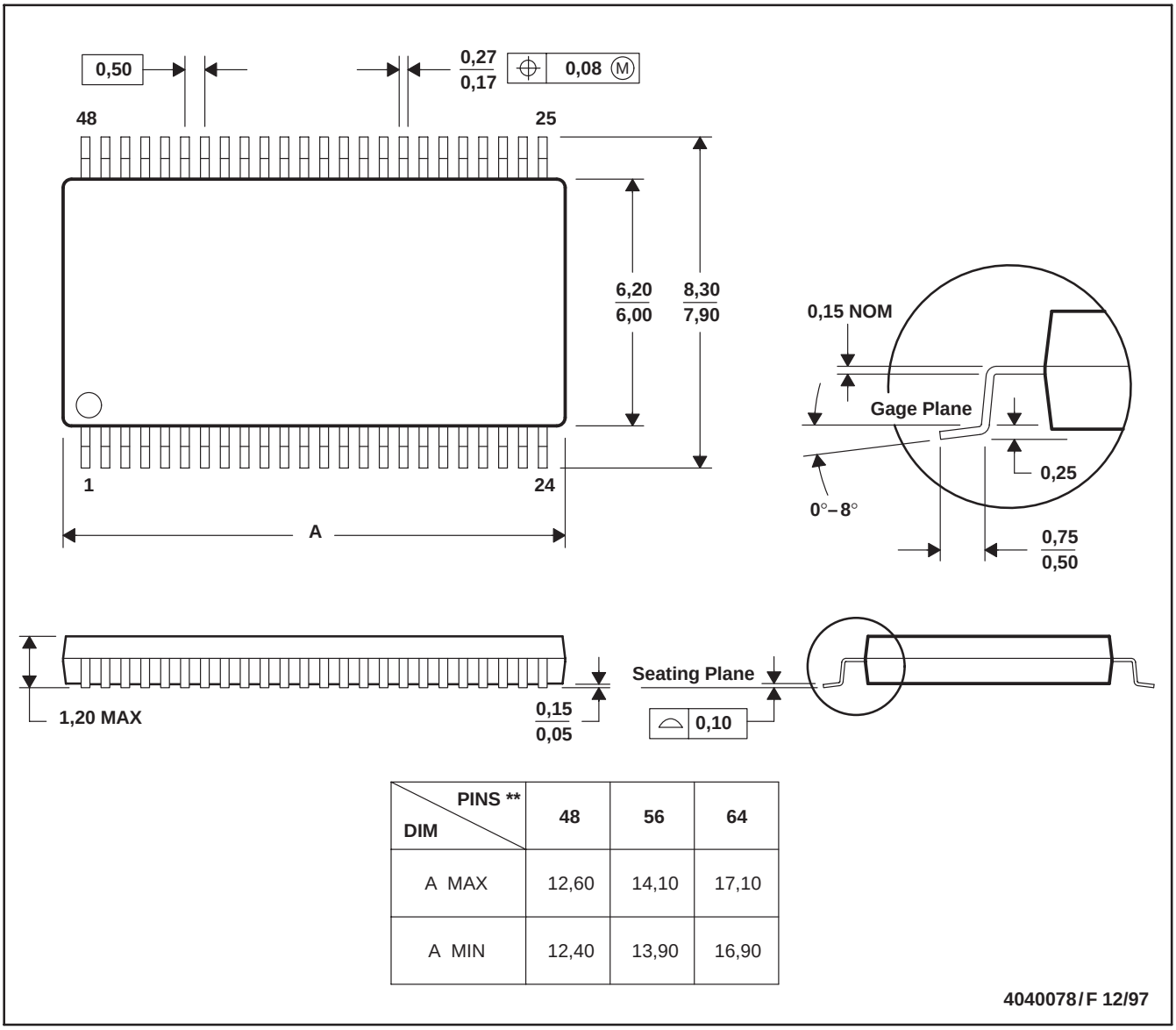

| DIM \ PINS ** | 28 | 48 | 56 |
|---|---|---|---|
| A MAX | 0.380 (9,65) | 0.630 (16,00) | 0.730 (18,54) |
| A MIN | 0.370 (9,40) | 0.620 (15,75) | 0.720 (18,29) |

**4040048/E 12/01**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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